

## ABSTRACT

### **Accurate Modeling of Transistor Stacks to Effectively Reduce Total Standby Leakage in Nano-Scale CMOS Circuits**

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In this work we have developed an accurate model of total leakage in a transistor stack based on the compact model of gate, subthreshold and band-to-band-tunneling leakage. Using this model, we have analyzed the opportunities for overall stand-by leakage reduction in scaled devices using transistor stacking and proved that the best input vector that minimize overall leakage depends on the relative magnitude of the different leakage components. A novel stacking technique based on the ratio of the different leakage components is proposed and its effectiveness in total leakage reduction in transistor stack and logic gate is analyzed.