# A 50-mW/ch 2.5-Gb/s/ch Data Recovery Circuit for the SFI-5 Interface Using Novel Eye-tracking Method

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We developed a 2.5-Gb/s/ch digital data recovery (DR) circuit for the SFI-5 interface. Our unique approach of treating a sequential 16-bit incoming data as one unit achieved a fully digital “eye-tracking” DR circuit. Fabricated by 0.18-μm SiGe-BiCMOS technology, the area of the DR circuit is 0.02-$mm^2$/ch and its power consumption is 50 mW/ch at 1.8 V. The measured jitter tolerance at 2.5 Gb/s is 0.7 UI p-p, which satisfies the jitter specifications for the SFI-5.