A Memory Using One-Transistor Gain Cell on SOI(FBC) with Performance Suitable for Embedded DRAM's

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A 288Kbit memory featuring a one-transistor gain cell on SOI of the size 0.21um^2 is presented and basic characteristics of the cell and the memory performance are disclosed. The threshold voltages of a cell transistor for data "1" and "0" are measured and a fail bit map is obtained. A sensing scheme is verified to be working and the random access time is measured. The retention time demonstrates to satisfy specifications for some embedded DRAM's.