Ultimate Solution for Low Thermal Budget Gate Spacer and Etch Stopper to Retard Short Channel Effect in Sub-90nm Devices

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For the first time, by employing low thermal budget processes of ALD SiO_2 and ALD SiN as gate spacer and silicide blocking layer, the short channel effects of CMOSFETs are significantly suppressed. Using the ALD SiO_2 and ALD SiN processes, we achieved excellent Vth roll-off characteristics in PMOS, which results in 10% increase of drive current and 15% decrease of inverter delay time. In conclusion, ALD processes of extremely low thermal budget are successfully implemented to sub-90nm CMOSFETs.