

# Fin-Array-FET on bulk silicon for sub-100 nm Trench Capacitor DRAM

R. Katsumata, N. Tsuda\*, J. Idebuchi\*, M. Kondo, N. Aoki, S. Ito, K. Yahashi\*, T. Satonaka\*,  
M. Morikado, M. Kito, M. Kido, T. Tanaka, H. Aochi and T. Hamamoto

SoC Research & Development Center and Process & Manufacturing Engineering Center\*,  
TOSHIBA Corporation, Semiconductor Company,

8, Shinsugita-cho, Isogo-ku, Yokohama, 235-8522, JAPAN

Fin gate array transistor (Fin-Array-FET) fabricated on bulk silicon substrate is applied to the DRAM cell with the deep trench capacitor. Fin-Array-FET is designed by using the 3-D process simulator and the 3-D device simulator. The device performance is evaluated by the electrical measurement of the test structure. It is demonstrated that Fin-Array-FET is the best candidate for the future high-speed DRAM cell by the sub-100 nm technologies.