

75 Word Abstract

Robust Process Integration of 0.78 μm^2 Embedded SRAM with NiSi Gate and Low-K Cu Interconnect for 90nm SoC Applications

Y.W. Kim, J. H. Ahn, T.S. Park, C.B. Oh, K.T. Lee, H. S. Kang, D.H. Lee, Y.G. Ko, K.S. Cheong, J.W. Jun, S.H. Liu
J.Kim[†], J.L.Nam[†], S.R.Ha[‡], J.B. Park,^{*}, S.A. Song^{*} and K.P. Suh

Technology Development, System LSI division, Samsung Electronics, [†]R&D Center, Memory division, Samsung Electronics
[‡]K1 Business, System LSI division, Samsung Electronics, ^{*}AE Center, Samsung Advance Institute of Technology
San 24 Nongseo-Ri, Kiheung-Eup, Yongin City, Kyunggi-Do, 449-711, Korea
Phone: +82-31-209-6590 E-mail: youngwug.kim@samsung.com

Abstract

The smallest high density embedded 0.78 μm^2 6T-SRAM cell for high performance 90nm SoC applications was successively integrated by using leading edge technologies such as 193nm ArF lithography, 1.2nm gate oxide, 50nm transistor and Cu dual damascene with low-K dielectric. Fully working for SRAM shows the SNM value above 200mV. Device current of 870 $\mu\text{A}/\mu\text{m}$ and 390 $\mu\text{A}/\mu\text{m}$ for NMOS and PMOS respectively is achieved at 1.0V operation. Reliability life time on hot carrier immunity shows more than 10 years.