

# Abstract

## High Performance/Reliability Cu Interconnect with Selective CoWP Cap

T. Ko, C. L. Chang, S. W. Chou, M. W. Lin, C. J. Lin, C.H. Shih, H.W. Su, M.H. Tsai, Winston S. Shue,  
and M. S. Liang

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC)  
6, Li-Hsin 6th Rd., Science-Based Industrial Park Hsin-Chu, Taiwan 300, R.O.C.  
E-mail: [winston\\_shue@tsmc.com.tw](mailto:winston_shue@tsmc.com.tw), TEL: 886-3-666-6666 ex 5353, FAX : 886-3-577-3671

In this work, a selective CoWP metal cap was employed after Cu CMP process for replacing conventional dielectric cap layer platform. A 5% reduction in RC delay was demonstrated for this new approach. The CoWP cap layer improves the interface between Cu and dielectric layer which reduces the Cu surface migration. EM for both via and trench shows more than 10X improvement. With optimized thickness and deposited process, 100% yield of line to line leakages, via chain Rc, and metal line Rs can be achieved. A semi-quantitative model was employed to determine surface migration dominating EM failure.