TECHNOLOGY RUMP SESSIONS
Wednesday, June 14
8:00 p.m. – 10:00 p.m.

Organizers: Shahin Sharifzadeh, Cypress Semi.
Renichi Yamada, Hitachi, Ltd.

RJ1 Power Management: What are the Device and Circuit Trade-offs. How Will it be Managed at 45nm and 32nm Nodes

Tapa I

Organizers:

Circuits	**Technology**
K. Nowka, IBM	H. Puchner, Cypress
Y. Oowaki, Toshiba	T. Ipposhi, Renesas

Moderator: T. Skotnicki, STMicroelectronics

Power management has historically focused on low standby and operating power for mobile devices to increase the battery time. In today's designs, it is increasingly important to optimize power for all electronic applications. Data centers can consume the power of small cities. Previous efforts for power reduction have been focusing on technology as well as design options to reduce standby power. However, it is not clear which of the options will be available in future designs and what other limitations will arise from these reduction techniques. The discussion panel is a compilation of design and process experts and will present views on power management for the 45-nm and 32-nm technology nodes. The panelists will present classical power reduction techniques such as gate leakage, sleeper transistors, cascading, fundamental improvements in leakage performance due to new device architectures. Various techniques will be debated on their merits for high-power vs low-power products or memory-intensive vs logic-dominated designs and technologies.

Panelists

Y. Urakawa, Toshiba
U. Ko, Texas Instruments
D. Frank, IBM
R. Kumar, Intel Corp
Y. Yamagata, NEC Electronics
D. Ditzel, Transmeta

R2: Embedded Memory in the Early 21st Century

Honolulu I

Moderator: S. Thompson, University of Florida
A. Nitayama, Toshiba

Two trends are making embedded memories a winning strategy: slowing of technology scaling and product requirements for large memories. A panel of industry experts will discuss

(1) Application field /market segmentations and forecast in next 10 years: consumer products, portable communication products, high-end products

(2) Forecast of dominant technologies. What e-memory technology will dominate the SoC memory markets during next 10 years?

(3) Volatile vs. Non-volatile or unified memory? When will unified memory be realized?

Panelists:

T. Ning, IBM
K. Zhang, Intel
C. Wang, TSMC
S. Fujii, Toshiba
K.-M. Chang, Freescale

R2: 3-D Integration

Honolulu II

Moderators: K. Saraswat, Stanford University
M. Koyanagi. Tohoku University

The unprecedented growth of the computer and the information technology industry is demanding ULSI circuits with increasing functionality and performance at minimum cost and power dissipation. ULSI circuits are being aggressively scaled to meet this demand. This in turn has introduced some very serious problems for the semiconductor industry. Scaling is reducing gate delays but rapidly increasing interconnect delays. Increasing drive for the integration of disparate signals and technologies is introducing various system-on-a-chip (SoC) design concepts, for which existing planar (2-D) IC design may not be suitable. 3-D chip design strategy that exploits the vertical dimension could alleviate the interconnect related problems and could facilitate SoC applications through heterogeneous integration. However there are many questions to be resolved. For which products 3D makes sense? There are many promising technologies, (wafer bonding, layer transfer, crystallization, epitaxial growth) for manufacturing 3-D ICs. Which technology is useful for which system application? Is 3D technology viable economically? One of the major concerns in 3-D ICs arises due to increased power. Will we have advanced heat sinking technology necessary to achieve maximum performance from the 3D chips?

Panelists:

C. Keast, Massachusetts Institute of Technology
S. Wong, Stanford University
R. Madurawe, VICICIV
A. Matsuzawa, Tokyo Institute of Technology
K. Takahashi, Toshiba
K. Lee, Samsung