SESSION 10 – TAPA I
Mobility Enhancement on Process Induced Strain

Wednesday, June 14, 10:25 a.m.
Chairpersons: F. Nouri, Applied Materials Inc.
T. Kuroi, Renesas Technology Corp.

10.1 – 10:25 a.m.
Integration of Local Stress Techniques with Strained-Si Directly On Insulator (SSDOI) Substrates, H. Yin, Z. Ren, H. Chen, J. Holt, X. Liu*, J. W. Sleight, K. Rim, V. Chan, D.M. Fried, Y.H. Kim*, J.O. Chu*, B.J. Greene, S.W. Bedell*, G. Pfeiffer, R. Bendernagel, D.K. Sadana*, T. Kanarsky, C.Y. Sung*, M. Ieong*, G. Shahidi*, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, *IBM T.J. Watson Research Center, Yorktown Heights, NY

Various local stress techniques have been integrated on strained-Si directly on insulator (SSDOI) substrates, including dual stress liner (DSL), stress memory technique (SMT), and embedded SiGe (eSiGe) in source/drain. SMT shows mild drive current enhancement on nFETs. PFETs with eSiGe exhibit significant enhancement, suggesting eSiGe compatibility with SSDOI is excellent. A ring oscillator delay of 3ps is achieved at leakage current of 1/uAμm and VDD=1.1V.

10.2 – 10:50 a.m.
Stress Memorization Technique (SMT) Optimization for 45nm CMOS, C. Ortolland[1,5], P. Morin[2], C. Chaton[3], E. Mastromatteo[1], C. Populaire[4], S. Orain[1], F. Leverd[2], P. Stolk[1], F. Boeuf[2], F. Arnaud[2], [1]Philips Semiconductors, Crolles, France, [2]STMicroelectronics, Crolles, France, [3]CEA-LETI, Crolles, France, [4]Freescale Semiconductor, Crolles, France, [5]Laboratoire Physique de la Matiere, Villeurbanne, France

In this paper, we present an optimization path of Stress Memorization Technique (SMT) for 45nm node and below using a nitride capping layer. We demonstrate that the understanding of coupling between nitride properties, dopant activation and Poly-Silicon gate mechanical stress allows enhancing nMOS performance by 7% without pMOS degradation. In contrast to previously reported works on SMT [1-3], a low-cost process compatible with consumer electronics requirements has been successfully developed.

10.3 – 11:15 a.m.
NiSi Schottky Barrier Process-Strained Si (SB-PSS) CMOS Technology for High Performance Applications, C.H. Ko, H.W. Chen, T.J. Wang, T.M. Kuan, J.W. Hsu, C.Y. Huang, C.H. Ge, L.S. Lai, W.C. Lee, Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan

State-of-the-art process-strained Si (PSS) technology featuring single-NiSi Schottky source/drain (S/D) and ultra-thin gate oxide of 1.2 nm is demonstrated for Lgate down to 39 nm. +10% performance boost of Schottky-Barrier (SB)-PSS NMOS, as compared to its non-Schottky counterpart, is demonstrated due to series resistance reduction of the silicide S/D and enhanced strain effects. Highest SB-PSS PMOS drive current of 821 mA/mm (at VD= −1.2V and Ioff=100 nA/mm) is recorded when integrated with recessed Si1-xGex S/D stressor.

10.4 – 11:40 a.m.
A Low Cost Drive Current Enhancement Technique Using Shallow Trench Isolation Induced Stress for 45-nm Node, C. Le Cam, F. Guyader*, C. de Buttet**, P. Guyader*, G. Ribes*, M. Sardo*, S. Vanbergue, F. Boeuf*, F. Arnaud*, E. Josse*, M. Haond*, Philips Semi., Crolles, France, *STMicroelectronics, Crolles, France, **Freescale Semi., Crolles, France

This paper demonstrates, for the first time, that sub-atmospheric chemical vapour deposition (SACVD) oxide is a good candidate for 45-nm node as Shallow Trench Isolation (STI) gap-fill as well as a mobility enhancement technique for both <100> and <110> channel orientations. 11% and 18% drive current enhancement for NMOS and PMOS transistors are reported leading to a 12% ring oscillator speed improvement compared to a conventional High Density Plasma (HDP) process.