

SESSION 14 – TAPA I
Advanced Interconnect Technology

Wednesday, June 14, 3:25 p.m.

Chairpersons: B. van Schravendijk, Novellus Systems, Inc.
Y. Takao, Fujitsu Ltd.

14.1 – 3:25 p.m.

High-performance Cu-interconnects with Novel Seamless Low-k SiOCH Stacks (SEALS) Featured by Compositional Modulation Process for 45nm-node ULSI Devices, M. Tagami, H. Ohtake, M. Tada, M. Ueki, F. Ito, T. Taiji*, Y. Kasama*, T. Iwamoto, H. Wakabayashi, T. Fukai*, K. Arai, S. Saito, H. Yamamoto, M. Abe, M. Narihiro, N. Furutake, T. Onodera, T. Takeuchi, Y. Tsuchiya*, N. Oda*, M. Sekine*, M. Hane, Y. Hayashi, NEC Corporation, Kanagawa, Japan, *NEC Electronics Corporation, Kanagawa, Japan

Damage-free, self-organized Cu dual-damascene (DD) interconnects have been developed for 45nm-node ULSIs with novel “seamless low-k SiOCH stacks” (SEALS) featured by compositional modulation in PECVD processes. In the SEALS ($k_{eff}=2.9$), a carbon-rich porous SiOCH ($k=2.45$) is stacked directly on an oxygen-rich porous-SiOCH ($k=2.7$) without etch-stop (ES) or buffer layer, while a non-porous, oxygen-rich SiOCH ($k=3.1$) is put on the top as the hard-mask (HM). Unique chemistry-controlled plasma-etching and CMP are essential to the damage-free, DD profile control without SiO₂-HM and ES. The 140nm-pitched Cu line has only 85fF/mm (single-load) due to the low k_{eff} , and the interconnect delay of 45nm-node CMOS ring oscillator is reduced by 10% referring to that of the 45nm-node DD interconnect with SiO₂-HM and ES. The Cu DD interconnect with SEALS is a strong candidate for high-speed and low-power, 45nm-node ULSIs.

14.2 – 3:50 p.m.

Thermally and Chemically Robust, Non-Reflowable Low-k Spin-on Glass ($k = 2.4$) for Gap-filling Technology in Sub-50-nm Memory Devices, D. Ryuzaki, H. Sakurai, T. Yoshikawa, K. Torii, Hitachi Chemical Co. Ltd., Tokyo, Japan

A novel non-reflowable low-k spin-on glass (NR-SOG, $k = 2.4$) has been developed for the gap-filling technology in sub-50-nm memory devices. The new SOG has planarizing capability as high as conventional reflowable SOGs have, while it has thermal stability up to 800C and high chemical stability. A damage-less via-formation process was also developed to integrate NR-SOG into interconnects. The fabricated interconnects with minimum spacing of 50 nm showed sufficiently low capacitance and high TDDB reliability.

14.3 – 4:15 p.m.

Direct Non-contact Electrical Measurement of Low-k Damage in Patterned Low-k Films by a Near-Field Scanned Microwave Probe, J.S. Tsai, J.W. Hsu, V.V. Talanov*, A. Scherz*, A.R. Schwartz*, J.H. Shieh, S.M. Jang, M.S. Liang, Taiwan Semiconductor Manufacturing Co. Ltd., Hsinchu, Taiwan, *Neocera, Inc., Beltsville, MD

We demonstrate a near-field scanned microwave probe and specific test keys for direct non-contact electrical measurement of low-k dielectric constant and damage after deposition, during trench/via processing, and after metallization. This work successfully defines the dielectric constant and the thickness of the damaged layer in patterned low-k films, and is the first demonstration of a metrology for electrical in-line measurements of low-k damage. Furthermore, we point out the integration issue of porous low-k by using this novel technique.

14.4 – 4:40 p.m.

Integration of Self-Formed Barrier Technology for 32nm-node Cu Dual-Damascene Interconnects with Hybrid Low-k (PAr/SiOC) Structure, Y. Ohoka, K. Inoue, T. Hayashi, N. Komai, S. Arakawa, R. Kanamura, S. Kadomura, Sony Corporation, Kanagawa, Japan

Self-formed MnOx barrier technology has been successfully integrated for 150nm pitch Cu dual-damascene interconnects with PAr/SiOC ($k=2.65$) hybrid structure. Barrier formation at the interface of Cu and various low-k films with few Si or O was confirmed by adhesion, XPS and TEM/EDX analyses. No degradation of interconnect performance and excellent electromigration lifetime were verified. It is concluded that this self-formed barrier technology is a promising technique to satisfy the reliability requirement for 32nm-node Cu/Low-k interconnects.

14.5 – 5:05 p.m.

Lower Resistance Scaled Metal Contacts to Silicide for Advanced CMOS, A. Topol, C. Sheraw*, K. Wong*, X. Shao, R. Knarr*, S. Rossnagel, C.-C. Yang*, B. Baker-O’Neal, A. Simon*, B. Haran, Y. Li*, C. Ouyang, S. Allen*, C. Brodsky*, S. Cohen, L. Deligianni, X. Chen*, S. Deshpande*, C.Y. Sung*, M. Ieong, IBM T. J. Watson Research Center, Yortown Heights, NY, *IBM Systems and Technology, Hopewell Junction, NY

Self-formed MnOx barrier technology has been successfully integrated for 150nm pitch Cu dual-damascene interconnects with PAr/SiOC ($k=2.65$) hybrid structure. Barrier formation at the interface of Cu and various low-k films with few Si or O was confirmed by adhesion, XPS and TEM/EDX analyses. No degradation of interconnect performance and excellent electromigration lifetime were verified. It is concluded that this self-formed barrier technology is a promising technique to satisfy the reliability requirement for 32nm-node Cu/Low-k interconnects.