SESSION 15 – TAPA II
Alternative Non-Volatile Memory

Wednesday, June 14, 3:25 p.m.
Chairpersons: C. Dennison, Ovonyx Technologies, Inc.
T. Nakamura, Rohm Co., Ltd.

15.1 – 3:25 p.m.
Highly Reliable 256Mb PRAM with Advanced Ring Contact Technology and Novel Encapsulating Technology, Y.J. Song, K.C. Ryoo, Y.N. Hwang, C.W. Jeong, D.W. Lim, S.S. Park, J.I. Kim, J.H. Kim, S.Y. Lee, J.H. Kong, S.J. Ahn, S.H. Lee, J.H. Park, J.H. Oh, Y.T. Oh, J.S. Kim, J.M. Shin, J.H. Park, Y. Fai, G.H. Koh, G.T. Jeong. R.H. Kim, H.S. Lim, I.S. Park, H.S. Jeong, K. Kim, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea

Advanced ring type technology and encapsulating scheme were developed to fabricate highly manufacturable and reliable 256Mb PRAM. Very uniform BEC area was prepared by the advanced ring type technology in which core dielectrics were optimized for cell contact CMP process. In addition, relatively high set resistance was stabilized from encapsulating $Gb_2Sb_2Te_5$ (GST) stack with blocking layers, thus giving rise to a wide sensing window. These advanced ring type and encapsulating technologies can provide great potentials of developing high density 512Mb PRAM and beyond.

15.2 – 3:50 p.m.
Novel One-Mask Self-Heating Pillar Phase Change Memory, T.D. Happ*, M. Breitwisch, A. Schrott, J.B. Philipp*, M.H. Lee**, R. Cheek, T. Nirschl*, M. Lamorey, C.H. Ho**, S.H. Chen**, C.F. Chen**, E. Joseph, S. Zaidi*, G.W. Burr, B. Yee, Y.C. Chen**, S. Raoux, H.L. Lung**, R. Bergmann*, C. Lam, IBM, Yorktown Heights, NY, *Infineon Technologies, **Macronix International Co. Ltd.

A novel Pillar phase change memory based on fully integrated test arrays in 180nm CMOS technology has been successfully fabricated. A current-confining Pillar structure leads to self-heating at the center of the chalcogenide layer, and needs only one additional mask level for its fabrication. Switching characteristics with write currents less than 900uA at 75nm diameter are reported. Multilevel storage can further reduce the effective cell size, and different MLC program strategies have been compared.

15.3 – 4:15 p.m.
A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Applications, F. Pellizzer, A. Benvenuti, B. Gleixner*, Y. Kim*, B. Johnson*, M. Magistretti, T. Marangon, A. Pirovano, R. Bez, G. Atwood*, STMicroelectronics, Agrate Brianza, Italy, *Intel Corporation, Santa Clara, CA

A 90nm technology node Phase Change Memory process, based on a chalcogenide material storage element with a vertical pnp-BJT selector device, is presented. The small cell area of 12F2, the good electrical results, and the intrinsic reliability demonstrate the viability of the PCM cell concept. Programming currents as low as 400uA, very good distributional data achieved on multi-megabit arrays for programming (set and reset), endurance, and retention, demonstrate the suitability of PCM for fabrication of a high density array at 90nm.

15.4 – 4:40 p.m.
World Smallest 0.34µm^2 COB Cell 1T1C 64Mb FRAM with New Sensing Architecture and Highly Reliable MOCVD PZT Integration Technology, Y.M. Kang, H.J. Joo, J.H. Park, S.K. Kang, J.-H. Kim, S.G. Oh, H.S. Kim, J.Y. Kang, J.Y. Jung, D.Y. Choi, E.S. Lee, S. Y. Lee, H.S. Jeong, K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

We have demonstrated a 0.34um^2 COB cell 1T1C 64Mb FRAM at 150nm technology node. The signal window between of 64M bit cells was 300mV at 85°C, 1.6V VDD. This wide signal window was achieved by advanced anneal technology and optimized capacitor layout, from which the variation of individual cell charge was greatly improved, with 70nm thick MOCVD PZT. The multi-reference cell equalizing scheme, greatly improved the variation of the reference cell signal. As a result, no single bit failure was found in our 1T1C 64Mb FRAM after 500hour bake at 150°C.

15.5 – 5:05 p.m.
High Density and High Reliability Chain FeRAM with Damage-Robust MOCVD-PZT Capacitor with $SrRuO_3/IrO_2$ Top Electrode for 64Mb and Beyond, O. Hidaka, T. Ozaki, H. Kanaya, Y. Kumura, Y. Shimojo, S. Shuto, Y. Yamada, K. Yahashi, K. Yamakawa, S. Yamazaki, D. Takashima, T. Miyakawa, S. Shiratake, S. Ohtsuki*, I. Kunishima, A. Nitayama, Toshiba Corporation, Yokohama, Japan, *Toshiba Microelectronics Corporation, Yokohama, Japan

An excellent 64Mb chainFeRAMTM using a highly reliable capacitor with damage-robust MOCVD-PZT and $SrRuO_3/IrO_2$ top electrode (TE) is successfully demonstrated for the first time. A very large signal margin of 540mV at 1.8V is achieved for the capacitor as small as 0.19µm^2. Large sensing margin is well maintained after 85°C storage, and 10 years lifetime is successfully guaranteed. The combination of damage-robust MOCVD-PZT and optimized $SrRuO_3/IrO_2$ TE as well as a sophisticated 'chain' structure that has a small bit line capacitance (Cb) nature shows excellent reliability and scalability. This work demonstrates that high density 256Mb chain FeRAM with 0.1µm^2 planar capacitor can be realized.