SESSION 18 – TAPA I
Strain Enhanced High
Performance PMOS Devices

Thursday, June 15, 10:25 p.m.
Chairpersons: T. Grider, Texas Instruments
M. Masahara, AIST

**18.1 – 10:25 a.m.**
**Strained-Si, Relaxed-Ge Or Strained-(Si)Ge For Future Nanoscale p-MOSFETs?,** T. Krishnamohan, D. Kim, C. Jungemann*, Y. Nishi, K.C. Saraswat, Stanford University, Stanford, CA, *Technical University of Braunschweig, Germany

The optimal channel material (strained-Si, relaxed-Ge or strained-SiGe) and device geometries for future nanoscale DG p-MOSFETs are obtained through detailed BTBT (including band structure and quantum effects), Full-Band Monte-Carlo and 1-D Poisson-Schrodinger Simulations, and Experiments on ultra-thin (<10nm) SOI MOSFETs. The tradeoffs between drive current, intrinsic delay, BTBT leakage and short channel effects have been systematically compared. (x,0) strained-SiGe becomes the material of choice compared to (0,x) strained-Si for x>0.6. Optimal performance can be obtained in a sub-20nm, (1,0) s-Ge heterostructure p-MOSFET with an ultra-thin ~2nm strained-Ge channel.

**18.2 – 10:50 a.m.**
**Relationship Between Hole Mobility and Current Drive Enhancement in Uniaxially Strained Thin-Body SiGe-on-Insulator pMOSFETs,** T. Tezuka, T. Irisawa, T. Numata, Y. Moriyama, N. Hirashita, E. Toyoda*, K. Usuda, N. Sugiyama, S.-I. Takagi**, MIRAI-ASET, Kawasaki, Japan, *Toshiba Ceramics, Kawasaki, Japan, **MIRAI-AIST, Kawasaki, Japan

Hole mobility of uniaxially strained thin-body SiGe-on-Insulator (SGOI) pMOSFETs was directly measured and was compared with that of biaxially strained ones for the first time. The uniaxial stress was induced by lateral strain relaxation in narrow strained SGOI channels. It was demonstrated from the relation between the mobility enhancement and the short-channel Id enhancement that the uniaxial compressive strain can provide the significant enhancement in high field carrier transport as well as the low-field mobility.

**18.3 – 11:15 a.m.**
**Superior Current Enhancement in SiGe Channel p-MOSFETs Fabricated on (110) Surface,** P.W. Liu, J.W. Pan, T.Y. Chang, T.L. Tsai, T.F. Chen, Y.C. Liu, C.H. Tsai, B.C. Lan, Y.H. Lin, W.T. Chiang, C.T. Tsai, United Microelectronics Corporation, Hsin-Chu City, Taiwan

The promising potential of (110) SiGe channel as next generation high performance p-MOSFETs is well demon-strated in this work. As high as 48% of drive current enhancement on SiGe channel p-MOSFETs fabricated on (110) surface have been achieved for the first time. In addition, combining with compressive stress capping layer, the (110) SiGe channel p-MOSFETs exhibits an extended 81% Idsat gain with Idsat of 850uA/um at 100nA/um Ioff. The 32% larger longitudinal piezoresistance coefficient compared to Si extracted from SiGe channel p-MOSFET reveals the advantage of applying strain in SiGe channel. The 3.3× hole mobility enhancement of (110) SiGe over (100) Si illustrates the advantage of this device architecture.

**18.4 – 11:40 a.m.**
**Origin of Drivability Enhancement in Scaled pMOSFETs with 45° Rotated <100> Channels,** S. Saito, D. Hisamoto, Y. Kimura, N. Sugii, R. Tsuchiya, K. Torii, S. Kimura, Hitachi Ltd., Tokyo, Japan

We have elucidated the mechanism of the drive current enhancement in <100> channel pMOSFETs on (100) substrate. In spite of the huge anisotropic effective mass, the long channel mobility of <100> is identical to that of <110>, while it is enhanced when L and W are scaled. We found an evidence that the origin is process induced stress, and the mobility enhancement is theoretically supported by the reduction of the average effective mass in a diffusive transport regime. We propose that a combination of <100> channel and biaxial compressive stress is effective to enhance the mobility.