SESSION 20 – TAPA I
Advanced High K Stacks

Thursday, June 15, 1:30 p.m.
Chairpersons: S. Deleonibus, CEA-LETI
T. Kuroi, Renesas Technology Corp.

20.1 – 1:30 p.m.
Poly-Si/AlN/HfSiO Stack for Ideal Threshold Voltage and Mobility in Sub-100 nm MOSFETs, K.L. Lee, M.M. Frank, V. Paruchuri, E. Cartier, B. Linder, N. Bojarczuk, X. Wang*, J. Rubino, M. Steen, P. Kozlowski, J. Newbury, E. Sikorski, P. Flaitz*, M. Gribelyuk*, P. Jamison, G. Singco, V. Narayanan, S. Zafar, S. Guha, P. Oldiges*, R. Jammy, M. Ieong, IBM Research Division, Yorktown Heights, NY, *IBM Systems and Technology Group, Hopewell Junction, NY

A scalable poly-Si/AlN/HfSiO gate stack, implementing a new aluminum nitride (AlN) cap layer, combined with oxygen diffusion barrier, halo and counter doping and high temperature spike anneal for gate and junction activation, has been successfully developed to fully offset the large threshold voltage (Vt) shifts in poly-Si/HfSiO devices. Carrier mobilities are close to those of SiON control devices. We thus have achieved sub-100 nm device Vt of 0.3-0.4 V with PFETs Ion ~ 140 µA/µm at Ioff ~13 pA/µm, suitable for low-power CMOS technologies.

20.2 – 1:55 p.m.
Dual High-k Gate Dielectric Technology Using Selective AlO_x Etch (SAE) Process with Nitrogen and Fluorine Incorporation, H.-S. Jung, S.K. Han, H. Lim, Y.-S. Kim, M.J. Kim, M.Y. Yu, C.-K. Lee, M.S. Lee, Y.-S. You, Y. Chung*, S. Kim*, H.S. Baik*, J.-H. Lee, N.-I. Lee, H.-K. Kang, Samsung Electronics Co. Ltd., Kyunggi-Do, Korea, *Samsung Advanced Institute of Technology, Kyunggi-Do, Korea

We propose a novel Vth control method for HfO_2 with poly-Si and MIPS gates. By using a selective AlOx etch (SAE) process, we successfully integrate HfSiO/poly-Si for nMOS and HfSiO/AlO_x/poly-Si for pMOS. Therefore symmetrical Vth values of 0.43V/-0.44V have been obtained in poly-Si gate. For MIPS gate, we perform the SAE process with N2 and F incorporation. Consequently, nMOS Vth of 0.35V and pMOS Vth of -0.45V are obtained without counter channel doping.

20.3 – 2:20 p.m.
A Novel Remote Reactive Sink Layer Technique for the Control of N and O Concentrations in Metal/High-k Gate Stacks, Y. Akasaka[1], K. Shiraishi[2,3], N. Umezawa[3], O. Ogawa[1], T. Kasuya[1], T. Chikyow[3], F. Ootsuka[1], Y. Nara[1], K. Nakamura[1], [1]Semiconductor Leading Edge Technologies Inc., Ibaraki, Japan, [2]University of Tsukuba, Tsukuba, Japan, [3]National Institute for Materials Science

A novel technique for the control of nitrogen (N) and oxygen (O) concentrations in the metal/high-k gate stacks is proposed. By inserting a reactive metal (Ti) layer remote from work function metal and high-k insulator, N and O concentration is easily decreased. This technique effectively suppresses the EOT increase after high-temperature annealing. Moreover, improved electron mobility and decreased interfacial trap density can be obtained by this technique. We demonstrated MISFET with extremely high electron mobility and thin EOT can be easily obtained even with relaxed process of HfSiON.

20.4 – 2:45 p.m.
Sub-1nm EOT $HfSi_x/HfO_2$ Gate Stack Using Novel Si Extrusion Process for High Performance Application, T. Ando, T. Hirano, K. Tai, S. Yamaguchi, T. Kato, Y. Hagimoto, K. Watanabe, R. Yamamoto, S. Kanda, K. Nagano, S. Terauchi, Y. Tateshita, Y. Tagawa, M. Saito, H. Iwamoto, S. Yoshida*, H. Watanabe*, N.Nagashima, S. Kadomura, Sony Corporation, Kanagawa, Japan, *Osaka University, Osaka, Japan

We have succeeded in scaling down the EOT of nMOSFET to 0.9 nm without mobility degradation for the first time with $HfSi_x/HfO_2$ gate stacks. A low and well-controlled Vth was obtained from the low work function of $HfSi_x$.The resultant Ion (Ioff) of 1165 uA/um (81 nA/um) at Vdd = 1.0 V is the highest value reported in the industry for unstrained Si and even comparable to the state-of-the-art CMOS devices with strain enhanced technologies.