SESSION 6 – TAPA I
Non-Volatile Trapped Charge Memory

Tuesday, June 13, 3:25 p.m.
Chairpersons: K.-M. Chang, Freescale
J.H. Lee, MagnaChip Semiconductor Inc.

6.1 – 3:25 p.m.
A 4-Bit Double SONOS Memory (DSM) with 4 storage Nodes per Cell for Ultimate Multi-Bit Operation, C.W. Oh, S.H. Kim, N.Y. Kim, Y.L. Choi, K.H. Lee, B.S. Kim, N.M. Cho, S.B. Kim, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyungki-Do, Korea

6.2 – 3:50 p.m.
A Novel Non-Volatile Memory Cell Using a Gated-Diode Structure with a Trapping-Nitride Storage Layer, W.J. Tsai, T.F. Ou, H.L. Kao, E.K. Lai, Y.Y. Liao, C.C. Yeh, T. Wang, J. Ku, C.-Y. Lu, Macronix International Co. Ltd., Hsin-Chu, Taiwan

A novel trapping-nitride-based non-volatile memory cell by using a gated-diode structure is proposed. Fowler-Nordheim electron injection and band-to-band-tunneling induced hot-hole injection are utilized as the erase and program methods, respectively. BTBT current modulated by the trapped charges is the sensing signal to distinguish the cell's bit state. This cell structure overcomes the channel-length related drawbacks in convention field-effect-transistor-based cells. Furthermore, its array architecture and bias methods can relieve the complex word-line bias schemes and program-inhibit techniques used in NAND-type arrays. Good program/erase characteristics and reliability are also presented.

6.3 – 4:15 p.m.
Very Low Voltage SiO_2/HfON/HfAlO/TaN Memory with Fast Speed and Good Retention, C.H. Lai, A. Chin, H.L. Kao, K.M. Chen, M. Hong*, J. Kwo*, C.C. Chi*, National Chiao-Tung University, Hsinchu, Taiwan, *National Tsing Hua University, Hsinchu, Taiwan

At 85 C under very low ±8V and fast 100us P/E, good memory device integrity of 2.5V initial Vth window and 1.45V 10-year extrapolated retention are obtained. This was achieved in SiO_2/HfON/HfAlO/TaN MONOS using very high-k (~22) and deep trapping HfON, which further gives good 1.0V 10-year memory window even at 125 C.

6.4 – 4:40 p.m.
A Highly Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory, E.-K. Lai, H.-T. Lue, Y.-H. Hsiao, J.-Y. Hsieh, S.-C. Lee, C.-P. Lu, S.-Y. Wang, L.-W. Yang, K.-C. Chen, J. Gong*, K.-Y. Hsieh, J. Ku, R. Liu, C.-Y. Lu, Macronix International Co. Ltd., Hsinchu, Taiwan, *National Tsing Hua University, Hsinchu, Taiwan

For the first time, a successful TFT NAND-type Flash memory is demonstrated using a low thermal budget process suitable for stacking the memories. A TFT-SONOS device using bandgap engineered SONOS (BE-SONOS) [1] with fully-depleted (FD) poly silicon (50 nm) channel and tri-gate P+-poly gate is integrated into a NAND array. Small devices (L/W=0.18/0.09 μm) with good DC performance are achieved, owing to the good control capability of the tri-gate FD structure. Successful NAND array functions are demonstrated, with more than 1 μA read current for a 16-string NAND array and good program disturb immunity. This new device also shows good endurance and data retention, and negligible read disturb. These results are very encouraging for future 3D Flash memory.

6.5 – 5:05 p.m.
A Novel Multi-Functional Silicon-On-ONO (SOONO) MOSFETs for SoC Applications : Electrical Characterization for High Performance Transistor and Embedded Memory Applications, C.W. Oh, S.H. Kim, N.Y. Kim, Y.L. Choi, Y.S. Lee, W.J. Jang, H.S. Lee, H.S. Park, D.-W. Kim, D. Park, B.-I. Ryu, Samsung Electronics Co., Kyungki-Do, Korea

We proposed and successfully demonstrate multi-functional Si-on-ONO (SOONO) MOSFETs. As a high performance transistor and embedded 2-bit flash memory, they show the reasonable characteristics. SOONO MOSFETs act as ultra thin body transistor with self-limited shallow junction, resulting in good SCE immunity and high driving currents, 737uA/μm for nMOS and 330uA/μm for pMOS at lVGSl=lVDSl=1V, IOFF=100nA/μm). In terms of flash memory, SOONO MOSFET acts as 2-bit flash memory with 2 physically separated storage node in back side. By using CHEI/HHI program/erase, each node was easily programmed and erased. In the gate length of 120nm, we achieved the read/write margins of ~1.3 V at VDS=1.2V and the VTH shifts of ~2.5V for both program/erase.