SESSION 7 – TAPA II
Multi-Gate FETs

Tuesday, June 13, 3:25 p.m.
Chairpersons: T.-J. King Liu, Synopsys, Inc.
M. Masahara, AIST

7.1 – 3:25 p.m.
Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering, J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, R. Chau, Intel Corporation, Hillsboro, OR

We have combined the benefits of the fully depleted TriGate transistor architecture with high-k gate dielectrics, metal gate electrodes and strain engineering. High performance NMOS and PMOS trigate transistors are demonstrated with IDSAT=1.4mA/um and 1.1mA/um respectively (IOFF=100nA/um, VCC=1.1V and LG=40nm) with excellent short channel effects (SCE) – DIBL and subthreshold swing, delta-S. The contributions of strain, the <100> vs. <110> substrate orientations, high-k gate dielectrics, and low channel doping are investigated for a variety of channel dimensions and FIN profiles. We observe no evidence of early parasitic corner transistor turn-on in the current devices which can potentially degrade ION-IOFF and delta-S.

7.2 – 3:50 p.m.
Performance Enhancement of MUGFET Devices Using Super Critical Strained–SOI (SC-SSOI)and CESL, N. Collaert, R. Rooyackers, F. Clemente, P. Zimmerman, I. Cayrefourcq*, B. Ghyselen*, K.T. San^, B. Eyckens, M. Jurczak, S. Biesemans, IMEC, Leuven, Belgium, *SOITEC, Crolles Cedex, France, ^Texas Instruments Inc., Dallas, TX

This paper describes the performance of nMOS and pMOS tall triple gate (MUGFET) devices with fin widths down to 20 nm fabricated for the first time on Super Critical Strained Si On Insulator (SC-SSOI). The electrical and μRaman measurements show that the tensile strain can be maintained in SSOI substrates even for fins as narrow as 20nm giving 80% and 10% drive current increase in long and short channel nMOS devices, respectively. Additionally, the introduction of tensile Contact Etch Stop Layers (CESL) improves the nMOS drive current by as much as 35% for short channel devices.

7.3 – 4:15 p.m.
Investigation of FinFET Devices for 32nm Technologies and Beyond, H. Shang, L. Chang, X. Wang, M. Rooks, Y. Zhang, B. To, K. Babich, G. Totir, Y. Sun, E. Kiewra, M. Ieong, W. Haensch, IBM Semiconductor Research and Development Center, Yorktown Heights, NY

FinFET devices are demonstrated with multiple fins (>2) at a 120nm pitch using e-beam lithography to address some key challenges of FINFETs for 32nm node technologies and beyond. Target Vt's are achieved by proper halo design using 20nm fins. Vt scatter due to Fin width variation is greatly reduced with a reduced halo. When such a realistic fin pitch is used, S/D contact formation becomes a serious challenge due to poly-to-active overlay requirements and the need for raised S/D for series resis-tance reduction. A new FinFET design without S/D contact pads is thus proposed and a selective epitaxial process to merge indi-vidual fins is developed.

7.4 – 4:40 p.m.
Strained N-Channel FinFETs with 25 nm Gate Length and Silicon-Carbon Source/Drain Regions for Performance Enhancement, T.-Y. Liow[1,2], K.-M. Tan[1], R. T. P. Lee[1], A. Du[2], C.-H. Tung[2], G. S. Samudra[1], W.-J. Yoo[1], N. Balasubramanian[2], Y.-C. Yeo[1], [1]National University of Singapore, Singapore, [2]Institute of Microelectronics, Singapore

We report the demonstration of 25 nm gate length LG tri-gate FinFETs with Si0.99C0.01 source and drain (S/D) regions. The strain-induced mobility enhancement due to the Si0.99C0.01 S/D leads to a drive current IDsat improvement of 20% at a fixed off-state current Ioff of 1×10-7 A/um. With additional channel strain engineering, FinFETs incorporating Si0.99C0.01 S/D and a tensile-stress silicon nitride (SiN) capping etch-stop layer (ESL) achieve an IDsat enhancement of 56%.

7.5 – 5:05 p.m.
Sub-5nm All-Around Gate FinFET for Ultimate Scaling, H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S.C. Jeon*, G.S. Lee*, J.S. Oh*, Y.C. Park*, W.H. Bae*, H.M. Lee*, J.M. Yang*, J.J. Yoo*, S.I. Kim*, Y.-K. Choi, Korea Advanced Institute of Science and Technology, Daejeon, Korea, *Korean National Nanofab Center, Daejeon, Korea

Sub-5nm all-around gate FinFETs with 3nm fin width were fabricated for the first time. The n-channel FinFET of sub-5nm with 1.4nm HfO_2 shows an IDsat of 497A/μm at VG=VD=1.0V. Characteristics of sub-5nm transistor are verified by using 3-D simulations as well as analytical models. A threshold voltage increases as the fin width reduces by quantum confinement effects. The threshold voltage shift was fitted to a theoretical model with consideration of the first-order perturbation theory. And a channel orientation effect, based on a current-flow direction, is shown.