Session 1 – TAPA 1/2/3
Joint Plenary Session
Tuesday, June 19, 8:10 a.m.

8:05 a.m. **Joint Welcome and Opening Remarks**
Mukesh Khare, IBM
Gunther Lehmann, Infineon

Technology Plenary

T1.1 – 8:40 a.m.
Memory Technology: The Core to Enable Future Computing Systems, Scott J. DeBoer, Micron Technology, Inc.

9:20 a.m. **EDS Remarks, Fellows Recognition**
Fernando Guarin, EDS President
Mukesh Khare, Technology General Chair

T1.2: 9:30 a.m.
Revolutionizing Cancer Genomic Medicine by AI and Supercomputer with Big Data, Satoru Miyano, University of Tokyo

10:10 a.m. **Break**

Circuits Plenary

10:30 a.m. **Best Student Paper Awards and IEEE Awards**
Gunther Lehmann, Infineon
Mukesh Khare, IBM

C1.1 - 10:40 a.m.
Hardware-Enabled Artificial Intelligence, Bill Dally, Nvidia

11:20 a.m. **2019 Joint Announcement**
Makoto Ikeda, University of Tokyo
Meishoku Masahara, AIST

C1.2 - 11:30 a.m.
Semiconductor Technologies Accelerate Our Future Vision: "ANSHIN Platform", Tsuneo Komatsuzaki, SECOM

Session 2 - TAPA 1
SRAM Designs
Tuesday, June 19, 1:30 p.m.

Co-Chairs: A. Loke, Qualcomm
J. Chang, TSMC

C2-1 - 1:30 p.m.
A 290mV Ultra-Low Voltage One-Port SRAM Compiler Design Using a 12T Write Contention and Read Upset Free Bit-Cell in 7nm FinFET Technology, M. E. Sinangil, Y.-T. Lin, H.J. Liao, J. Chang, TSMC

C2-2 - 1:55 p.m.
A 7nm Double-Pumped 6R6W Register File for Machine Learning Memory, H. Nguyen, J. Jeong, F. Atallah, M. Jansen, A. Polomik, D. Yingling, H. Akkaraju, B. Appel, R. Nadkarni, K. Bowman, Qualcom Technologies Inc.

C2-3 - 2:20 p.m.

Half-and-Half Compare Content Addressable Memory with Charge-Sharing based Selective Match-Line Precharge Scheme, W. Choi, H. Kim*, C. Park*, T. Song*, J. Park,Korea University, *Samsung Electronics

C2-4 - 2:45 p.m.
12-nm Fin-FET 3.0G-search/s 80-bit x 128-Entry Dual-port Ternary CAM, Makoto Yabuuchi, Masao Morimoto, Koji Nii, and Shinji Tanaka, Renesas Electronics Corporation

Session 3 - Honolulu
Wireless Systems
Tuesday, June 19, 1:30 p.m.

Co-Chairs: A. Zolfaghari, Broadcom
H. Song, POSTECH

C3-1 - 1:30 p.m.
A Dual-Mode Configurable RF-to-Digital Receiver in 16nm FinFET, A. Whitcombe, F. Sheikh*, E. Alpman*, A. Ravi*, B. Nikolic, UC Berkeley, *Intel Corporation

C3-2 - 1:55 p.m.
An 113dB-Link-Budget Bluetooth-5 SoC with an 8dBm 22%-Efficiency TX, T. Wang, Y. Ogasawara, Y. Tuda, T. Ta*, M. Oshiro, J. Ihara, T. Maruyama, T. Hashimoto, A. Sai*, Takashi Tokairin,Toshiba Electronic Devices & Storage Corporation, *Toshiba Corporation

C3-3 - 2:20 p.m.
Fully Integrated OOK-powered Pad-less Deep Sub-wavelength-sized 5-GHz RFID With on-chip Antenna Using Adiabatic Logic in 0.18µm CMOS, Y. Toeda, T. Fujimaki, M. Hamada, T. Kuroda, Keio University

C3-4 - 2:45 p.m.
A Fast Triple-Interferer Sensor (Detector and Digital Encoder) with In-Situ Reference Frequency Acquisition at 2.7-to-3.7GHz in 0.13µm CMOS, D. Shin,* K.-J. Koh*, Virginia Tech, *Intel Corp, also with Intel

Session 4 - TAPA 1
Machine Learning Processors
Tuesday, June 19, 3:25 p.m.

Co-Chairs: D. Sylvester, University of Michigan
M. Hashimoto, Osaka University

C4-1 - 3:25 p.m.
STICKER: A 0.41-62.1 TOPS/W 8bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers, Z. Yuan, J. Yue, H. Yang, Z. Wang, J. Li, Y. Yang, Q. Guo, X. Li, M.-F. Chang*, H. Yang ,Y. Liu,Tsinghua University, *National Tsing Hua University

C4-2 - 3:50 p.m.
A Scalable Multi-TeraOPS Deep Learning Processor Core for AI Training and Inference, B. Fleischer, S. Shukla, M. Ziegler, J. Silberman, J. Oh, V. Srinivasan, J. Choi, S. Mueller, A. Agrawal, T. Babinsky, N. Cao, C.-Y. Chen, P. Chuang, T. Fox, G. Gristede, M. Guillorn, H. Haynie, M. Klaiber, D. Lee, S.Lo, G. Maier, M. Scheuermann, S. Venkataramani, C. Vezyrtzis, N. Wang, F. Yee, C. Zhou, P.-F. Lu, B. Curran, L. Chang, K. Gopalakrishnan, IBM TJ Watson Research Center,

C4-3 - 4:15 p.m.
An Ultra-high Energy-efficient reconfigurable Processor for Deep Neural Networks with Binary/Ternary Weights in 28nm CMOS, S. Yin, P. Ouyang*, J. Yang, T. Lu, X. Li, L. Liu, S. Wei, Tsinghua University, *Beihang University

C4-4 - 4:40 p.m.

2.9TOPS/W Reconfigurable Dense/Sparse Matrix-Multiply Accelerator with Unified INT8/INT16/FP16 Datapath in 14nm Tri-gate CMOS, M. Anders, H. Kaul, S. Mathew, V. Suresh, S. Satpathy, A. Agarwal, S. Hsu, R. Krishnamurthy, Intel Corporation

C4-5 - 5:05 p.m.
New Generation Dynamically Reconfigurable Processor Technology for Accelerating Embedded AI Applications (Invited), T. Fujii, T. Toi, T. Tanaka, K. Togawa, T. Kitaoka, K. Nishino, N. Nakamura, H. Nakahara*, and M. Motomura** Renesas Electronics Corporation, *Tokyo Institute of Technology, **Hokkaido University

Session 5 - HONOLULU SUITE
Extreme Wireline Transceivers
Tuesday, June 19, 3:25 p.m.

Co-Chairs: J. Proesel, IBM
J. Lee, National Taiwan University

C5-1 - 3:25 p.m.
A 112-Gb/s PAM4 Transmitter in 16nm FinFET, K. Tan, P.-C. Chiang, Y. Wang, H. Zhao, A. Roldan, H. Zhao, N. Narang, S. Lim, D. Carey, S. Ambatipudi, P. Upadhyaya, Y. Frans, K. Chang, Xilinx

C5-2 - 3:50 p.m.
112Gb/s PAM4 Wireline Receiver using a 64-way Time-Interleaved SAR ADC in 16nm FinFET, J. Hudner, D. Carey, R. Casey ,K. Hearne, P. Neto, I. Chlis, M. Erett, C. Poon, A. Laraba, H. Zhang, S. Ambatipudi, D. Mahashin, P. Upadhyaya, Y. Frans, K. Chang. Xilinx Incorporated

C5-3 – 4:15 p.m.
An Active Copper-Cable Supporting 56-Gbit/s PAM4 and 28-Gbit/s NRZ with Continuous Time Linear Equalizer IC for 10-meters Reach Interconnection (Invited), K. Maeda, T. Norimatsu, K. Kogo, N. Kohmu, K. Nishimura* and I. Fukasaku* Hitachi, Ltd. Research and Development Group, *Hitachi Metals, Ltd. Cable Materials Company

C5-4 - 4:40 p.m.
A 64 Gb/s 1.5 pJ/bit PAM-4 Transmitter with 3-Tap FFE and Gm-Regulated Active-Feedback Driver in 28 nm CMOS, H. Ju, M-C. Choi, G-S. Jeong, D-K. Jeong, Seoul National University

C5-5 - 5:05 p.m.
A 0.3pJ/bit 112Gb/s PAM4 1+0.5D TX-DFE Precoder and 8-tap FFE in 14nm CMOS, T. Toifl, C. Menolfi, M. Braendli, A. Cevrero, P.A. Francese, M. Kossel, L. Kull, D. Luu*, T. Morf, I. Oezkaya, IBM, *ETH Zurich and IBM

Session 6 - TAPA 1
Adaptive and Application Specific Digital Circuits
Wedesday, June 20, 8:10 a.m.

Co-Chairs: E. Beigne, CEA LETI
M. Yamaoka, Hitachi, Ltd.

C6-1 - 8:10 a.m.
Memory Expansion Technology for Large-Scale Data Processing Using Software-Controlled SSD (Invited), E. Yoshida, S. Kazama, S. Kuwamura, S. Gokita, T. Miyoshi, Y. Noguchi, and Y. Honda*, Fujitsu Laboratories Ltd., *Fujitsu Ltd.

C6-2 - 8:35 a.m.
An Out-of-Order RISC-V Processor with Resilient Low-Voltage Operation in 28 nm CMOS, P.-F. Chiu, C. Celio, K. Asanovic, D. Patterson, B. Nikolic, University of California, Berkeley

C6-3 - 9:00 a.m.

An Adaptive Body-Biasing SoC Using *in situ* Slack Monitoring for Runtime Replica Calibration, M. Saligane, J. Lee, Qing Dong, M. Yasuda*, K. Kumeno*, F. Ohno*, S. Miyoshi**, M. Kawaminami*/**, D. Blaauw, D. Sylvester, University of Michigan, *Mie Fujitsu Semiconductor Limited, **Fujitsu Semiconductor Electronics, Inc.

C6-4 - 9:25 a.m.
An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor, F. Rahman, S. Kim, N. John, R. Kumar, R. Pamula, K. Bowman*, Visvesh Sathe University of Washington, *Qualcomm Technologies Inc.

Session 7 - HONOLULU SUITE
Time-of-Flight and Advanced Image Sensors
Wednesday, June 20, 8:10 a.m.

Co-Chairs: H. Lee, Google
Y. Oike, Sony Semiconductor Solutions Corp.

C7-1 - 8:10 a.m.
A 252 × 144 SPAD Pixel FLASH LiDAR with 1728 Dual-clock 48.8 ps TDCs, Integrated Histogramming and 14.9-to-1 Compression in 180nm CMOS Technology, S. Lindner, C. Zhang*, I. Antolovic*, M. Wolf**, E. Charbon***, EPFL/University of Zurich, *TUDelft, **University of Zurich, ***EPFL/TUDelft

C7-2 - 8:35 a.m.
A 220 m-Range Direct Time-of-Flight 688 × 384 CMOS Image Sensor with Sub-Photon Signal Extraction (SPSE) Pixels Using Vertical Avalanche Photo-Diodes and 6 kHz Light Pulse Counters, S, Koyama, M. Ishii, S. Saito, M. Takemoto, Y. Nose, A. Inoue, Y. Sakata, Y. Sugiura, M. Usuda, T. Kabe, S. Kasuga, M. Mori, Y. Hirose, A. Odagawa, T. Tanaka, Panasonic Corporation

C7-3 - 9:00 a.m.
Multipurpose, Fully-Integrated 128x128 Event-Driven MD-SiPM with 512 16-bit TDCs with 45 ps LSB and 20 ns Gating, A. Carimatto, A. Ulku, S. Lindner*, E. D'Aillon, S. Pellegrini**, B. Rae**, E. Charbon*, TU Delft, *EPFL, **ST Microelectronics

C7-4 - 9:25 a.m.
A Two-Tap NIR Lock-In Pixel CMOS Image Sensor with Background Light Cancelling Capability for Non-Contact Heart Rate Detection, C. Cao, Y. Shirakawa, L. Tan, M. W. Seo, K. Kagawa, K. Yasutomi, T. Kosugi*, S. Aoyama*, N. Teranishi, N. Tsumura**, S. Kawahito, Shizuoka University, *Brookman Technology, **Chiba University

Session 8 - TAPA 1
Joint Focus Session: Emerging Memory
Wednesday, June 20, 10:05 a.m.

Co-Chairs: E. Wang, Intel Corp.
N. Lu, Etron Technology, Inc.

C8-1 - 10:05 a.m.
Logic Process Compatible 40nm 16Mb, Embedded Perpendicular-MRAM with Hybrid-Resistance Reference, sub-µA Sensing Resolution, and 17.5nS Read Access Time, Y.-C. Shih, C.-F. Lee, Y.-A. Chang, P.-H. Lee, H.-J. Lin, Y.-L. Chen, K.-F. Lin, T.-C. Yeh, H.-C. Yu, H. Chuang, Y.-D. Chih, J. Chang, TMSC

C8-2 - 10:30 a.m.
SOT-MRAM 300mm Integration for Low Power and Ultrafast Embedded Memories, K. Garello, F. Yasin, S. Couet, L. Souriau, J. Swerts, S. Rao, S. Van Beek, W. Kim, E. Liu, S. Kundu, D. Tsvetanova, N. Jossart, K. Croes, E. Grimaldi*, M. Baumgartner*, D. Crotti, A. Furnémont, P. Gambardella*, G. S. Kar, imec, *ETHC

C8-3 - 10:55 a.m.

High-speed Voltage Control Spintronics Memory (VoCSM) Having Broad Design Windows, N. Shimomura, H. Yoda, T. Inokuchi, K. Koi, H. Sugiyama, Y. Kato, Y.Ohsawa, A. Buyandalai, S. Shirotori, S. Oikawa, M. Shimizu, M. Ishikawa, T. Ajay, and A. Kurobe, Toshiba Corp.

C8-4 - 11:20 a.m.
Energy Efficient Adiabatic FRAM with 0.99 pJ/bit Write for IoT Applications, S. Jeloka, Z. Wang, R. Xie**, S. Khanna***, S. Bartling***, D. Sylvester, D. Blaauw, University of Michigan, *ARM, **AMD, ***Texas Instruments

C8-5 - 11:45 a.m.
14nm FinFET 1.5Mb Embedded High-K Charge Trap Transistor One Time Programmable Memory Using Dynamic Adaptive Programming, E. Hunt-Schroeder, D. Anand, J. Fifield, M. Jacunski, M. Roberge, D. Pontius, K. Batson, T. Kirihata, GLOBALFOUNDRIES

Session 9 - HONOLULU SUITE
Nyquist ADC
Wednesday, June 20, 10:05 a.m.

Co-Chairs: R. Kapusta, Analog Devices
C. Liu, MediaTek, Inc.

C9-1 - 10:05 a.m.
A 12-bit 31.1uW 1MS/s SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4dB SFDR using 256fF Sampling Capacitance, J. Shen, A. Shikata, A. Liu, F. Chalifoux, Analog Devices

C9-2 - 10:30 a.m.
A 0.5-1.1V 10b Adaptive Bypassing SAR ADC Utilizing Oscillation Cycle Information of VCO-based Comparator, Z. Ding, X. Zhou, Q. Li, University of Electronic Science and Technology of China

C9-3 - 10:55 a.m.
A 2.3-mW, 950-MHz, 8-bit Fully-Time-Based Subranging ADC Using Highly-Linear Dynamic VTC, K. Ohhata, Kagoshima University

C9-4 - 11:20 a.m.
A >3GHz ERBW 1.1-GS/s 8-bit Two-Step SAR ADC with Recursive-Weight DAC, H. Chen, X. Zhou, Q. Yu, F. Zhang, Q. Li, University of Electronic Science and Technology of China

C9-5 - 11:45 a.m.
A 13bit 5GS/s ADC with time-interleaved chopping calibration in 16nm FinFET, B. Vaz, B. Verbruggen, C. Erdmann, D. Collins, J. Mcgrath, A. Boumaalif, E. Cullen, D. Walsh, A. Morgado, C. Mesadri, B. Long, R. Pathepuram, R. De La Torre, A. Manlapat, G. Karyotis, D. Tsaliagos, P. Lynch, P. Lim, D. Breathnach and B. Farley, Xilinx

Session 10 - TAPA 1
Joint Focus Session: Power Devices and Circuits
Wednesday, June 20, 1:30 p.m.

Co-Chairs: Y. Ramadass, Texas Instruments
P. Yue, Hong Kong University of Science and Technology

C10-1 - 1:30 p.m.
A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-to-2.22V Output and 93% Peak-Efficiency, N. Butzen, M. Steyaert, KU Leuven

C10-2 - 1:55 p.m.
New Methodology for Evaluating Minority Carrier Lifetime for Process Assessment, K. Kakushima, T. Hoshii, M. Watanabe, N. Shigyo, K. Furukawa, T. Saraya*, T. Takakura*, K. Itou*, M. Fukui*, S. Suzuki*, K. Takeuchi*, I. Muneta, H.

Wakabayashi, Y. Numasawa**, A. Ogura**, S. Nishizawa***, K. Tsutsui, T. Hiramoto**, H. Ohashi, and H. Iwai, Tokoyo Institute of Technology, *The University of Tokoyo, **Meiji University, ***Kyushu University

C10-3 - 2:20 p.m.
A Quasi-Digital Ultra-Fast Capacitor-less Low-Dropout Regulator Based on Comparator Control for x8 Current Spike of PCRAM systems, Sung-Won Choi, Yeunhee Huh, Sang-Hui Park, Kye-Seok Yoon, Jun-Suk Bang, Se-Un Shin, Yong-Min Ju, Yujin Yang, Junghyuk Yoon*, Changyong Ahn*, Taekseung Kim*, Sung-Wan Hong **, Gyu-Hyeong Cho, KAIST, *SK Hynix Semiconductor, **Sookmyung Women's University

C10-4 - 2:45 p.m.
0.5V-V_{IN}, 165-mA/mm^2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control, D. Kim, S. Kim, H. Ham*, J. Kim*, M. Seok, Columbia University, *SK Hynix

Session 11 - HONOLULU 1
Frequency References
Wednesday, June 20, 1:30 p.m.

Co-Chairs: C. Sander, Infineon
Y. Bando, Socionext, Inc.

C11-1 - 1:30 p.m.
A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with Sub-ppb Long-Term Stability and 66-mW DC Power, C. Wang, X. Yi, M. Kim, Y. Zhang, R. Han, Massachuetts Institute of Technology

C11-2 - 1:55 p.m.
A 64µs Start-Up 26/40MHz Crystal Oscillator with Negative Resistance Boosting Technique Using Reconfigurable Multi-Stage Amplifier, M. Miyahara, Y. Endo*, K. Okad**, A. Matsuzawa*., High Energy Accelerator Research Organization, *Tokyo Institute of Technology

C11-3 - 2:20 p.m.
A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation, J. Lim, T. Jang, M. Saligane, M. Yasuda*, S. Miyoshi**, M. Kawaminami, D. Blaauw, D. Sylvester, University of Michigan, *Mie Fujitsu Semiconductor Limited, **Fujitsu Electronics America

C11-4 - 2:45 p.m.
A Sub-Leakage pW-Power Hz-Range Relaxation Oscillator Operating with 0.3V-1.8V Unregulated Supply, O. Aiello, P. Crovetti*, M. Alioto, National University of Singapore, *Politecnico di Torino

Session 12 - HONOLULU 2
Bio-Medical Interfaces
Wednesday, June 20, 1:30 p.m.

Co-Chairs: D. Markovic, University of California, Los Angeles
T. Tokuda, Nara Institute of Science and Technology

C12-1 - 1:30 p.m.
A 0.8V 82.9µW In-Ear BCI Controller System with 8.8 PEF EEG Instrumentational Amplifier and Wireless BAN Transceiver, J. Lee, K.-R. Lee, U. Ha*, J.-H. Kim, K. Lee, H.-J. Woo, KAIST, *MIT Media Lab

C12-2 - 1:55 p.m.
A Battery-Powered Opto-Electrophysiology Neural Interface with Artifact-Preventing Optical Pulse Shaping, A. Mendrela, S.-Y. Park, M. Vöröslakos, M. Flynn, and E. Yoon, University of Michigan

C12-3 - 2:20 p.m.

Artifact-Tolerant Opamp-less Delta-Modulated Bidirectional Neuro-Interface, M. R. Pazhouhandeh, H. Kassiri, A. Shoukry, I. Wesspapir*, P. Carlen*, R. Genov, University of Toronto, *Toronto Western Hospital

C12-4 - 2:45 p.m.
A 400GΩ Input-impedance, 220mV$_{pp}$ Linear-input-range, 2.8V$_{pp}$ CM-interference-tolerant active electrode for Non-contact Capacitively Coupled ECG acquisition, Mingyi Chen, Ivan Dario Castro, Qiuyang Lin,Tom Torfs, Filip Tavernier*, Chris Van Hoof,Nick Van Helleputte, imec ,*KU Leuven

Session 13 - TAPA 1
Robotics and Machine Learning applications
Wednesday, June 20, 3:25 p.m.

Co-Chairs: B. Nikolic, University of California, Berkeley
K. Sohn, Samsung Electronics Co., Ltd.

C13-1 - 3:25 p.m.
Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones, A. Suleiman, Z. Zhang, L. Carlone, S. Karman, V. Sze, Massachusetts Institute of Technology

C13-2 - 3:50 p.m.
A 1920 × 1080 25fps, 2.4TOPS/W Unified Optical Flow and Depth 6D Vision Processor for Energy-Efficient, Low Power Autonomous Navigation, Ziyun Li, Jingcheng Wang, Dennis Sylvester, David Blaauw, and Hun-Seok Kim, University of Michigan

C13-3 - 4:15 p.m.
B-Face: 0.2 mW CNN-Based Face Recognition Processor with Face Alignment for Mobile User Identification, S. Kang, J. Lee, C. Kim, H. Yoo, KAIST

C13-4 - 4:40 p.m.
A 141 uW, 2.46 pJ/Neuron Binarized Convolutional Neural Network based Self-learning Speech Recognition Processor in 28nm CMOS, Shouyi Yin, Peng Ouyang*, Shixuan Zheng, Dandan Song, Xiudong Li, Leibo Liu, Shaojun Wei, Tsinghua University, *Beihang University

C13-5 - 5:05 p.m.
A Mixed-Signal Binarized Convolutional-Neural-Network Accelerator Integrating Dense Weight Storage and Multiplication for Reduced Data Movement, H. Valavi, P. Ramadge, E.Nestler*, and N. Verma, Princeton University, *Analog Devices Inc.

Session 14 - HONOLULU 1
Advanced Wireline and Memory Interfaces
Wednesday, June 20, 3:25 p.m.

Co-Chairs: E. Naviasky, Cadence
Y. Takai, Micron Memory Japan

C14-1 - 3:25 p.m.
A 0.5-28Gb/s Wireline Tranceiver with 15-Tap DFE and Fast-Locking Digital CDR in 7nm FinFET, J. Im, S. Chen, D. Freitas, A. Chou, L. Zhou, I. Zhuang, T. Cronin, D. Mahashin, W. Lin, K. L. Chan, H. Zhao, K. H. Tan, A. Bekele, D. Turker, P. Upadhyaya, Y. Frans, K. Chang, Xilinx Inc.

C14-2 - 3:50 p.m.
A sub-0.85V, 6.4Gbp/s/pin TX-Interleaved Transceiver with Fast Wake-up Time using 2-Step Charging Control and V$_{OH}$ Calibration in 20nm DRAM Process, J.-H.Baek, C.-K. Lee, K. Kim, D.-S. Moon, G.-H. Cha, J.-S. Heo, M. Ahn, D.-J. Kim, J.-J. Song, S. Kwon, J. Kim, K.-S.oo Kim, J. Ahn, J.-S. Nam, B. Kim, J.-H. Cho, J.-H. Oh, S.-J. Bae, I. Song, S.-H. Hyun, I. Kim, H.-J. Kwon, Y.-S. Sohn, J.-H. Choi, K.-I. Park, S.-J. Jang, Samsung Electronics

C14-3 - 4:15 p.m.
A 12.8 Gb/s Daisy Chain-Based Downlink I/F Employing Spectrally Compressed Multi-Band Multiplexing for High-Bandwidth and Large-Capacity Storage Systems, Y. Tsubouchi, D. Miyashita, Y. Satoh, T. Toi, F. Tachibana, M. Morimoto, J. Wadatsumi, J. Deguchi, Toshiba Memory Corporation

C14-4 - 4:40 p.m.
A Digital-Intensive 2-to-9.2 Gb/s/pin Memory Controller I/O with Fast-Response LDO in 10nm CMOS, R. Inti, M. Mansuri, J. Kennedy, H. Venkatram, C.-M. Hsu, A. Martin, J. Jaussi, B. Casper, Intel Corporation

C14-5 - 5:05 p.m.
An Automated SerDes Frontend Generator Verified with a 16nm Instance Achieving 15 Gb/s at 1.96 pJ/bit, E. Chang, N. Narevsky, J. Han, E. Alon, University of California, Berkeley

Session 15 - HONOLULU 2
Capacitive Sensor Interfaces
Wednesday, June 20, 3:25 p.m.

Co-Chairs: K. Makinwa, Delft University of Technology
Y. Xu, National University of Singapore

C15-1 - 3:25 p.m.
A 114-aF_{rms}-Resolution 46-nF/10-MΩ-Range Digital-Intensive Reconfigurable RC-to-Digital Converter with Parasitic-Insensitive Femto-Farad Baseline Sensing, A. George, W. Shim, M. Je* and J. Lee, DGIST, *KAIST

C15-2 - 3:50 p.m.
A 117dB In-band CMRR 98.5dB SNR Capacitance-to-Digital Converter for Sub-nm Displacement Sensing with an Electrically Floating Target, H. Jiang, S. Amani, J. Vogel, S. Shalmany, and S. Nihtianov, Delft University of Technology

C15-3 - 4:15 p.m.
A 181nW 970μg/√Hz Accelerometer Analog Front-End Employing Feedforward Noise Reduction Technique, I. Akita, T. Okazawa, Y. Kurui*, A. Fujimoto*, T. Asano, Toyohashi University of Technology, *Toshiba Corporation

C15-4 - 4:40 p.m.
A 2.69μW Dual Quantization-based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18μm CMOS, S.Park, G.H.Lee, S.H.Cho, KAIST

C15-5 - 5:05 p.m.
An 8.2 μW 0.14 mm^2 16-Channel CDMA-Like Period Modulation Capacitance-to-Digital Converter with Reduced Data Throughput, Yuxuan Luo, Chun-Huat Heng, National University of Singapore

Session 16 - TAPA 1
Hardware Security
Thursday, June 21, 8:10 a.m.

Co-Chairs: B. Calhoun, University of Virginia
N. Miura, Kobe University

C16-1 - 8:10 a.m.
An All-Digital Unified Static/Dynamic Entropy Generator Featuring Self-Calibrating Hierarchical Von Neumann Extraction for Secure Privacy-Preserving Mutual Authentication in IoT Mote Platforms, S. Satpathy, S. Mathew, V. Suresh, M. Anders, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, V. De, Intel Corporation

C16-2 - 8:35 a.m.

A 28nm Integrated True Random Number Generator Harvesting Entropy from MRAM, K. Yang, Q. Dong, Z. Wang, Y.-C. Shih*, Y.-D. Chih*, J. Chang*, D. Blaauw, D. Sylvester, University of Michigan, *TSMC

C16-3 - 9:00 a.m.
An All-Digital True-Random-Number Generator with Integrated De-correlation and Bias-Correction at 3.2-to-86 Mb/s, 2.58 pJ/bit in 65 nm CMOS, V. Rajesh Pamula, Xun Sun, Sung Kim, Fahim ur Rahman, Baosen Zhang and Visvesh Sathe, University of Washington

C16-4 - 9:25 a.m.
220mV-900mV 794/584/754 Gbps/W Reconfigurable GF$(2^4)^2$ AES/SMS4/Camellia Symmetric-Key Cipher Accelerator in 14nm Tri-gate CMOS, S. Satpathy, V. Suresh, S. Mathew, M. Anders, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, Intel Corporation

Session 17 - HONOLULU 1
Advanced PLLs
Thursday, June 21, 8:10 a.m.

Co-Chairs: E. Jassen, NXP Semiconductors
K. Agawa, Toshiba Corp.

C17-1 - 8:10 a.m.
A Digital Bang-Bang Phase-Locked Loop with Background Injection Timing Calibration and Automatic Loop Gain Control in 7nm FinFET CMOS, T.-K. Kuan, C.-Y. Wu, R.-P. Shen, C.-H. Chang, K. Hsieh, M. Chen, Taiwan Semiconductor Manufacturing Company

C17-2 - 8:35 a.m.
AMASS PLL: An Active-Mixer-Adopted Sub-Sampling PLL Achieving an FOM of -255.5dB and a Reference Spur of -66.5dBc, D. Lee, P. Mercier, University of California, San Diego

C17-3 - 9:00 a.m.
A 0.2GHz to 4GHz Hybrid PLL (ADPLL/Charge-Pump-PLL) in 7nm FinFET CMOS Featuring 0.619ps Integrated Jitter and 0.6us Settling Time at 2.3mW, T.-H. Tsai, R.-B. Sheen, C.-H. Chang, R. Staszewski*, Taiwan Semiconductor Manufacturing Company, *University College Dublin

C17-4 - 9:25 a.m.
153 fs_{RMS}-Integrated-Jitter and 114-Multiplication Factor PVT-Robust 22.8 GHz Ring-*LC*-Hybrid Injection-Locked Clock Multiplier, S. Choi, S. Yoo, Y. Lee, Y. Jo, J. Lee, Y. Lim, J. Choi, Ulsan National Institute of Science and Technology

Session 18 - HONOLULU 2
Wireless for Biomedical and IoT
Thursday, June 21, 8:10 a.m.

Co-Chairs: C. Lopez, imec
T. Nezuka, Denso Corp.

C18-1 - 8:10 a.m.
A Wireless Implantable Ultrasound Array Receiver for Thermoacoustic Imaging, A. Sawaby, M. L. Wang, E. So, J.-C. Chien, H. Nan, B. T. Khuri-Yakub, A. Arbabian, Stanford University

C18-2 - 8:35 a.m.
A 0.04mm^3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement, X. Wu, I. Lee, Q. Dong, K. Yang, D. Kim, J. Wang, Y. Peng, Y. Zhang, M. Saligane, M. Yasuda*, K. Kumeno*, F. Ohno*, S. Miyoshi**, M. Kawaminami*, D. Sylvester & D. Blaauw
1University of Michigan, *Mie Fujitsu Semiconductor Limited, **Fujitsu Electronics America, Inc.

C18-3 - 9:00 a.m.
Self-Regulated Wireless Power and Simultaneous 5 Mb/s Reverse Data over One Pair of Coils, J. Pan, A. A. Abidi, W. Jiang, D. Rozgic, D. Markovic, University of California, Los Angeles

C18-4 - 9:25 a.m.
A Single-Stage, Single-Inductor, 6-Input 9-Output Multi-Modal Energy Harvesting Power Management IC for 100µW-120mW Battery-Powered IoT Edge Nodes, Suhwan Kim, Vaibhav Vaidya, Christopher Schaef, Andrew Lines, Harish Krishnamurthy, Sheldon Weng, Xiaosen Liu, Dileep Kurian, Tanay Karnik, Krishnan Ravichandran, James Tschanz, Vivek De, Intel Corporation

Session 19 - TAPA 1
Oversampling Data Converters
Thursday, June 21, 10:05 a.m.

Co-Chairs: E. Martens, imec
M. Fukazawa, Renesas Electronics Corp.

C19-1 - 10:05 a.m.
A 1.2V 68µW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator, C. Lee, M. Jang, Y. Chae, Yonsei University

C19-2 - 10:30 a.m.
A 0.029mm^2 17-fJ/Conv.-Step CT ΔΣ ADC With 2nd-Order Noise-Shaping SAR Quantizer, Jiaxin Liu, Shaolan Li*, Wenjuan Guo*, Guangjun Wen, Nan Sun*, University of Electronic Science and Technology of China, *The University of Texas at Austin

C19-3 - 10:55 a.m.
A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure, Y. Song, Y. Zhu, C.-H. Chan, L. Geng*, R. P. Martins, University of Macau, *Xi'an Jiaotong University

C19-4 - 11:20 a.m.
A 1.25MS/s Two-Step Incremental ADC with 100dB DR and 110dB SFDR, T. Katayama, S. Miyashita, K. Sobue, K. Hamashita, Asahi Kasei Microdevices

C19-5 - 11:45 a.m.
A 550µW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65nm CMOS, B. Wang, S.-W. Sin, S.-P. U*, F. Maloberti**, R. P. Martins, University of Macau, *Synopsys Macau Ltd. ** University of Pavia

Session 20 - HONOLULU 1
RF Circuits and Techniques
Thursday, June 21, 10:05 a.m.

Co-Chairs: M. Chen, University of Southern California
H. Shin, Kwangwoon University

C20-1 - 10:05 a.m.
Terahertz RF Front-End Employing Even-Order Subharmonic MOS Symmetric Varactor Mixers in 65-nm CMOS for Hydration Measurements at 560 GHz, Q. Zhong, W. Choi , K. O, The University of Texas at Dallas

C20-2 - 10:30 a.m.
A Sub-Harmonic Switching Digital Power Amplifier with Hybrid Class-G Operation for Enhancing Power Back-off Efficiency, A. Zhang, M. Chen, University of Southern California

C20-3 - 10:55 a.m.

A 5.5 GHz Background-Calibrated Subsampling Polar Transmitter with -41.3 dB EVM at 1024 QAM in 28nm CMOS, N. Markulic*, P. Renukaswamy*, E. Martens, B. van Liempd, P. Wambacq*, J. Craninckx, imec; *also at Vrije Universiteit Brussel

C20-4 - 11:20 a.m.
A 16-Gb/s 0-dB Power Back-off 16-QAM Transmitter at 28 GHz in 65-nm CMOS, X. Meng, C. Wang, M. Kalantari, C. P. Yue, The Hong Kong University of Science and Technology

C20-5 - 11:45 a.m.
A modular 16nm Direct-RF TX/RX embedding 9GS/s DAC and 4.5GS/s ADC with 90dB isolation and sub-80ps channel alignment for monolithic integration in 5G base-station SoC, C. Erdmann, B. Verbruggen, B. Vaz, R. Pelliconi, J. Mcgrath, R. Kinnerk, R. De La Torre, P. Lynch, J. O'Dwyer, P. Kelly, P. Lim, D. Breathnach, B. Farley, XILINX

Session 21 - HONOLULU 2
Power Converters
Thursday, June 21, 10:05 a.m.

Co-Chairs: M. Chen, ADI / Linear
K. Kanda, Fujitsu Laboratories, Ltd.

C21-1 - 10:05 a.m.
A 95.3% Peak Efficiency, 135nA Quiescent Current Buck-Boost DC-DC Converter with Current-Slope-Based Mode Control, D. Lu, P. Liu, S. Yao, L. Wang, J. He, Analog Device Inc.

C21-2 - 10:30 a.m.
A Hybrid Dual-Path Step-Down Converter with 96.2% Peak Efficiency using a 250mΩ Large-DCR Inductor, Y. Huh, S.-U. Shin, S.-W. Hong*, Y.-J. Woo**, Y.-M, Ju, S.-W. Choi, G.-H. Cho, KAIST, *Sookmyung Women's University, **Silicon Works

C21-3 - 10:55 a.m.
A 92.8% Efficiency Adaptive-On/Off-Time Control 3-Level Buck Converter for Wide Conversion Ratio with Shared Charge Pump Intermediate Voltage Regulator, Y. Karasawa, T. Fukuoka, K. Miyaji, Shinshu University

C21-4 - 11:20 a.m.
An Ultra-low Quiescent Current 250nA Low Dropout Regulator for No-load to 10mA Internet-of-Everything Applications, S.-Q.Chen, C.-M. Huang, K.-H. Chen, Y.-H. Lin*, S.-R. Lin*, T.-Y. Tsai*, National Chiao Tung University, *Realtek Semiconductor Corporation

C21-5 - 11:45 a.m.
A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit, J.-E Park, D.-K. Jeong, Seoul National University

Session 23 - TAPA 1
Advanced Amplifiers and Analog Front-Ends
Thursday, June 21, 1:50 p.m.

Co-Chairs: A. Molnar, Cornell University
M. Je, KAIST

C22-1 - 1:50 p.m.
A 1mW -101dB THD+N Class-AB High-Fidelity Headphone Driver in 65nm CMOS, N. Mehta, J. Huijsing*, V. Stojanovic, University of California at Berkeley, *Delft University of Technology

C22-2 - 2:15 p.m.
A 2.2 NEF Neural-Recording Amplifier Using Discrete-Time Parametric Amplification, T. Jang, K. Choo, J. Lim, S. Nason, J. Lee, S. Oh, S. Jeong, C. Chestek, D. Sylvester, D. Blaauw, University of Michigan

C22-3 - 2:40 p.m.
A 6.5µW 92.3dB-DR Biopotential-Recording Front-End with 360mV$_{pp}$ Linear Input Range, J.-S. Bang*, H. Jeon, M. Je, G.-H. Cho, KAIST, *also with Samsung Electronics

C22-4 - 3:05 p.m.
A 0.6V 54dB SNR Analog Frontend with 0.18% THD for Low Power Sensory Applications in 65nm CMOS, K. Badami, K. Murthy, P. Harpe*, M. Verhelst, KU Leuven, Texas Instruments, *Eindhoven University of Technology

Session 22 - HONOLULU 1
Next Generation Sensors
Thursday, June 21, 1:50 p.m.

Co-Chairs: A. Arbabian, Stanford University
Y. Hirose, Panasonic Corp.

C23-1 - 1:50 p.m.
A 5500fps 85GOPS/W 3D stacked BSI vision chip based on parallel in-focal-plane acquisition and processing, L. Millet, S. Chevobbe, C. Andriamisaina, E. Beigne, F. Guellec, T. Dombek, L. Benaissa, E. Deschaseaux, M. Duranton, K. Benchehida, M. Darouich, M. Lepecq, CEA

C23-2 - 2:15 p.m.
A 2pJ/pixel/direction MIMO Processing based CMOS Image Sensor for Omnidirectional Local Binary Pattern Extraction and Edge Detection, X. Zhong, Q. Yu, A. Bermak**, C.-Y. Tsui, M.-K. Law*, Hong Kong University of Science and Technology, *University of Macau, **also with Hamad Bin Khalifa University

C23-3 - 2:40 p.m.
Room-Temperature Quantum Sensing in CMOS: On-Chip Detection of Electronic Spin States in Diamond Color Centers for Magnetometry, M. Ibrahim, C. Foy, D. Kim, D. Englund, and R. Han, Massachusetts Institute of Technology

C23-4 - 3:05 p.m.
A 179-lux Energy-Autonomous Fully-Encapsulated 17-mm³ Sensor Node with Initial Charge Delay Circuit for Battery Protection, I. Lee, G. Kim*, E. Moon, S. Jeong*, D. Kim, J. Phillips, D. Blaauw*, University of Michigan, *also with CubeWorks

Session 24 - TAPA 1
Machine Learning for Health and Neuro Inspired Processing
Thursday, June 21, 3:45 p.m.

Co-Chairs: V. Sze, Massachusetts Institute of Technology
H. Inoue, NEC Corp.

C24-1 - 3:45 p.m.
A 4096-neuron 1M-synapse 3.8pJ/SOP Spiking Neural Network with On-chip STDP Learning and Sparse Weights in 10nm FinFET CMOS, G. K. Chen, R. Kumar, H. E. Sumbul, P. Knag, R. K. Krishnamurthy, Intel Corporation

C24-2 - 4:10 p.m.
A 0.76mm² 0.22nJ/Pixel DL-assisted 4K Video Encoder LSI for Quality-of-Experience over Smart-Phones, Tsu-Ming Liu, Chang-Hung Tsai, Tung-Hsing Wu, Jia-Ying Lin, Li-Heng Chen, Han-Liang Chou and Chi-Cheng Ju, Mediatek Inc.

C24-3 - 4:35 p.m.
A 1.9mW SVM Processor with On-chip Active Learning for Epileptic Seizure Control, S-A. Huang, K.-C. Chang*, H.-H. Liou*, C.-H. Yang**, National Taiwan University, *National Taiwan University Hospital, ** also with National Chiao-Tung University

C24-4 - 5:00 p.m.
A 12.6mW 573-2,901KS/s Reconfigurable Processor for Reconstruction of Compressively-Sensed Physiological Signals, Y.-Z. Wang, Y.-P. Wang, Y.-C. Wu, C.-H. Yang, National Taiwan University

C24-5 - 5:25 p.m.
PhaseMAC: A 14 TOPS/W 8bit GRO based Phase Domain MAC Circuit for In-Sensor-Computed Deep Learning Accelerators, K. Yoshioka, Y. Toyama, K. Ban, D. Yashima, S. Maya, A. Sai, K. Onizuka, Toshiba

Session 25 - HONOLULU 1
Wireline Building Blocks
Thursday, June 21, 3:45 p.m.

Co-Chairs: B. Casper, Intel Corp.
H. Katsurai, NTT Device Technology Laboratories

C25-1 - 3:45 p.m.
A 50Gb/s 1.6pJ/b RX Data-Path with Quarter-Rate 3-tap Speculative DFE, P.A. Francese, A. Cevrero, I. Ozkaya, M. Braendli, C. Menolfi, T. Morf, M. Kossel, L. Kull, D. Luu* and T. Toifl, IBM Research-Zurich, *also with ETH

C25-2 - 4:10 p.m.
An Inverter-based Analog Front End for a 56 Gb/s PAM4 Wireline Transceiver in 16nm CMOS, K. Zheng, Y. Frans*, Sai L. Ambatipudi*, S. Asuncion*, H. Reddy*, K. Chang*, B. Murmann, Stanford University, *Xilinx Inc.

C25-3 - 4:35 p.m.
A 14 µm × 26 µm 20-Gb/s 3-mW CDR Circuit with High Jitter Tolerance, Long Kong, Yikun Chang, Behzad Razavi, University of California, Los Angeles

C25-4 - 5:00 p.m.
A 40Gb/s Optical NRZ Transmitter Based on Monolithic Microring Modulators in 45nm SOI CMOS, S. Lin, S. Moazeni, V. Stojanovic, University of California, Berkeley

C25-5 - 5:25 p.m.
A 10-bit 20-40 GS/s ADC with 37 dB SNDR at 40 GHz Input using First Order Sampling Bandwidth Calibration, L. Kull*, D. Luu**, C. Menolfi, Thomas Morf, P. Francese, M. Braendli, M. Kossel, A. Cevrero, I. Ozkaya, T. Toifl. IBM Research, **also with ETH