Session 1 – TAPA 1/2/3

Joint Plenary Session

Tuesday, June 19, 8:10 a.m.

8:10 a.m. **Joint Welcome and Opening Remarks**
Mukesh Khare, IBM, VLSI Technology General Chair
Gunther Lehmann, Infineon, VLSI Circuits General Chair

Technology Plenary

T1-1- 8:40 a.m. **Memory Technology: The Core to Enable Future Computing Systems**
Scott J. DeBoer, Micron Technology, Inc.

9:20 a.m. **EDS Remarks, Fellows Recognition**
Fernando Guarin, EDS President
Mukesh Khare, VLSI Technology General Chair

T1-2- 9:30 a.m. **Revolutionizing Cancer Genomic Medicine by AI and Supercomputer with Big Data**
Satoru Miyano, University of Tokyo

10:10 a.m. **Break**

Circuits Plenary

10:30 a.m. **Best Student Paper Awards and IEEE Awards**
Gunther Lehmann, Infineon, VLSI Circuits General Chair
Mukesh Khare, IBM, VLSI Technology General Chair

C1-1- 10:40 a.m.
Hardware-Enabled Artificial Intelligence
Bill Dally, nVidia

11:20 a.m. **2019 VLSI Simposia Joint Announcement**
Makoto Ikeda, University of Tokyo
Meishoku Masahara, AIST

C1-2- 11:30 a.m.
Semiconductor Technologies Accelerate Our Future Vision: "ANSHIN Platform"
Tsuneo Komatsuzaki, SECOM

12:10 p.m. **Lunch Break**

Session T2 – TAPA 3
Technology Focus Session: Back-End Compatible Devices and Advanced Thermal Management
Tuesday, June 19, 1:30 p.m.

Co-Chairs: K. Benaissa, Texas Instruments
K. Endo, AIST

T2-1- 1:30 p.m.
Shaping Circuit Environment to Face Thermal Challenges (Invited), P. Coudrain, STMicroelectronics

T2-2- 1:55 p.m.
Thermal Management Research – From Power Electronics to Portables (Invited), K. Goodson, Stanford University

T2-3- 2:20 p.m.
Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points, C. Zhou, R. Wong*, S-J. Wen*, C. H. Kim, University of Minnesota, *Cisco Systems

T2-4- 2:45 p.m.
Low Thermal Budget Amorphous Indium Tungsten Oxide Nano-Sheet Junctionless Transistors with Near Ideal Subthreshold Swing, P-Y. Kuo, C-M. Chang, P-T. Liu, National Chiao Tung University

Session T3 – TAPA 2
Devices and Systems for AI
Tuesday, June 19, 1:30 p.m.

Co-Chairs: K. Baker, NXP
T. Tanaka, Tohoku University

T3-1- 1:30 p.m.
Capacitor-Based Cross-Point Array for Analog Neural Network with Record Symmetry and Linearity, Y. Li, S. Kim, X. Sun, P. Solomon, T. Gokmen, H. Tsai, S. Koswatta, Z. Ren, R. Mo, C. C. Yeh, W. Haensch, E. Leobandung, IBM T. J. Watson Research Center

T3-2- 1:55 p.m.
Analog Spike Processing with High Scalability and Low Energy Consumption Using Thermal Degree of Freedom in Phase Transition Materials, T. Yajima, T. Nishimura, A. Toriumi, The University of Tokyo

T3-3- 2:20 p.m.
An Energy Efficient FinFET-Based Field Programmable Synapse Array (FPSA) Feasible for One-Shot Learning on EDGE AI, J. L. Kuo, H. W. Chen, E. R. Hsieh, S. S. Chung, T. P. Chen*, S. A. Huang*, T. J. Chen*, O. Cheng*, National Chiao Tung University, *UMC

T3-4- 2:45 p.m.
Novel In-Memory Matrix-Matrix Multiplication with Resistive Cross-Point Arrays, Y. Liao, H. Wu, W. Wan*, W. Zhang, B. Gao, H-S. P. Wong*, H. Qian, Tsinghua University, *Stanford University

3:10 p.m. **Break**

Session T4 – TAPA 3
Technology Focus Session: Sensors and Devices for IoT, Medicine and Smart Living
Tuesday, June 19, 1:30 p.m.

Co-Chairs: T. Skotnicki, STMicroelectronics
O. Cheng, United Microelectronics Corp.

T4-1- 3:25 p.m.
Sensors & Related Devices for IoT, Medicine, and Smart Living (Invited), T. Ernst, CEA LETI, APIX Analytics, Moovlab

T4-2- 3:50 p.m.
Development of Multisite, Closed-Loop Neuromodulator for Theranosis of Neural Degenerative Diseases (Invited), H. Chen, National Tsing-Hua University

T4-3- 4:15 p.m.
High Performance High Density Gas-FET Array in Standard CMOS, Q. Yu*, X. Zhong*, F. Boussaid**, A. Bermak*,***, C. Y. Tsui*, *Hong Kong University of Science and Technology, **University of Western Australia, ***Hamad Bin Khalifa University

T4-4- 4:40 p.m.
High-Sensitivity and Low-Power Inertial MEMS-on-CMOS Sensors using Low-Temperature-Deposited Poly-SiGe Film for the IoT Era, H. Tomizawa, Y. Kurui, I. Akita*, A. Fujimoto, T. Saito, A. Kojima, H. Shibata, Toshiba Corporation, *Toyohashi University of Technology

Session T5 – TAPA 2
Negative Capacitance FET
Tuesday, June 19, 1:30 p.m.

Co-Chairs: S. Datta, University of Notre Dame
M. Kobayashi, The University of Tokyo

T5-1- 3:25 p.m.
A Comprehensive Study of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Layer Effects on Negative Capacitance FETs for Sub-5 nm Node, Y-T. Tang, C-J. Su, Y-S. Wang*, K-H. Kao*, T-L. Wu**, P-J. Sung, F-J. Hou, C-J. Wang, M-S. Yeh, Y-J. Lee, W-F. Wu, G-W. Huang, J-M. Shieh, W-K. Yeh, Y-H. Wang*,***, National Nano Device Laboratories, *National Cheng Kung University, **National Chiao Tung University, ***National Applied Research Laboratories

T5-2- 3:50 p.m.
First Experimental Demonstration of Negative Capacitance InGaAs MOSFETs With $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Gate Stack, Q. H. Luc*, C. C. Fan-Chiang*, S. H. Huynh*, P. Huang*, H. B. Do*, M. T. H. Ha*, Y. D. Jin*, T. A. Nguyen*, K. Y. Zhang*, H. C. Wang*, Y. K. Lin*, Y. C. Lin*, C. Hu*,**, H. Iwai*,***, E. Y. Chang*, *National Chiao Tung University, **University of California Berkeley, ***Tokyo Institute of Technology

T5-3- 4:15 p.m.
Response Speed of Negative Capacitance FinFETs, D. Kwon, Y-H. Liao, Y-K. Lin, J. P. Duarte, K. Chatterjee, A. J. Tan, A. K. Yadav, C. Hu, Z. Krivokapic*, S. Salahuddin, University of California, Berkeley, *GLOBALFOUNDRIES Inc.

T5-4- 4:40 p.m.
Ferroelectric Switching Delay as Cause of Negative Capacitance and the Implications to NCFETs (Invited), B. Obradovic, Samsung

T5-5- 5:05 p.m.
Negative Capacitance, n-Channel, Si FinFETs: Bi-Directional Sub-60 mV/dec, Negative DIBL, Negative Differential Resistance and Improved Short Channel Effect, H. Zhou, D. Kwon, A. B. Sachid, Y. Liao, K. Chatterjee, A. J. Tan, A. K. Yadav, C. Hu, and S. Salahuddin, University of California, Berkeley

Session T6 – TAPA 2/3
Technology Highlights
Wednesday, June 20, 8:10 a.m.

Co-Chairs: T. Palacios, Massachusetts Institute of Technology
M. Tada, NEC Corp.

T6-1- 8:10 a.m.
True 7 nm Platform Technology Featuring Smallest FinFET and Smallest SRAM Cell by EUV, Special Constructs and 3rd Generation Single Diffusion Break, W. C. Jeong, S. Maeda, H. J. Lee, K. W. Lee, T. J. Lee, D. W. Park, B. S. Kim, J. H. Do*, T. Fukai, D. J. Kwon, K. J. Nam, W. J. Rim*, M. S. Jang*, H. T. Kim*, Y. W. Lee*, J. S. Park, E. C. Lee*, D. W. Ha, C. H. Park, H-J. Cho, S-M. Jung, H. K. Kang, Semiconductor R&D Center, Samsung Electronics, *Foundry Business, Samsung Electronics

T6-2- 8:35 a.m.
Nanosecond Laser Anneal for BEOL Performance Boost in Advanced FinFETs, R. Lee, N. Petrov, J. Kassim, M. Gribelyuk, J. Yang, L. Cao, K. B. Yeap, T. Shen, A. N. Zainuddin, A. Chandrashekar, S. Ray, E. Ramanathan, A. S. Mahalingam, R. Chaudhuri, J. Mody, D. Damjanovic, Z. Sun, R. Sporer, T. J. Tang, H. Liu, J. Liu, B. Krishnan, GLOBALFOUNDRIES

T6-3- 9:00 a.m.
From Memory to Sensor: Ultra-Low Power and High Selectivity Hydrogen Sensor Based on ReRAM Technology, Z. Wei, K. Homma, K. Katayama, K. Kawai, S. Fujii, Y. Naitoh*, H. Shima*, H. Akinaga*, S. Ito, S. Yoneda, Panasonic Semiconductor Solutions Co., *National Institute of Advanced Industrial Science and Technology

T6-4- 9:25 a.m.
Demonstration of Ultra-Low Voltage and Ultra-Low Power STT-MRAM Designed for Compatibility with 0x Node Embedded LLC Applications, G. Jan, L. Thomas, S. Le, Y-J. Lee, H. Liu, J. Zhu, J. Iwata-Harms, S. Patel, R-Y. Tong, V. Sundar, S. Serrano-Guisan, D. Shen, R. He, J. Haq, Z. J. Teng, V. Lam, Y. Yang, Y-J. Wang, T. Zhong, H. Fukuzawa, P-K. Wang, TDK-Headway Technologies

9:50 a.m. Break

Session T7 – TAPA 3
Process and Material Technologies 1
Wednesday, June 20, 10:05 a.m.

Co-Chairs: Y. Pan, LAM Research
T. Tsunomura, Tokyo Electron Ltd.

T7-1- 10:05 a.m.
3D Sequential Stacked Planar Devices on 300 mm Wafers Featuring Replacement Metal Gate Junction-Less Top Devices Processed at 525 °C with Improved Reliability, A. Vandooren, J. Franco, B. Parvais**, Z. Wu, L. Witters, A. Walke, W. Li, L. Peng, V. Desphande, F. M. Bufler***, N. Rassoul, G. Hellings, G. Jamieson, F. Inoue, G. Verbinnen, K. Devriendt, L. Teugels, N. Heylen, E. Vecchio, T. Zheng, E. Rosseel, W. Vanherle, A. Hikavyy, B. T. Chan, R. Ritzenthaler, G. Besnard*, W. Schwarzenbach*, G. Gaudin*, I. Radu*, B-Y. Nguyen*, N. Waldron, V. De Heyn, D. Mocuta, N. Collaert, imec, *SOITEC, **also with Vrije Universiteit Brussel, ***also with ETH Zürich

T7-2- 10:30 a.m.
An Over 120 dB Wide-Dynamic-Range 3.0 µm Pixel Image Sensor with In-Pixel Capacitor of 41.7 fF/µm^2 and High Reliability Enabled by BEOL 3D Capacitor Process, M. Takase, S. Isono, Y. Tomekawa, T. Koyanagi, T. Tokuhara, M. Harada, Y. Inoue, Technology Innovation Division, Panasonic Corporation

T7-3- 10:55 a.m.
Selective Pore-Sealing of Highly Porous Ultra-Low-k Dielectrics for ULSI Interconnects by Cyclic Initiated Chemical Vapor Deposition Process, S. J. Yoon, K. Pak*, H. J. Ahn, A. Yoon**, S. G. Im*, B. J. Cho, Dep. of Electrical Eng., KAIST, *Dep. of Chemical and Biomolecular, KAIST, **Lam Research Corp.

T7-4- 11:20 a.m.
Performance and Reliability of a Fully Integrated 3D Sequential Technology, A. Tsiara*,**,***, X. Garros*,***, L. Brunet*,***, P. Batude*,***, C. Fenouillet-Béranger*,***, K. Triantopoulos*,***, M. Cassé*,***, M. Vinet*,***, F. Gaillard*,*** G. Ghibaudo**,***, *CEA-LETI, MINATEC, **IMEP-LAHC, ***Université Grenoble Alpes

T7-5- 11:45 a.m.
Metal/P-type GeSn Contacts with Specific Contact Resistivity Down to 4.4×10^{-10} Ω·cm^2, Y. Wu, W. Wang, S. Masudy-Panah, Y. Li, K. Han, L. He, Z. Zhang*, D. Lei, S. Xu, Y. Kang, X. Gong, Y-C. Yeo, National University of Singapore, *Institute of Material Research and Eng. A*STAR

Session T8 – TAPA 2
Advanced FinFET and GAA
Wednesday, June 20, 10:05 a.m.

Co-Chairs: V. Narayanan, IBM
Y. Masuoka, Samsung Electronics Co., Ltd.

T8-1- 10:05 a.m.
Multiple Workfunction High Performance FinFETs for Ultra-Low Voltage Operation, M. Togo, R. Asra, P. Balasubramaniam, X. Zhang, H. Yu, S. Yamaguchi, E. Geiss, H. S. Yang, B. Cohen, H-C. Lo, O. Hu, H. Lazar,

O. Kwon, D. Burnett, J. Versaggi, E. Banghart, M. K. Hassan, E. Bazizi, L. Pantisano, J. G. Lee, S. B. Samavedam, D. K. Sohn, GLOBALFOUNDRIES

T8-2- 10:30 a.m.
An In-Depth Study of High-Performing Strained Germanium Nanowires pFETs, J. Mitard, D. Jang, G. Eneman, H. Arimura, B. Parvais*, O. Richard, P. Van Marcke, L. Witters, E. Capogreco, H. Bender, R. Ritzenthaler, H. Mertens, A. Hikavyy, R. Loo, H. Dekkers, F. Sebaai, A. Milenin, N. Horiguchi, A. Mocuta, D. Mocuta, N. Collaert, imec, *also with Vrije Universiteit Brussel

T8-3- 10:55 a.m.
Si/SiGe Superlattice I/O FinFETs in a Vertically-Stacked Gate-All-Around Horizontal Nanowire Technology, G. Hellings*, H. Mertens, A. Subirats, E. Simoen, T. Schram, L.-A. Ragnarsson, M. Simicic, S-H. Chen, B. Parvais***, D. Boudier*, B. Cretu*, J. Machillot**, V. Pena**, S. Sun[¥], N. Yoshida[¥], N. Kim**, A. Mocuta, D. Linten, N. Horiguchi, imec, *Normandie University, **Applied Materials Leuven, [¥]Applied Materials Santa Clara, ***also with Vrije Universiteit Brussel

T8-4- 11:20 a.m.
Leakage Aware Si/SiGe CMOS FinFET For Low Power Applications, G. Tsutsui, C. Durfee*, M. Wang, A. Konar*, H. Wu, S. Mochizuki, R. Bao, S. Bedell, J. Li, H. Zhou, D. Schmidt*, C. Yang*, J. Kelly, K. Watanabe, T. Levin, W. Kleemeier*, D. Guo, D. Sadana, D. Gupta, A. Knorr*, H. Bu, IBM Research, *Globalfoundries

T8-5- 11:45 a.m.
First Direct Experimental Studies of $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Polarization Switching Down to 100-picosecond in Sub-60 mV/dec Germanium Ferroelectric Nanowire FETs, W. Chung, M. Si, P. Shrestha*, J. Campbell*, K. Cheung*, P. Ye, Purdue University, *NIST

12:10 a.m. Lunch Break

Session T9 – TAPA 3
IoT Devices and Technology
Wednesday, June 20, 1:30 p.m.

Co-Chairs: E. Pop, Stanford University
N. Sugii, Hitachi, Ltd.

T9-1- 1:30 p.m.
10 μW/cm^2-Class High Power Density Planar Si-Nanowire Thermoelectric Energy Harvester Compatible with CMOS-VLSI Technology, M. Tomita, S. Ohba, Y. Himeda, R. Yamato, K. Shima, T. Kumada, M. Xu, H. Takezawa, K. Mesaki, K. Tsuda, S. Hashimoto, T. Zhan, H. Zhang*, Y. Kamakura**, Y. Suzuki***, H. Inokawa***, H. Ikeda***, T. Matsukawa[^], T. Matsuki[¥], T. Watanabe, Waseda University, *Gunma University, **Osaka University, ***Shizouka University, [^]AIST, [¥]Waseda University and AIST

T9-2- 1:55 p.m.
A Low-Power and High-Speed True Random Number Generator Using Generated RTN, J. Brown, R. Gao, Z. Ji, J. Chen*, J. Wu*, J. Zhang, B. Zhou, Q. Shi, J. Crowford, W. Zhang, Liverpool John Moores University, *Shandong University

T9-3- 2:20 p.m.

Ultrahigh-Sensitive and CMOS Compatible ISFET Developed in BEOL of Industrial UTBB FDSOI, G. P. Ayele*,**,***,^, S. Monfray*, S. Ecoffey***,^, F. Boeuf^, R. Bon*, J. P. Cloarec**, D. Drouin***,^, A. Souifi**, *STMicroelectronics, **INL - Lyon Institute of Nanotechnology, ***3IT, Université de Sherbrooke, ^LN2, Université de Sherbrooke

T9-4- 2:45 p.m.
RX-PUF: Low Power, Dense, Reliable, and Resilient Physically Unclonable Functions Based on Analog Passive RRAM Crossbar Arrays, M. R. Mahmoodi, H. Nili, D. B. Strukov, University of California, Santa Barbara

Session T10 – TAPA 2
Resistive RAM
Wednesday, June 20, 1:30 p.m.

Co-Chairs: G. Jurczak, ASM
B. Hun Lee, Gwangju Institute of Science and Technology

T10-1- 1:30 p.m.
A Methodology to Improve Linearity of Analog RRAM for Neuromorphic Computing, W. Wu, H. Wu, B. Gao, P. Yao, X. Zhang, X. Peng*, S. Yu*, H. Qian, Tsinghua University, *Arizona State University

T10-2- 1:55 p.m.
Non-Volatile Ternary Content Addressable Memory (TCAM) with Two $HfO_2/Al_2O_3/GeO_x$/Ge MOS Diodes, Y. Zhang, B. Chen, W. Dong, W. Liu, S. Xu, R. Cheng, S-W. Lee, Y. Zhao, Zhejiang University

T10-3- 2:20 p.m.
Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM, Z. Jiang*, S. Qin*, H. Li*, S. Fujii**, D. Lee***, S. Wong*, H-S. P. Wong*, *Stanford University, **also with Toshiba Memory Corporation, ***also with Semiconductor R&D Center Samsung

T10-4- 2:45 p.m.
5x Reliability Enhanced 40 nm TaO_x Approximate-ReRAM with Domain-Specific Computing for Real-Time Image Recognition of IoT Edge Devices, Y. Yamaga, Y. Deguchi, S. Fukuyama, K. Takeuchi, Chuo University

3:10 p.m. Break

Session T11 – TAPA 3
Process and Material Technologies 2
Wednesday, June 20, 3:25 p.m.

Co-Chairs: N. Collaert, imec
K. Tateiwa, Tower Jazz Panasonic Semi. Co., Ltd.

T11-1- 3:25 p.m.
Comprehensive Thermal SPICE Modeling of FinFETs and BEOL with Layout Flexibility Considering Frequency Dependent Thermal Time Constant, 3D Heat Flows, Boundary/Alloy Scattering, and Interfacial Thermal Resistance with Circuit Level Reliability Evaluation, J-Y. Yan , C-C. Chung, S-R. Jan, H.

H. Lin*, W. K. Wan*, M-T. Yang*, C. W. Liu^, National Taiwan University, *PTD Media Tek, ^also with National Nanodevice Laboratories NTU

T11-2- 3:50 p.m.
Differentiated Performance and Reliability Enabled by Multi-Work Function Solution in RMG Silicon and SiGe MOSFETs, R. Bao, R. G. Southwick III, H. Zhou, C. H. Lee, B. P. Linder, T. Ando, D. Guo, H. Jagannathan, V. Narayanan, IBM Research, Albany

T11-3- 4:15 p.m.
Process Optimization of Perpendicular Magnetic Tunnel Junction Arrays for Last-Level Cache Beyond 7 nm Node, L. Xue, C. Ching, A. Kontos, J. Ahn, X. Wang, R. Whig, H. Tseng, J. Howarth, S. Hassan, H. Chen, M. Bangar, S. Liang, R. Wang, M. Pakala, Applied Materials, Inc.

T11-4- 4:40 p.m.
Dependence of Reliability of Ferroelectric $HfZrO_x$ on Epitaxial SiGe Film with Various Ge Content, K-Y. Chen, Y-H. Huang, R-W. Kao, Y-X. Lin, Y-H. Wu, National Tsing Hua University

T11-5- 5:05 p.m.
Modeling of FinFET Self-Heating Effects in Multiple FinFET Technology Generations with Implication for Transistor and Product Reliability, H. C. Sagong, K. Choi, J. Kim, T. Jeong, M. Choe, H. Shim, W. Kim, J. Park, S. Shin, S. Pae, Foundry Business, Samsung Electronics

Session T12 – TAPA 2
Beyond CMOS
Wednesday, June 20, 3:25 p.m.

Co-Chairs: P. Ye, Purdue University
K. Miyashita, Toshiba Corp.

T12-1- 3:25 p.m.
All-Electrical Control of a Hybrid Electron Spin/Valley Quantum Bit in SOI CMOS Technology, L. Hutin*, L. Bourdet**, B. Bertrand*, A. Corna**, H. Bohuslavskyi*,**, A. Amisse*,**, A. Crippa**, R. Maurand**, S. Barraud*, M. Urdampilleta***, C. Bäuerle***, T. Meunier***, M. Sanquer**, X. Jehl**, S. De Franceschi**, Y.-M. Niquet**, M. Vinet*, *CEA-LETI, **CEA, INAC, ***CNRS, Institute Néel

T12-2- 3:50 p.m.
High-Density and Fault-Tolerant Cu Atom Switch Technology Toward 28 nm-node Nonvolatile Programmable Logic, R. Nebashi, N. Banno, M. Miyamura, Y. Tsuji, A. Morioka, X. Bai, K. Okamoto, N. Iguchi, H. Numata, H. Hada, T. Sugibayashi, T. Sakamoto, M. Tada, NEC Corporation

T12-3- 4:15 p.m.
A Threshold Switch Augmented Hybrid-FeFET (H-FeFET) with Enhanced Read Distinguishability and Reduced Programming Voltage for Non-Volatile Memory Applications, M. Jerry, A. Aziz*, K. Ni, S. Datta, S. K. Gupta*, N. Shukla**, University of Notre Dame, *Purdue University, ** University of Virginia

T12-4- 4:40 p.m.
A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs, K. Ni, M. Jerry, J. A. Smith, and S. Datta, University of Notre Dame

T12-5- 5:05 p.m.
Record 47 mV/dec Top-Down Vertical Nanowire InGaAs/GaAsSb Tunnel FETs, A. Alian, S.El Kazzi, A. Verhulst, A. Milenin, N. Pinna, T. Ivanov, D. Lin, D. Mocuta, N. Collaert, imec

Session T13 – TAPA 3
FET Performance and Scaling
Thursday, June 21, 8:10 a.m.

Co-Chairs: G. Yeric, ARM
K. Uchida, Keio University

T13-1- 8:10 a.m.
Improving Performance, Power, and Area by Optimizing Gear Ratio of Gate-Metal Pitches in Sub-10 nm Node CMOS Designs, Y. Ban, X. Zhu, J. Petykiewicz, J. Zeng, GLOBALFOUNDRIES

T13-2- 8:35 a.m.
Achieving High-Scalability Negative Capacitance FETs with Uniform Sub-35 mV/dec Switch Using Dopant-Free Hafnium Oxide and Gate Strain, C. C. Fan, C. H. Cheng*, C. Y. Tu, C. Liu, W. H. Chen, T-J. Chang, C. Y. Chang, National Chiao Tung Univ., *National Taiwan Normal Univ.

T13-3- 9:00 a.m.
The Complementary FET (CFET) for CMOS Scaling Beyond N3, J. Ryckaert, P. Schuddinck, P. Weckx, G. Bouche*, B. Vincent**, J. Smith***, Y. Sherazi, A. Mallik, H. Mertens, S. Demuynck, T. Huynh Bao, A. Veloso, N. Horiguchi, A. Mocuta, D. Mocuta, J. Boemmels, imec, *GLOBALFOUNDRIES assegnee at imec, **Coventor, ***Tokyo Electron, Albany

T13-4- 9:25 a.m.
Power-Performance Trade-Offs for Lateral Nano-Sheets on Ultra-Scaled Standard Cells, M. Garcia Bardon, Y. Sherazi, D. Jang, D. Yakimets, P. Schuddinck, R. Baert, H. Mertens, L. Mattii*, B. Parvais**, A. Mocuta, D. Verkest, imec, *Cadence Design System, **also with Vrije Universiteit Brussel

Session T14 – TAPA 2
Joint Focus Session: DTCO
Thursday, June 21, 8:10 a.m.

Co-Chairs: Y. Liang, nVidia
K. Tomida, Sony Semiconductor Solutions Corp.

T14-1- 8:10 a.m.
Enabling CMOS Scaling Towards 3 nm and Beyond (Invited), A. Mocuta, P. Weckx, S. Demuynck, D. Radisic, Y. Oniki, J. Ryckaert, imec

T14-2- 8:35 a.m.
Smart Scaling Technology for Advanced FinFET Devices (Invited), J. Kye, Samsung

T14-3- 9:00 a.m.

Sub-550 mV SRAM Design in 22 nm FinFET Low Power (22FFL) Technology with Self-Induced Collapse Write Assist, D. Kim, J. Wiedemer, P. Kolar, A. Shrivastava, J. Shah, S. Nalam, G. Baek, X. Wang, Z. Guo, E. Karl, Intel Corporation

T14-4- 9:25 a.m.
Design Technology Co-Optimization in Advanced FDSOI CMOS Around the Minimum Energy Point: Body Biasing and Within-Cell V_T-Mixing, F. Andrieu, L. Pirro*, R. Berthelon**, J. Morgan*, G. Cibrario, M. Wiatr*, J. Hoentschel* and M. Vinet, CEA-LETI, * GLOBALFOUNDRIES fab1, **also with STMicroelectronics

9:50 a.m. Break

Session T15 – TAPA 3
Photonics and RF/Analog
Thursday, June 21, 10:05 a.m.

Co-Chairs: T. Letavic, GLOBALFOUNDRIES
Y. Shiratori, NTT Corp.

T15-1- 10:05 a.m.
Self-Organized Gate Stack of Ge Nanosphere/SiO_2/$Si_{1-x}Ge_x$ Enables Ge-Based Monolithically-Integrated Electronics and Photonics on Si Platform, P. H. Liao*, M. H. Kuo*, C. W. Tien**, Y. L. Chang**, P. Y. Hong**, T. George*, H. C. Lin**, and P. W. Li*,**, *National Central University, **National Chiao Tung University

T15-2- 10:30 a.m.
A Near- & Short-Wave IR Tunable InGaAs Nanomembrane PhotoFET on Flexible Substrate for Lightweight and Wide-Angle Imaging Applications, Y. Li, A. Alian*, L. Huang, K. W. Ang, D. Lin*, D. Mocuta*, N. Collaert*, A.V-Y. Thean, National University of Singapore, *imec

T15-3- 10:55 a.m.
Integration of 2D Black Phosphorus Phototransistor and Silicon Photonics Waveguide System Towards Mid-Infrared On-Chip Sensing Applications, L. Huang, B. Dong, X. Guo*, Y. Chang, N. Chen, X. Huang, H. Wang*, C. Lee, K-W. Ang, National University of Singapore, *Nanyang Technological University

T15-4- 11:20 a.m.
Next-Generation Fundus Camera with Full Color Image Acquisition in 0-lx Visible Light by 1.12-micron Square Pixel, 4K, 30-fps BSI CMOS Image Sensor with Advanced NIR Multi-Spectral Imaging System, H. Sumi*,**, T. Takehara**, S. Miyazaki**, D. Shirahige**, K. Sasagawa**, T. Tokuda**, Y. Watanabe*, N. Kishi*, J. Ohta**, M. Ishikawa*, *The University of Tokyo, **NAIST

T15-5- 11:45 a.m.
InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance, C. B. Zota, C. Convertino, V. Deshpande, T. Merkle*, M. Sousa, D. Caimi, L. Czornomaz, IBM Research, *Fraunhofer IAF

Session T16 – TAPA 2
Joint Focus Session: In Memory and In Sensor Computing

Thursday, June 21, 10:05 a.m.

Co-Chairs: S. Song, Qualcomm, Inc.
H. Miyake, Micron Memory Japan, Inc.

T16-1- 10:05 a.m.
Neuromorphic Technology Based on Charge Storage Memory Devices (Invited), J-H. Lee, Seoul National University

T16-2- 10:30 a.m.
Nonvolatile Circuit-Device Interaction for Memory, Logic and AI (Invited), M-F. Chang, National Tsing Hua University

T16-3- 10:55 a.m.
XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks, Z. Jiang, S. Yin*, M. Seok, J-S. Seo*, Columbia University, *Arizona State University

T16-4- 11:20 a.m.
A 4M Synapses Integrated Analog ReRAM Based 66.5 TOPS/W Neural-Network Processor with Cell Current Controlled Writing and Flexible Network Architecture, R. Mochida, K. Kouno, Y. Hayata, M. Nakayama, T. Ono, H. Suwa, R. Yasuhara, K. Katayama, T. Mikawa, Y. Gohou, Panasonic Semiconductor Solutions Co., Ltd.

T16-5- 11:45 a.m.
A Novel 3D AND-Type NVM Architecture Capable of High-Density, Low-Power In-Memory Sum-of-Product Computation for Artificial Intelligence Application, H-T. Lue, W. Chen, H-S. Chang, K-C. Wang, C-Y. Lu, Macronix International Co., Ltd.

12:10 p.m. Lunch Break

Session T17 – TAPA 3
STT MRAM

Thursday, June 21, 1:50 p.m.

Co-Chairs: G. Hemink, Western Digital
S. Chung, National Chiao Tung Univ.

T17-1- 1:50 p.m.
Embedded STT-MRAM in 28 nm FDSOI Logic Process for Industrial MCU/IoT Application, Y. K. Lee, Y. Song*, J. Kim, S. Oh*, B-J. Bae*, S. Lee, J. Lee*, U. Pi*, B. Seo, H. Jung*, K. Lee*, H. Shin*, H. Jung, M. Pyo, A. Antonyan, D. Lee, S. Hwang, D. Jang, Y. Ji, S. Lee, J. Lim, K-H. Koh*, K. Hwang*, H. Hong*, K. Park, G. Jeong, J. S. Yoon, E. S. Jung, Faundry Business Samsung Electronics Co., *R&D Center Samsung Electronics Co.

T17-2- 2:15 p.m.
22 nm FDSOI Embedded MRAM with Full Solder Reflow Compatibility and Enhanced Magnetic Immunity, K. Lee, K. Yamane, S. Noh, V. B. Naik, H. Yang , S. H. Jang, J. Kwon, B. Behin-Aein, R. Chao, J. H.

Lim, S. K., K. W. Gan, D. Zeng, N. Thiyagarajah, L. C. Goh, B. Liu, E. H. Toh, B. Jung, T. L. Wee, T. Ling, T. H. Chan, N. L. Chung, J. W. Ting, S. Lakshmipathi, J. S. Son, J. Hwang, L. Zhang, R. Low, R. Krishnan, T. Kitamura, Y. S. You, C. S. Seet, H. Chong, D. Shum, J. Wong, S. T. Woo, J. Lam, E. Quek, A. See, S. Y. Siah, GLOBALFOUNDRIES Singapore

T17-3- 2:40 p.m.
Low RA Magnetic Tunnel Junction Arrays in Conjunction with Low Switching Current and High Breakdown Voltage for STT-MRAM at 10 nm and Beyond, C. Park, H. Lee, C. Ching*, J. Ahn*, R. Wang*, M. Pakala*, S. H. Kang, Qualcomm Technologies, Inc., *Applied Materials, Inc.

T17-4- 3:05 p.m.
Rare-Failure Oriented STT-MRAM Technology Optimization, N. Xu, F. Chen, D. Apalkov, W. Qi, J. Wang, Z. Jiang, W. Choi, D. S. Kim*, Samsung Semiconductor Inc., *Semiconductor R&D Center Samsung Electronics

Session T18 – TAPA 2
Process and Material Technologies 3
Thursday, June 21, 1:50 p.m.

Co-Chairs: J. Chen, AMD
S. Takagi, The University of Tokyo

T18-1- 1:50 p.m.
Significant Performance Enhancement of UTB GeOI pMOSFETs by Advanced Channel Formation Technologies, W. H. Chang, T. Irisawa, H. Ishii, H. Hattori, N. Uchida, T. Maeda, National Institute of Advanced Industrial Science and Technology (AIST)

T18-2- 2:15 p.m.
First Demonstration of Vertically-Stacked Gate-All-Around Highly Strained Germanium Nanowire p-FETs, E. Capogreco, L. Witters, H. Arimura, F. Sebaai, C. Porret, A. Hikavyy, R. Loo, A. P. Milenin, G. Eneman, P. Favia, H. Bender, K. Wostyn, E. Dentoni Litta, A. Schulze, C. Vrancken, A. Opdebeeck, J. Mitard, R. Langer, F. Holsteyns, N. Waldron, K. Barla, V. De Heyn, D. Mocuta, N. Collaert, imec

T18-3- 2:40 p.m.
Hole Mobility Enhancement in Extremely-Thin-Body Strained GOI and SGOI pMOSFETs by Improved Ge Condensation Method, K-W. Jo, W-K. Kim, M. Takenaka, S. Takagi, The University of Tokyo

T18-4- 3:05 p.m.
GeSn p-FinFETs with Sub-10 nm Fin Width Realized on a 200 mm GeSnOI Substrate: Lowest SS of 63 mV/decade, Highest Gm,int of 900 µS/µm, and High-Field µeff of 275 cm2/V·s, D. Lei, K. Han, K. H. Lee*, Y-C. Huang**, W. Wang, S. Yadav, A. Kumar, Y. Wu, H. Heliu, S. Xu, Y. Kang, Y. Li, E. Y-J. Kong, C. S. Tan*, X. Gong, National University of Singapore, *Nanyang Technological University, **Applied Materials, Inc.

3:30 p.m. Break

Session T19 – TAPA 3

3D Vertical and Stackable NVM
Thursday, June 21, 3:45 p.m.

Co-Chairs: N. Ramaswamy, Micron
H-T. Lue, Macronix International Co., Ltd.

T19-1- 3:45 p.m.
Space Program Scheme for 3D NAND Flash Memory Specialized for the TLC Design, H-J. Kang, N. Choi, D. H. Lee*, T. Lee*, S. Chung*, J-H. Bae, B-G. Park, J-H. Lee, Seoul National University, *R&D Division SK Hynix, Inc.

T19-2- 4:10 p.m.
First Demonstration of Monocrystalline Silicon Macaroni Channel for 3D NAND Memory Devices, R. Delhougne, A. Arreghini, E. Rosseel, A. Hikavyy, E. Vecchio, L. Zhang, M. Pak, L. Nyns, T. Raymaekers, N. Jossart, L. Breuil, S. S. V-Palayam, C-L. Tan, G. Van den Bosch, A. Furnémont, imec

T19-3- 4:35 p.m.
High Endurance Self-Heating OTS-PCM Pillar Cell for 3D Stackable Memory, C. W. Yeh, W. C. Chien, R. L. Bruce*, H. Y. Cheng, I. T. Kuo, C. H. Yang, A. Ray*, H. Miyazoe*, W. Kim*, F. Carta*, E. K. Lai, M. BrightSky*, H. L. Lung, Macronix International Co., Ltd., *IBM T. J. Watson Research Center

T19-4- 5:00 p.m.
Te-Based Binary OTS Selectors with Excellent Selectivity (>10^5), Endurance (>10^8) and Thermal Stability (>450 °C), J. Yoo, Y. Koo, S. A. Chekol, J. Park, J. Song, H. Hwang, POSTECH

T19-5- 5:25 p.m.
Half-Threshold Bias I_{off} Reduction Down to nA Range of Thermally and Electrically Stable High-Performance Integrated OTS Selector, Obtained by Se Enrichment and N-doping of Thin GeSe Layers, N. S. Avasarala, G. L. Donadio, T. Witters, K. Opsomer, B. Govoreanu, A. Fantini, S. Clima, H. Oh, S. Kundu, W. Devulder, M. H. Van der Veen, J. Van Houdt, M. Heyns, L. Goux, G. S. Kar, imec

Session T20 – TAPA 2
CMOS Platform and Technology
Thursday, June 21, 3:45 a.m.

Co-Chairs: W. Rachmady, Intel Corp.
Y. Yeo, Taiwan Semiconductor Manufacturing Co.

T20-1- 3:45 p.m.
Highly Manufacturable Low Power and High Performance 11LPP Platform Technology for Mobile and GPU Applications, H-J. Kim, B. H. Choi, Y. H. Lee, J. H. Ahn, Y. S. Bang, Y. D. Lim, J. H. Do, J. H. Jung, T. J. Song, Y. Yasuda-Masuoka, K. C. Park, S. D. Kwon, J. S. Yoon, Foundry Division Samsung Electronics

T20-2- 4:10 p.m.
A 12 nm FinFET Technology Featuring 2nd Generation FinFET for Low Power and High Performance Applications, H. C. Lo, D. Choi, Y. Hu, Y. Shen, Y. Qi, J. Peng, D. Zhou, M. Mohan, C. Yong, H. Zhan, H. Wei, X. He, D. Kang, A. Sirman, Y. Wang, H. Zang, S. Y. Mun, A. Vinslava, W. H. Chen, C. Gaire, J. Liu, X.

Dou, Y. Shi, P. Zhao, B. Zhu, A. Jha, X. Zhang, X. Wan, E. Lavigne, C. Kyono, M. Togo, J. Versaggi, H. Yu, O. Hu, J. G. Lee, S. B. Samavedam, D. K. Sohn, GLOBALFOUNDRIES Malta

T20-3- 4:35 p.m.
8LPP Logic Platform Technology for Cost-Effective High Volume Manufacturing, H. Rhee, I. Kim, J. Jeong, N. Son, H. Hong, S. Cho, Y. Park, D. Kim, Y. Choi, J. Ahn, S. G. Kang, K. Yeo, J. Kim, E. Lee, J. M. Youn, J. S. Yoon, Foundry Division Samsung Electronics

T20-4- 5:00 p.m.
High Performance Mobile SoC Productization with 2nd Generation 10 nm FinFET Technology and Extension to 8 nm Scaling, J. Yuan, K. Rim, Y. Chen, M. Cai, Y. Suh, J. Choi, J. Deng, J. Bao, Z. Song, L. Ge, H. Wang, X-Y. Wang, V. Lin, C. Kuo, S. Yang, A. Rabindranath, S. Siva, P. Bhadri, S. Kim, K. Lee, S. Cho, S. Kang, S. Oh, S. D. Kwon, X. Chen, P. Penzes, P. Agashe, W. Miller, P. R. Chidambaram, Qualcomm Technologies, Inc.

T20-5- 5:25 p.m.
Hybrid 14 nm FinFET - Silicon Photonics Technology for Low-Power Tb/s/mm2 Optical I/O, M. Rakowski, Y. Ban, P. De Heyn, N. Pantano, B. Snyder, S. Balakrishnan, S. Van Huylenbroeck, L. Bogaerts, C. Demeurisse, F. Inoue, K. Rebibis, P. Nolmans, X. Sun, P. Bex, A. Srinivasan, J. De Coster, S. Lardenois, A. Miller, P. Absil, P. Verheyen, D. Velenis, M. Pantouvaki, J. Van Campenhout, imec