A Low-Swing Clock Double-Edge Triggered Flip-Flop

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Abstract

A low-swing clock double-edge triggered flip-flop (LSDFF) is developed to reduce power consumption significantly compared to conventional FFs. LSDFF avoids unnecessary internal node transition and reduce fighting currents. The overall power saving in flip-flop operation is estimated to be 30.2 to 50.8% with additional 78% power savings in clock network.