

On-die Clock Jitter Detector for High Speed Microprocessors

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This paper describes an on-die clock jitter detector for high-speed microprocessor circuits. The detector can measure variation in clock high/low time or period. Innovative circuit techniques are used to provide fast initial DLL lock, adaptive filtering, granular jitter computation, and enhanced immunity to power-supply noise. It compares individual clock cycles to the average clock period, reporting the differences. The system has multiple output modes to allow more complete understanding of the jitter distribution and time dependence.