Quasi-Worst-Condition Built-In-Self-Test Scheme for 4-Mb Loadless CMOS Four-Transistor SRAM Macro

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We have developed a quasi-worst-condition Built-In-Self-Test (BIST) scheme capable of detecting defective cells. The effectiveness of the BIST, which is conducted at the time of power supply injection, is independent of ambient temperature. Measurement results indicate that defective cells detected in a wafer functional test in worst condition would also be detected with our newly developed BIST.