Robustness of sub-70nm Dynamic Circuits: Analytical Techniques and Scaling Trends

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Abstract

We present an accurate (to within 3%, across two process generations), three parameter, closed form, time-domain technique for evaluating the noise response of domino circuits. We evaluate the robustness of scaled topologies to show that conventional domino circuits will cease to be useful around the 70nm generation. The paper concludes with possible device/circuit approaches to extend domino circuit usefulness.