

An Area-Efficient 2GB/s 256Mb Packet-based DRAM with Daisy-Chained Redundancy Scheme

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Abstracts

An area-efficient packet-based 256Mb DRAM with a 4 bank architecture and a peak bandwidth of 1.0Gbps/pin at $V_{cc}=2.35V$, $Temp=100^{\circ}C$ is developed. This chip features a daisy chained redundancy scheme, an area-efficient logic block placement and routing technique and a process insensitive DLL with duty error reduction scheme to overcome large chip size penalty and to improve chip yield.