Experimental and Simulation Study on Sub-50 nm CMOS Design

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Abstract

CMOS devices with gate length down to sub-50 nm were fabricated using poly-Si gate with notches and conventional gate structure. It was shown that optimal halo as compared to conventional gate is achieved when tilted implant is performed using gate with notches. Due to optimal halo placement, for the same extension implant up to 7% improvement in drain current for p-MOS and 15% improvement for n-MOS and simultaneously 20 nm improvement in threshold voltage roll-off were observed for notched gate devices.