A Process Variation Compensating Technique for Sub-90nm Dynamic Circuits

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Abstract

A process variation compensating technique for dynamic circuits is described for sub-90nm technologies where leakage variation is severe. A keeper whose effective strength is optimally programmable based on die leakage enables 10% faster performance, 35% reduction in delay variation, and 5x reduction in robustness failing dies over conventional static keeper design in 90nm dual-V_t CMOS.