A 90nm 1GHz 22mW 16x16-bit 2's Complement Multiplier for Wireless Baseband

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This paper describes a static 16x16-bit 2's complement wireless baseband multiplier testchip in 1.2V, 90nm dual-Vt CMOS technology. One-hot Booth encoding, sum/delay difference optimized 3:2 compressor tree, and signal-profile optimized final adder schemes are employed to achieve 1GHz, 22mW operation at 1.2V, scalable to 500MHz, 3mW at 0.8V.