A Low Cost High Performance Register-Controlled Digital DLL for 1Gbps x32 DDR SDRAM

Jong-Tae Kwak, Chang-Ki Kwon, Kwan-Weon Kim, Seong-Hoon Lee, Joong-Sik Kih
Memory R&D Division, Hynix Semiconductor Inc., Ichon, Kyoungki, Korea

A low cost high performance register-controlled digital delay-locked loop (DLL) that has novel resolution-enhancing structure with inherent duty cycle correction capability was developed for 1Gbps x32 DDR SDRAM. Experimental results in a 0.13um 4Mx32 DDR SDRAM show <25ps peak-to-peak jitter with quiet supply, <±2% duty correction from external duty error of ±7%, <150cycle lock-time, 24mW at 1.8V/400MHz, 60mW at 2.5V/500MHz, and a wide locking range from 66MHz to over 500MHz.