

# **A Post-Silicon Clock Timing Adjustment Using Genetic Algorithms**

Abstract

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A post-silicon clock timing adjustment architecture utilizing genetic algorithms (GA) is proposed, which has three advantages: (1) enhanced clock frequency leading to improved operating yields, (2) lower power supply voltages while maintaining operating yield, and (3) reductions in design times. Experiments with two different developed LSI chips and a design experiment demonstrated these advantages with a clock frequency enhancement of 25% (max), a power supply voltage reduction of 33%, and 21% shorter design times.