A Cost-Efficient Dynamic Ternary CAM in 130nm CMOS Technology with Planar Complementary Capacitors and TSR Architecture

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Abstract

A novel dynamic Ternary-CAM (TCAM) architecture with transparently scheduled refresh, address-input-free writing and planar complementary capacitors is proposed. The planar dynamic concept allows small TCAM cell size of 4.79um2 in a 130nm CMOS technology that is about half of the static TCAM cell size, and the complementary capacitors improve the stability of conventional-DRAM-based TCAM cells. Transparently scheduled refresh and address-input-free writing make the proposed TCAM especially attractive for classifying applications in network routers.