ArF Lithography Technologies for 65nm-node CMOS (CMOS5) with 30nm Logic Gate and High Density Embedded Memories

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Abstract

This paper presents ArF lithography technologies for 65nm-node CMOS with 30nm logic gate and high density embedded memories. The technologies consist of two major concepts. One is the approach to narrow lithography process window. Since ArF step-and-scan exposure systems with 0.75NA are implemented to all critical layers, the accurate lithography design for low k_1 lithography is needed. The other is gate fabrication process which includes both 30nm logic gates and high density embedded memory cells. For this achievement, special process steps are implemented with two kinds of lithography.