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Abstract

2-1 A 50.3ns Transient-Response CR-Free SIMO Power Converter with Adaptive Current Compensation

A fast-transient, cross-regulation-free, single-inductor multiple-output (SIMO) power converter is proposed. To overcome the inherent drawback of slow load transient response, it employs an adaptive current compensation technique and linear-assisted SIMO architecture, achieving 50.3ns transient response to 270mW load change at 500kHz switching frequency and with 0.35um CMOS process. The efficiency reaches the peak of 82.8% at 102mW and stays above 70% over the entire 300mW power range.

2-2 A 98% Cross-Talk Self-Cancellation Single-Inductor Dual-Output DC-DC Converter Using Bidirectional Power Prediction (BPP) Control in 65nm CMOS

98% cross-talk self-cancellation is achieved by the bidirectional power prediction (BPP) control in the proposed single-inductor dual-output (SIDO) converter. The frequency-controlled resistor based on the switched-capacitor (SC) structure determines the energy correlation scheme between dual outputs. The embedded rough and fine energy trackers in the BPP controller guarantee accurate cross-talk cancellation according to both output voltages and currents. The fabricated chip occupies 1.28 mm^2 in 65nm CMOS and achieves 90% peak efficiency.

2-3 A Single-Inductor 8-channel Output DC-DC Boost Converter with Time-limited One-shot Current Control and Single Shared Hysteresis Comparator

This paper describes a time-limited one-shot current control technique used to extend the outputs of a single-inductor multiple-output DC-DC converter without stability and complexity issues. The proposed scheme also reliably supports many outputs with unbalanced loads. True all-comparator control is realized with a single shared hysteresis comparator and a fixed switching frequency of 800-kHz. The maximum efficiency reaches 92%. The fabricated chip possessing 8-channel outputs occupies 2.4²2.1 mm^2 in a 0.35-um CMOS process.

2-4 Fixed-Frequency Adaptive-On-Time Boost Converter with Fast Transient Response and Light Load Efficiency Enhancement by Auto-Frequency-Hopping

An integrated fixed-frequency adaptive on time DC-DC converter with fast transient response and high light load efficiency is presented. To achieve fixed frequency at continuous conduction mode, the on time is adaptively controlled to force the switching frequency tracks the reference frequency with less than +/-0.5% error within the whole operating range. To enhance the light load efficiency as well as reduce EMI noise problem, the on time is adjusted to maintain the switching frequency hops between 1MHz and 1MHz/N where $N = 2^i$ and i = 1 to 5 according to the loads without load current sensor.

2-5 A Spurious-Free Switching Buck Converter Using a Delta-Sigma Modulation Controller with a Scalable Sampling Frequency

This switching DC-DC buck converter uses a delta-sigma-modulator controller with a scalable sampling frequency, in order to eliminate the spurs and minimize the noise floor at its output without sacrificing the power efficiency. Fabricated in 0.13-um digital CMOS, it achieves a spurious-free output with voltage ripples below 70mV over the full loading range (2mA to 800mA). Furthermore, its power efficiency is higher than 72% over this range, with 96% peak efficiency.

3-1 A 0.38THz Fully Integrated Transceiver Utilizing Quadrature Push-Push Circuitry

The first fully integrated transceiver operating at 0.38THz has been demonstrated in 0.13um SiGe BiCMOS with f_T=150GHz. Quadrature push-push circuitry using transformer-coupled stages and Coplanar Strip (CPS) lines are used to realize a terahertz (THz) subharmonic mixer, a quadrature generator, and a quadrupler from a strong fundamental LO quardature signal generated at the W-band. The measured Equivalent Isotropically Radiated Power (EIRP) is -13dBm and the noise figure (NF) is 35dB, while dissipating a power of 364mW.

3-2 A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS

This paper presents a low-power adaptive 60GHz baseband in 65nm CMOS. The design integrates variable gain amplifiers, analog phase rotator, 40-coefficient I/Q decision feedback equalizers (DFEs), clock generation and data recovery circuits, and adaptation hardware. The baseband achieves 10Gb/s while consuming 53mW (DFE adaptation on)/45mW (DFE adaptation off), representing ~10X improvement in data-rate and power efficiency over prior art.

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3-3 A 2.5GHz Delay-based Wideband OFDM Outphasing Modulator in 45nm-LP CMOS

A 2.5 GHz delay-based CMOS outphasing transmitter for wideband OFDM is presented in 45nm LP CMOS. It dynamically delays LO edges to modulate the phase of two outphasing signals. A Tapped-Delay-Line coarse delay modulator allows delay modulation at the LO rate with no glitches. This is used to implement a 11-bit sigma-delta dithered theta modulator with phase-domain filtering, and a 9-bit open-loop phi modulator. The system meets EVM and ACPR requirements for 802.11g at 2.5GHz.

3-4 A Configurable Multi-band Multi-mode Transmitter with Spur Cancellation through Digital Baseband

A 65nm CMOS configurable transmitter with spur cancellation scheme is presented. Over 10dB spur cancellation is achieved by applying a digital sideband signal at Tx DAC input. The transmitter covers bands from 410 to 2700MHz and supports 2G, 3G and 4G. ACLR is -43dBc at 8dBm and receiver band noise is -160.7dBc/Hz at 4dBm. It consumes 32mW at -8dBm for WCDMA IMT band in SAW-less mode.

3-5 A 3.5mm^2, Inductor-less Digital-intensive Radio SoC for 300-to-950MHz ISM-band Applications Supporting 1.0-to-240kbps Multi-data-rates

A small-sized (less than 2mm^2 total analog and radio area) sub-GHz radio SoC for low power and low data-rate wireless applications is presented. The SoC has been equipped with a low-power analog-to-digital conversion scheme having a variable over-sampling ratio, multi-sampling-rate channel select filtering, and inductor-less RF front-end circuits incorporating a high output power stair-like shaping CMOS power-amplifier with a duty-imbalance-compensated level-shifter. The SoC, fabricated with 90nm CMOS, occupies only 3.5mm^2. It has a sensitivity of -118dBm in a 2.4kbps FSK mode for a 433MHz band, and channel selectivity for data rates ranging from 1.0 to 240kbps.

4-1 A 12-ENOB 6X-OSR Noise-Shaped Pipelined ADC Utilizing a 9-bit Linear Front-End

A noise-shaped pipelined ADC is presented in this paper. A minimal complexity Delta-Sigma modulator in the first two sub-ADCs and residue feedback in the
latter stages lead to high-order noise shaping. This also leads to reduced sensitivity to analog imperfections in the front-end stage. Implemented in 0.18um CMOS, the ADC achieves 12~ENOB with 64~MHz clock at 6X~OSR.

4-2 A 32nm, 1.05V, BIST enabled, 10-40MHz, 11-9 bit, 0.13mm^2 Digitized Integrator MASH DS A/D Converter

A 11-9 bit, 10-40MHz DS A/D converter with a digitized integrator (DI) MASH structure with a low swing feed-forward architecture to allow for scalable, portable, and reconfigurable ADC in 32nm CMOS process using all minimum channel length transistors. An on-chip SNR calculator allows high volume sort testing on a digital tester; startup automatic offset and reference calibration to prevent integrator overload due to manufacturing variations, and compensation for finite opamp gain.

4-3 A Continuous-Time, Jitter Insensitive Sigma Delta Modulator Using a Digitally Linearized G_m-C Integrator with Embedded SC Feedback DAC

This paper explores the use of a digitally linearized, low-power Gm-C integrator in the first stage of a 5th order CT sigma-delta modulator. The proposed architecture features a jitter insensitive SC feedback and a noisy-but-linear auxiliary modulator to estimate the nonlinearities of the first integrator in the main signal path. A 65-nm CMOS experimental prototype achieves 79 dB DR, and 73.3 dB peak SNDR for bandwidth of 1.95 MHz consuming 8.55 mW.

4-4 A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass Delta-Sigma ADC for RF Digitization with Integrated PLL and Polyphase Decimation Filter in 40nm CMOS

A 2.22GHz 4th-order BP DeltaSigma ADC has been realized in 40nm CMOS. The test chip contains a complete system consisting of the ADC core, the PLL with clock generation network, and the digital decimation filters and downconversion (DFD). The quantizers are 6 times interleaved enabling a polyphase structure for the DFD and relaxing speed requirements. Sampled at 8.88GS/s the ADC achieves a DR of 48dB in a band of 80MHz with an IIP3 of +1dBm.

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4-5 A 2.8 mW Delta-Sigma ADC with 83 dB DR and 1.92 MHz BW Using FIR Outer Feedback and TIA-Based Integrator

A low-power continuous-time Delta-Sigma ADC for HSDPA (High-Speed Downlink Packet Access) applications provides 83 dB dynamic range and 1.92 MHz bandwidth. A high sample rate (245.76 MHz) and an FIR filter in the outer feedback path minimize susceptibility to jitter. A TIA-based integrator with direct connection of inner feedback DAC current sources to integration capacitors supports the high sample rate. The modulator, implemented using 40 nm CMOS, dissipates only 2.8 mW and achieves a 110 fJ / conversion step figure-of-merit.

5-1 Measurement, Analysis and Improvement of Supply Noise in 3D ICs

Supply noise measurements from a 3D IC have been presented for the first time. IR noise rather than Ldi/dt noise is shown to be dominant due to the fewer supply pins and the additional resistance from the through-silicon vias (TSVs). Kelvin probing for IR noise reveals that the effect of pins is significantly more than TSVs. A novel multi-story power delivery is demonstrated for a 393kb SRAM suppressing the IR noise by 30-70%.

5-2 Isolation Techniques against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) for RF/Mixed-Signal SoCs

Isolation techniques against substrate noise coupling utilizing TSV processes are proposed. The TSV encloses the RF circuit on a SoC chip to improve the isolation between digital circuits and the RF circuit without constraints of on-chip interconnect above the TSV. Various test patterns are fabricated on a CMOS 10ohm-cm silicon substrate. The combinational pattern with TSV, DTI and HR layer shows 60dB improvement of the isolation. Both simplified model and mesh equivalent model are well matched with measurement results.

5-3 A Fully-integrated Cantilever-based DNA Detection SoC in a CMOS Bio-MEMS Process

A highly-integrated DNA detection SoC, which includes DNA sensors, readout circuit, MCU, and OOK TX/RX, is implemented in a 0.35um CMOS Bio-MEMS process. An oscillator-based self-calibrated readout circuit with high sensitivity (2kHz/ohm) is proposed to convert small resistance variation of the piezoresistive cantilever sensor into adequate frequency shift. The measured results reveal that it could detect <0.02% of resistance variation (0.6ohm) and cover detection concentration range of specific DNA from 100pM to 1uM.

5-4 A 65nm CMOS Movable Parts Manager for Optical Disc System

This paper describes a high-precision Movable Parts Manager (MPM) for BD/DVD applications. To realize the high precise optical pick-up control, the MPM employs a mixed-signal actuator driver (MiSiA) with direct voltage feedback method using simple 1st-order delta-sigma ADCs. It achieves high resolution of 1% linearity error and 0.2% DC error. The chip size of the MPM is 7.6mm^2 in 65nm CMOS processes. The MPM can be applied to next-generation high-density recording systems.

5-5 20-uW Operation of an a-IGZO TFT-based RFID Chip Using Purely NMOS "Active" Load Logic Gates with Ultra-Low-Consumption Power

We fabricated the first RFID chip using amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) on a glass substrate. Logic gates with low-consumption current (~1 nA) and steep on/off switching was also proposed. The logic circuit achieved small enough power consumption (20 uW) for wireless operation and a wireless operation of the RFID tag was demonstrated.

6-1 A 100dB DR Ground-Referenced Single-Ended Class-D Amplifier in 65nm CMOS

A ground-referenced Class-D headset amplifier combines digital PWM and analog PWRM schemes. The closed-loop analog driver includes a feed-forward path and a T-bridge power stage. The single-ended amplifier in 65nm CMOS achieves 100dB DR, 82dB PSRR and 80% efficiency with an integrated charge pump.

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6-2 A Ping-Pong-Pang Current-Feedback Instrumentation Amplifier with 0.04% Gain Error

A ping-pong-pang auto-zeroed and chopped current-feedback instrumentation amplifier (CFIA) uses three dynamically-matched input stages to achieve a gain error of 0.04%, a 2.5x improvement over prior art. Its 4uV offset and 28nV/sqrt(Hz) noise are achieved at 3.5x less supply current than a comparable ping-pong auto-zeroed CFIA.

6-3 A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz f_T BiCMOS Process

We describe a DAC which can operate at up to 7.2 GSa/s with 14-bit resolution or up to 12 GSa/s with 12-bit resolution. It uses a segmented architecture, with an R/2R ladder for the 10 LSBs; distributed resampling is applied to all current sources. The DAC achieves an SFDR of 77 dB at low output frequencies and an SFDR of 67 dB and an SNR of 62 dB from DC to 3 GHz. It demonstrates a phase noise of -157 dBc/Hz at 10 kHz from a 1 GHz carrier, 22 dB better than synthesized signal generation instruments.
The DAC is built in a 165-GHz f_T, 130-nm BiCMOS process and packaged in a 780-ball BGA.

6-4 A 3GS/s, 9b, 1.2V Single Supply, Pure Binary DAC with >50dB SFDR up to 1.5GHz in 65nm CMOS

A 9b 3GS/s pure binary current steering DAC is implemented in 65nm CMOS. It demonstrates a low noise CML latch and a low power delay balancing technique while drawing 50mA from a single 1.2V power supply. When sampling at 3GHz, it exhibits more than 50dB SFDR until 1.5GHz output frequency and less than -60dB IM3 up to 1GHz output frequency. Total silicon area is less than 0.04mm^2.

6-5 A 10b 600MS/s Multi-mode CMOS DAC for Multiple Nyquist Zone Operation

A 10b 600MS/s current-steering DAC, implemented in a 65nm CMOS process, realizes direct waveform synthesis for TV band cognitive radio applications. A multi-mode reconstruction technique enables the DAC to utilize the image spectrum in higher Nyquist zones for wideband direct synthesis. The measured SFDR is better than 55dB across the first three Nyquist zones at 600MS/s with 30mW of power dissipation.

7-1 A 40nm Fully Functional SRAM with BL Swing and WL Pulse Measurement Scheme

A method for direct measurements of bit-line (BL) swing, sense amplifier (SA) offset and word-line (WL) pulse width is demonstrated in a 40nm CMOS 32kb fully functional SRAM macro with <2% area penalty. This allows, for the first time, deciding the best tuning option for WL-pulse (WLP) width based on the results being measured on site for BL swing and dynamic read/write stability (DRWS), which depend on WLP width, as well. It has enabled to eliminate a need of additional margin for BL swing, which was conventionally needed for ensuring tolerance against its simulation errors and inaccurate SA-offset estimation. As a result, it was found that more aggressive option for WLP width could be chosen while ensuring the target BL swing.

7-2 A 40-nm 0.5-V 20.1-uW/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme

This paper presents a novel disturb mitigation scheme which achieves low-power and low-voltage operation for a deep sub-micron SRAM macro. We fabricated a 512-Kb 8T SRAM test chip that operates at a single 0.5-V supply voltage. The proposed scheme achieves 8.8-uW/MHz active energy in a write cycle and 72.8-uW leakage power, which are 35% and 26% better than the conventional write-back scheme. The total energy is 20.1 uW/MHz at 0.5 V.

7-3 A Larger Stacked Layer Number Scalable TSV-based 3D-SRAM for High-Performance Universal-Memory-Capacity 3D-IC Platforms

This work demonstrates the first fabricated TSV-based die-to-die bonding stacked-layer-number-scalable 3D-SRAM macro. This 3D-SRAM uses a semi-master-slave (SMS) structure and a self-timed differential-TSV signal transfer (SDST) scheme to 1) provide a constant-load logic-SRAM interface across various layer configurations; 2) suppress TSV-induced power and speed overheads; 3) tolerate die-to-die variation, and 4) enable pre-bonding KGD sorting, to improve the speed and yield of universal-memory-capacity platforms. Superior scalability of increasing stacked layer number with small speed overheads is demonstrated in the fabricated 3D-SRAM macro with layer-scalable test-modes. This macro has two SRAM layers that are stacked by a via-last process with die-to-die bonding.

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7-4 A Chip-ID Generating Circuit for Dependable LSI Using Random Address Errors on Embedded SRAM and On-Chip Memory BIST

A chip-ID generating scheme with high-tamper resistance is proposed. This enables to extract a unique finger print from each chip by using random failure bits in an SRAM under the ID generation mode, and on-chip memory BIST. The stability and average of Humming distance of 128 bit ID become 99.9999999% and 63.9, respectively. The proposed scheme does not require any additional hardware IPs.

8-1 An 8x10-Gb/s Source-Synchronous I/O System Based on High-Density Silicon Carrier Interconnects

A serial I/O chip set in 45nm SOI CMOS is mounted via 50um pitch micro-C4 bumps to a silicon carrier and communicates over ultra-dense interconnects with pitches of between 8um and 22um. With DFE-IIR RX equalization, data is received over distances up to 6cm with channel losses as high as 16.3dB. The energy efficiency is better than 6.1pJ/bit.

8-2 A 5.6Gb/s 2.4mW/Gb/s Bidirectional Link With 8ns Power-On

A fast power-on low-power signaling system was developed and fabricated in TSMC's 40nm LP process. The system uses matched source-synchronous clocking (MSSC), fast power-on bias, a rapid-turn on 4x multiplying ILO, and CML clock distribution to achieve 2.5-5.6Gb/s/lane and 8ns turn on at 2.4mW/Gb/s per link across a 6-lane parallel interface. First-edge clock jitter is minimized by using matching equalizers in the clock and data paths. PSN is reduced by using a staggered bias turn-on.

8-3 An 8Gb/s Forwarded-Clock I/O Receiver with up to 1GHz Constant Jitter Tracking Bandwidth Using a Weak Injection-Locked Oscillator in 0.13um CMOS

This paper presents a forwarded-clock I/O receiver with wide range constant jitter tracking bandwidth (JTB). A JTB interpolator in the receiver enables wide JTB using a weak injection-locked oscillator (ILO) instead of a strong ILO, so narrow VCO tuning is also possible. By using the JTB interpolator, the proposed receiver compensates for the JTB reduction caused by deskew-JTB dependency in conventional ILOs. An 8Gb/s receiver has been implemented to verify 70M~1GHz constant JTB and one UI deskew with only 1.94~2GHz VCO tuning. The 0.13um test chip consumes 17.2~21.4mW and occupies 0.04mm^2.

8-4 A 0.12mm^2 5Gbps Reciever with a Level Shifting Equalizer and a Cumulative-Histogram-Based Adaptation Engine

A 0.12mm^2 5Gbps receiver with an adaptive equalizer was presented. To minimize the equalizer area, a source-input front-end performing level shift and equalization is proposed. An adaptation algorithm finds an optimal equalizer setting by observing the cumulative histogram of the equalizer-output amplitude, reducing the hardware cost. A test chip was fabricated in a 65-nm CMOS. It achieved the equalization of 20dB transmission loss with a BER less than 10^{-12} while consuming 33mW at 1.2V.

9-1 A Digital CDS Scheme on Fully Column-Inline TDC Architecture for An APS-C Format CMOS Image Sensor

This paper proposes a digital correlate double sampling (CDS) scheme which is suitable for a column-inline time to digital converter (TDC). The column-parallel TDCs, where measurements are made with a counter and delay line interpolation, achieve high speed A/D conversion without decreasing resolution. An APS-C format image sensor with 12-bit 360 Mpixel/s readout is realized in a cost-effective 0.18-um CMOS technology.

9-2 A 640x480 Image Sensor with Unified Pixel Architecture for 2D/3D Imaging in 0.11um CMOS

A 3D image sensor is presented employing a time multiplexed concept for color and depth image acquisition in a single chip to generate a real-time 3D image of an arbitrary scene. The pixel adopts a split photodiode to demodulate time-of-flight signals effectively. Every four pixels share two storages and readout transistors to utilize 100% of photons and increase the sensitivity of infrared light by simple binning operation at the expense of resolution. With the fabricated prototype sensor, 640x480 color and depth images of the scenes 1-3m away are captured with an accuracy of 1-6cm.

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9-3 A Dual In-Pixel Memory CMOS Image Sensor for Computation Photography

We present a new image sensor to help applications like high-dynamic range, structured illumination, motion corrected photography, etc. by providing two analog memories in each pixel. Clever pixel design allowed us to create the smallest pixel size and the largest fill factor for this class of imager, while supporting dual global shutter operation and true correlated double sampling (CDS) readout from both in-pixel memories to cancel kTC noise.

9-4 A CMOS $\Sigma-\Delta$ Photodetector Array for Bioluminescence-Based DNA Sequencing

A fully-integrated photodetector array for long-read length bioluminescence-based DNA sequence-by-synthesis is implemented. Each pixel has 120dB photocurrent detection dynamic range and includes a 10fA-10nA pulse frequency modulation (PFM) background subtraction block and a 1st-order $\Sigma-\Delta$ modulator.

11-1 A Low Spur Fractional-N Digital PLL for 802.11 a/b/g/n/ac with 0.19 psrms Jitter

A 5.9-to-8.0 GHz fractional-N digital PLL with TDC histogram calibration, reference doubler compensation and non-periodic DCO dithering is implemented in 55nm CMOS. With reference doubled from 40 MHz, the rms jitter integrated from 1kHz to 10MHz is 0.19ps or 0.4 deg for a 5825 MHz clock measured at TX output, and the in-band noise floor is -108 dBc/Hz. The reference and worst-case fractional spurs are -94dBc and -70dBc, respectively, and it draws 36mW.

11-2 A -104dBc/Hz In-Band Phase Noise 3GHz All Digital PLL with Phase Interpolation Based Hierarchical Time to Digital Convertor

An ADPLL which uses a time-to-digital convertor with <0.13rad resolution achieves LO generation at 3GHz with -104dBc/Hz in-band phase noise. The fine and stable resolution is derived by known phase interpolation circuits. It is fabricated in a 65nm CMOS process and the active area is 0.18mm^2.

11-3 A 3.6GHz 1MHz-Bandwidth delta-sigma Fractional-N PLL with a Quantization-Noise Shifting Architecture in 0.18um CMOS

This paper presents a 3.6GHz fractional-N phase-locked loop (FNPLL) with a quantization-noise shifting (QNS) architecture. The proposed design decreases the amount of the quantization error while effectively increases the modulating frequency; hence, shifting the quantization noise to higher frequency and lower level. Fabricated in a 0.18um CMOS, the FNPLL achieves -120dBc/Hz at 3MHz offset, with a bandwidth of 1MHz. Measurement results show up to 30dB improvement on quantization noise when QNS mode is activated.

11-4 A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping Delta-Sigma TDC

A 2 GHz fractional-N digital PLL with a single delay cell, noise shaping delta-sigma TDC is implemented in a 0.13um CMOS. With a simple structure of delta modulator followed by a charge pump integrator, a wide range TDC input is converted to delta-sigma modulated bit stream. The implemented TDC consumes 1 mA, and the DPLL shows the in-band phase noise of -107 dBc at 500 kHz offset.

12-1 A 12b 3GS/s Pipeline ADC with 500mW and 0.4 mm^2 in 40nm Digital CMOS

A 12b 3GS/s 2-way interleaved pipeline ADC is presented. To achieve high speed, multiple internally generated power/ground rails are used with thin-oxide MOS devices. The ADC achieves a SNR of 61dB and a DNL of -0.4/+0.6LSB, consumes 500mW at 3GS/s and occupies 0.4 mm^2 area in 40nm CMOS process.

12-2 An 11b 300MS/s 0.24pJ/Conversion-Step Double-Sampling Pipelined ADC with On-chip Full Digital Calibration for All Nonidealities Including Memory Effects

An 11b Double-Sampling Pipelined ADC with memory effect calibration is presented. The full digital calibration simplifies the analog circuit, which extends the operation speed over 300MHz. The chip is fabricated in a 40nm CMOS and occupies 0.42mm^2 including the calibration logics. The ADC consumes 40mW from a 1.8V supply, and the FoM is 0.24pJ/conversion-step.

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12-3 A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-bit/stage Folding Converter Architecture

We have developed a 7-b 1.3-GSa/s 1-bit/stage pipeline ADC with a folding characteristic that uses a polarity selecting technique. The ADC achieves an ENOB of 6.5-b and consumes only 22 mW from 1.2V supply. These results yield a figure of merit (FOM) of 190-fJ/conv.-step. It is implemented in 45-nm CMOS technology and occupies a core area of 0.023 mm^2.

12-4 A 10b 320 MS/s 40 mW Open-Loop Interpolated Pipeline ADC

An open-loop interpolated pipeline ADC is proposed. Weight controlled capacitor arrays are introduced to realize an interpolation and a pipelined operation with open-loop amplifiers. The 10-bit ADC fabricated in 90nm CMOS demonstrates ENOB of 8.5b over 80MHz bandwidth (BW) and a conversion rate of 320MS/s without linearity compensation and consumes 40mW. The FoMs are 780fJ/c.-s. defined by the 80MHz BW and 390fJ/c.-s. defined by the 320 MSps conversion rate with a BW of 80MHz.

12-5 A 16mW 8-bit 1-GS/s Subranging ADC in 55nm CMOS

A subranging ADC was fabricated using a 55nm CMOS technology. To improve speed, subranging is executed in the digital domain by activating comparators. To save power, comparators are latches with automatic offset calibration. Operating at 1GHz sampling rate, the ADC consumes 16mW from 1.2V supplies. The measured DNL is 0.8LSB and INL is 1.2LSB. The measured SFDR and SNDR are 55dB and 43.5dB respectively. The ADC occupies active area of 0.2mm^2. Its FOM is 125fJ/conversion-step.

13-1 The 10G-EPON OLT and ONU LSIs for the Coexistence of 10G-EPON and GE-PON toward the Next FTTH Era

10G-EPON OLT and ONU LSIs with parallel 10- and 1-Gb/s datapaths with a partly-shared-block architecture for full-wire rate throughput and the coexistence of 10G-EPON and GE-PON were developed for the first time in 40-nm CMOS. The full-wire rate throughput without a frame loss and a table look-up in a minimum frame interval are achieved for 10- and 1-Gb/s frames simultaneously.

13-2 A 2.37Gb/s 284.8mW Rate-Compatible (491,3,6) LDPC-CC Decoder

In this paper, a (491, 3, 6) time-varying LDPC-CC decoder chip supporting five code-rates is implemented in 90nm CMOS technology.
The decoder containing 5 processors occupies 2.24mm^2 and provides twice faster decoding convergence speed. Maximum throughput 2.37Gb/s is measured under 1.2V supply with a 0.024nJ/bit/proc energy efficiency.

13-3 A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric

A 2048 look-up-table FPGA with a radix-2 hierarchical interconnect network is realized in 3.94mm^2 in 65-nm CMOS. It has an interconnect-to-logic area ratio of 1:1, which is a 3-4x reduction from modern FPGAs while allowing up to 100% resource utilization. As a proof of concept, it is designed with standard cells, achieving 16.4 GOPS/mm^2 at 370MHz. Peak energy efficiency of 1.1 GOPS/mW is measured at 0.5V.

13-4 SWIFT: A 2.1Tb/s 32 x 32 Self-Arbitrating Manycore Interconnect Fabric

A 32 x 32 64b self-arbitrating switch fabric called SWIFT achieves a bandwidth of 2.1Tb/s with single cycle arbitration and data transfer latency in 65nm technology while operating at 1026MHz at 1.2V. SWIFT co-optimizes arbiter and crossbar logic using a unique fabric architecture that integrates conflict resolution with data routing to optimally use logic and interconnect resources. It spans 0.35mm^2, achieves an efficiency of 7.39Tbps/W, and operates down to 530mV.

14-1 A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications

This paper describes a mixed-signal ECG System-on-chip (SoC) that is capable of implementing configurable functionality with low-power consumption for portable ECG monitoring applications. A low-voltage and high performance analog front-end extracts 3-channel ECG signals and single channel impedance measurement with high signal quality. A custom digital signal processor provides the configurability and advanced functionality like motion artifact removal and R peak detection. The SoC is implemented in 0.18um CMOS process and consumes minimum 31.1uW from a 1.2V.

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14-2 A 96-Channel Full Data Rate Direct Neural Interface in 0.13um CMOS

A sensor interface consumes 6.5 mW from 1.2 V supplies while occupying 5 mm x 5 mm in 0.13 um CMOS. The interface enables full bandwidth access to 96 channels of data acquired from cortical microelectrodes as part of a head-mounted wireless recording system. Open loop amplification and switched-capacitor filtering with 2.2 uV_{rms} input referred noise conditions the signals before conversion by 10-bit SAR ADCs with 60.3 dB SNDR and 41.5 fJ/conv step.

14-3 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication

We report a bolt-shape minimally-invasive neural interface, BioBolt, for epidural recording. Sixteen-channel analog front-end has been implemented in 0.25um technology with low-power wireless data transmission using intra-skin communication. The fabricated ASIC consumes 365uW, occupies 3.2 mm x 0.9 mm, and obtains a 10kb/s data rate.

14-4 A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor

An energy-autonomous and MRI-compatible CMOS implantable sensor is presented that operates by harvesting the energy of the light which penetrates into the tissue. On-chip P+/N-well diodes are used as on-chip photovoltaic cells and in-vivo physiological data is transmitted neuromorphically to the skin surface.

15-1 A 0.63ps Resolution, 11b Pipeline TDC in 0.13um CMOS

This paper presents the first pipeline TDC based on time-domain 1.5b MDAC stages with a digital-domain residue calibration and a time amplifier gain calibration. The proposed architecture is implemented with an 11b TDC using a 0.13um CMOS. The TDC achieves the finest 1b resolution of 0.63ps ever reported in a conversion range of 1.3ns, DNL of 0.5LSB, and INL of 2LSB.

15-2 553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator

A 553-GHz quadruple-push oscillator is demonstrated using low leakage transistors in 45-nm CMOS. The currents of coupling transistors of a quadrature oscillator were summed up to implement quadruple pushing. Quasi-optical measurements showed that the circuit generates 4th harmonic signal at 553 GHz with the power level of 220 nW, while suppressing unwanted harmonic signals. The circuit consumes 64 mW from a 1.4 V supply.

15-3 High-PSRR All-Digital Delay Locked Loop with Burst Update Mode and Power Noise Damping Scheme

The proposed all-digital delay locked loop (DLL) eliminates power noise jitter over all frequency range by combining two methods: Burst update mode and power noise damping filter. The design is fabricated in Hynix's late 30nm DRAM process and tested with DRAM full-chip operations. The jitter of the proposed DLL was measured in a single-para ATE (Automatic Test Equipment). In 1333Mbps, the measured jitter is 34ps at V_{DD} of 1.5V with the operation current of 1.5mA.

15-4 A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance

A MEMS-based clock generator achieves sub-ps jitter in 0.18um CMOS. Key enabling techniques include a 48MHz MEMS oscillator, a reference doubler, a linear XOR-based PFD, a switched-resistor loop filter using accumulation mode NMOS varactors, and native NMOS devices with an RC filter. The overall output at 156.25MHz achieves an integrated phase jitter of 668fs rms over an integration bandwidth of 10kHz-20MHz.

16-1 A Battery-less WiFi-BER Modulated Data Transmitter with Ambient Radio-wave Energy Harvesting

We have developed a new battery-less bit-error-rate modulated (BERM) data transmission technology that can directly send data to a WiFi-equipped PC without affecting WiFi communication on the PC. BER modulated data at a 5.5kbps data-rate has been successfully transmitted at a 30-cm distance between a test chip and measurement equipment. The chip also has an energy harvesting function with an active ambient-radio power searching (AAPS) architecture that enhances harvest efficiency.

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Abstract

16-2 315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4uW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS

A 315MHz injection-locked OOK transmitter and a power-gated receiver front-end for wireless ad hoc network are developed in 40nm CMOS. The developed injection-locked frequency multiplier for carrier generation by edge combining achieves 11uW power consumption at 315MHz. The proposed power-gated low noise amplifier with current second-reuse technique achieves the lowest power consumption of 8.4uW with 7.9dB noise figure and 20.5dB gain in state-of-the-art designs.

16-3 A 550uW Inductorless Bandpass Quantizer in 65nm CMOS for 1.4-to-3GHz Digital RF Receivers

This paper presents an inductorless clockless RF bandpass quantizer in a standard 65nm CMOS technology. An entirely new approach is used based on the information sign and envelope of the RF signal. The quantizer achieves a SNDR of 34dB for an 80MHz bandwidth within a frequency range of 1.4 to 3GHz while consuming 550uW and occupying 0.04mm^2. A FOM of 64fJ/conv is a 45-fold improvement over previous art.

16-4 A 1mm^3 2Mbps 330fJ/b Transponder for Implanted Neural Sensors

An implanted fully-integrated 65nm CMOS 1.1mm x 1.1mm x 0.8mm remotely-powered wireless transponder for implantable neural sensors provides 5uW for sensor interfaces, while consuming 3uW and transmitting 2Mbps at 330fJ/b without violating exposure limitations. This is accomplished by combining a time-multiplexed power and data transmission scheme with a reflective impulse transmitter architecture.

17-1 A 0.5-V Sub-mW Wireless Magnetic Tracking Transponder for Radiation Therapy

As the position of tumor in patient moves during radiation therapy, real-time knowledge of the position of tumor is necessary in order to allow maximum amount of radiation to be focused on the tumor and minimum damage on surrounding healthy tissues. A 0.5-V sub-mW wireless active transponder for a magnetic tracking system is designed in 130-nm CMOS technology to track the position of the tumor. An error of less than 5 mm is achieved with the tracking system.

17-2 A 256 Channel Magnetoresistive Biosensor Microarray for Quantitative Proteomics

This work presents a high sensitivity biosensing platform for quantitative proteomics. Biomolecules labeled with magnetic nanoparticle (MNP) tags are quantitatively sensed by a high density array of 256 giant magnetoresistive spin-valve (GMR SV) sensors connected to a 0.18 um CMOS sensor interface featuring 16 sigma delta modulators with 84 dB dynamic range. The performance of the system is demonstrated through detection of a spiked tumor biomarker, epithelial cell adhesion molecule (EpCAM), at concentrations below 10 picomolar (pM).

17-3 Magnetic Relaxation Detector for Microbead Labels in Biomedical Assays

A Hall-effect biosensor based on magnetic label detection is implemented in 0.18 um CMOS. No external magnet, reference sensor or calibration is required. The sensor offset is suppressed to sub-uV by a mixed-signal feedback loop and correlated double sampling (CDS). Flicker noise and thermal noise are rejected by CDS and averaging. A single 4.5 um bead is detected in 16 ms with a probability of error < 0.1%.

17-4 Low Power Control IC for Efficient High-Voltage Piezoelectric Driving in a Flying Robotic Insect

A dual-channel, low power control IC for driving high voltage piezoelectric actuators in a flapping-wing robotic insect is presented. The IC controls milligram-scale power electronics that meet the stringent weight and power requirements of aerial microrobots. Designed in a 0.13 micron CMOS process, the IC implements an efficient control algorithm to drive piezoelectric actuators with high temporal resolution while consuming <100 microwatts during normal operation at 1.0V.

18-1 A 27% Active-Power-Reduced 40-nm CMOS Multimedia SoC with Adaptive Voltage Scaling Using Distributed Universal Delay Lines

AVS technique for extremely scaled SoCs has been developed. To reduce design cost, we have developed a supply voltage control scheme employing universal delay line (UDL) for monitoring the critical path delay (T_{crit}). The error to Tcrit is as small as that with replica delay line. The UDL can be used in any product without any need for customizing. We have shown that 40-nm CMOS SoCs using our AVS can reduce active power by 27%.

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18-2 LC^2: Limited Contention Level Converter for Robust Wide-Range Voltage Conversion

We propose a robust single-stage static level converter called LC^2 that uses a pulsed control strategy to avoid contention. It reliably converts from 0.3V to 2.5V across wide PVT ranges. Fabricated in 130nm CMOS, 80 measured converters have an average delay of 2.38FO4 and 229fJ switching energy, marking 3.0x and 7.4x improvements over the best prior work. It consumes 475pW static power.

18-3 Adaptive Robustness Tuning for High Performance Domino Logic

A new domino design style is proposed that provides performance gains of up to 71% over conventional domino, and is demonstrated in a 32b multiplier in 65nm CMOS. The design dynamically tunes domino gates to trade surplus noise margins at nominal conditions for performance by detecting stability errors during runtime while guaranteeing correct operation.

18-4 A 381 fs/bit, 51.7 nW/bit Nearest Hamming-Distance Search Circuit in 65 nm CMOS

The developed fully-parallel associative memory in 65nm CMOS for nearest Hamming-distance search is based on distance-frequency mapping with ring oscillators. The largest reference-data capacity of 128 pattern with 512 bit each, the shortest minimum search time of $3.81 \cdot 10^{-13}$ s/bit and the lowest power dissipation of $5.17 \cdot 10^{-8}$ W/bit in comparison to previous designs are reported. In particular, the power-delay product of $1.97 \cdot 10^{-20}$ J/bit is improved by a factor 140.

19-1 A 21nm High Performance 64Gb MLC NAND Flash Memory with 400MB/s Asynchronous Toggle DDR Interface

A monolithic 64Gb MLC NAND flash based on 21nm process technology has been developed for the first time. The device consists of 4-plane arrays and provides page size of up to 32KB. It also features a newly developed DDR interface that can support up to the maximum bandwidth of 400MB/s. To address performance and reliability, on-chip randomizer, soft data readout, and incremental bit lin precharge scheme have been developed.

19-2 A Fast Rewritable 90nm 512Mb NOR "B4-Flash" Memory with $8F^2$ Cell Size

This paper introduces a first 512Mb B4-Flash product chip with $8F^2$ cell size, which is the smallest NOR cell in the 90nm generation. High rewriting throughput (8MB/s) is realized by 10MB/s programming and 100ms/block erasing without over-erase problem. 10MB/s programming is achieved by 1kB simultaneous programming and proposed fast verify scheme. This work proves that B4-Flash can realize not only high rewriting performance like NAND Flash but also fast random access like conventional NOR Flash.

19-3 4-Times Faster Rising V_{PASS} (10V), 15% Lower Power V_{PGM} (20V), Wide Output Voltage Range Voltage Generator System for 4-Times Faster 3D-integrated Solid-State Drives

A wide output voltage range from 10V to 20V voltage generator system is proposed for 3D-SSDs. The circuits are fabricated with the smart mix and match of the standard CMOS, low voltage and high voltage NAND flash memory technologies. The measured rising time for V_{PASS},10V, is four times shorter. The power consumption for V_{PGM}, 20V, decreases by 15%. As a result, the SSD performance increases by 4 times.

19-4 A 512Mb Phase-Change Memory (PCM) in 90nm CMOS Achieving 2b/cell

We present a 256Mcell phase-change memory chip in 90nm CMOS serving as a versatile platform to demonstrate and benchmark multi-level cells. The chip achieves 2b/cell with access times of 320ns and 9.8us for read and write respectively. The mixed-signal circuitry enables up to 4b/cell and includes a programmable controller supporting various programming algorithms. The 6b readout ADC offers high-throughput (690Mb/s) characterization of PCM arrays directly on chip, thereby allowing studies of drift and noise.

20-1 A 20-Gb/s, 0.66-pJ/bit Serial Receiver with 2-Stage Continuous-Time Linear Equalizer and 1-Tap Decision Feedback Equalizer in 45nm SOI CMOS

A power-efficient equalizing serial receiver, including a 2-stage continuous-time linear equalizer (CTLE) and 1-tap decision feedback equalizer (DFE), is reported operating at data rates of up to 20 Gb/s. The DFE adopts a half-rate speculative architecture without explicit summing amplifiers by injecting offset-controlling currents directly into StrongARM sampling latches. At 20 Gb/s, a PCB trace with 26.3dB of loss is equalized while consuming 13.2mW (0.66 pJ/bit).

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20-2 A 40Gb/s Adaptive Receiver with Linear Equalizer and Merged DFE/CDR

A 40Gb/s adaptive receiver using a linear equalizer and a merged half-rate DFE/CDR circuit is fabricated in a 65nm process. For a 40Gb/s PRBS7, the measured jitter of the retimed data is $9.8ps_{pp}$ and $10.7ps_{pp}$ with BER<10^{-12} for the channel loss of 6.7dB and 23.5dB, respectively.

20-3 A 2.6mW/Gbps 12.5Gbps RX with 8-tap Switched-Cap DFE in 32nm CMOS

A 12.5Gb/s receiver circuit with 8-tap decision feedback equalizer (DFE) is presented, which consumes only 2.6mW/Gb/s, and was measured to receive data error-free over a channel with -27dB attenuation. The receiver uses a switched-capacitor (SC) approach for the DFE, where charge is added to the summation node by switching digitally adjustable capacitances dependent on the received data history.

20-4 A 4.4uW Wake-Up Receiver Using Ultrasound Data Communications

We demonstrate free-space ultrasound data communications for ultra-low power wireless wake-up in sensor networks. Using ultrasound carriers allows for an order-of-magnitude power reduction over RF based solutions. The 65nm CMOS 0.6V receiver prototype achieves a BER of better than 10^{-3} over 8.6m for a 0.25kb/s free-space link in a typical indoor environment while dissipating only 4.4uW and requiring only -18dBm transmit signal power.

21-1 A True Random Number Generator Using Time-Dependent Dielectric Breakdown

A true random number generator (tRNG) is proposed that, for the first time, uses the random physical process of time to oxide breakdown under voltage stress. Time to breakdown is repeatedly measured with a counter and serialized into a bitstream. The 1200 um^2 tRNG, called OxiGen, was fabricated in 65 nm CMOS, passes all 15 NIST randomness tests without post-processing and in a 3 month run generated sufficient bits for worst-case expected internet use while being < 10% exhausted.

21-2 On-chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS

An on-chip transistor characterization system for combined C-V/I-V characterization is presented. Capacitance measurement uses a quasi-static charged-based measurement technique with atto-Farad resolution. Random and systematic variability in device I-V and C-V characteristics is studied. The random variability in intrinsic gate capacitance is shown to exhibit Pelgrom scaling. Correlation between I-V and C-V measurements is used to identify systematic channel-length variation gradients in a device array.

21-3 Electrical Monitoring of Gate and Active Area Mask Misalignment Error

A model-free, gate-diffusion (PC-RX) misalignment monitor circuit is implemented in 32nm CMOS for fabrication tool and layout ground rule characterization. It requires only DC current measurements compared to existing optical methods that require special microscopy equipment. An on-chip circuit is also designed to convert misalignment to digital data to enable post-Si repair.

21-4 A 80kS/s 36uW Resistor-based Temperature Sensor Using BGR-free SAR ADC with a Unevenly-weighted Resistor String in 0.18um CMOS

A resistor-based temperature sensor with a BGR-free SAR ADC is reported. The non-zero temperature dependency of the ADC reference voltages, as a result of without using a BGR, is compensated by adopting the proposed unevenly-weighted 9-bit resistor string for reference voltage generation. Fabricated in a 0.18um CMOS, the sensor achieves 0.25°C resolution over 0~100°C range and draws 20uA from a 1.8V supply. At a conversion rate of 80kS/s, the FOM[1] is 0.11nJ/°C.

21-5 PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability

We propose a new ring oscillator (RO) structure to monitor NBTI and PBTI effects separately. In addition, the unique circuit topology makes it possible to directly correlate the RO frequency degradation to transistor threshold voltage (V_t) degradation without relying on compact modeling with device parameters extracted from transistor-level measurements. It also enables high-speed (> GHz) AC BTI stress experiment with accompanying on-chip AC stress circuitry. The validity of the circuit concept is confirmed by measurements from a test chip in a high-k/metal gate SOI CMOS technology.

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22-1 3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype

For the first time we report a high performance embedded DRAM prototype fabricated in a 3D stackable 32nm High-K/Metal Gate technology with copper through-silicon vias. Post through-via processing functional test demonstrates that <1.5ns latency and 500MHz operation are preserved.

22-2 In-substrate-bitline Sense Amplifier with Array-noise-gating Scheme for Low-noise $4F^2$ DRAM Array Operable at 10-fF Cell Capacitance

An in-substrate-bitline sense amplifier (SA) with an array-noise-gating (ANG) scheme-for stable sensing operation in a $4F^2$ DRAM array with cell capacitance of under 20 fF-is proposed. A circuit simulation assuming 40-nm-class 4F2 DRAM chip shows that the SA reduces noise by 58% compared to a conventional SA and achieves stable sensing operation even at cell capacitance of 10 fF.

22-3 A 12.8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications

A single-ended (SE) memory interface utilizing a compact voltage-mode (VM) driver and equalizer, and a reference-voltage (VREF) noise tracking system achieves 12.8-Gbps per pin data rate. Same interface can also communicate with 6.4-Gbps GDDR5 and 1.6-Gbps DDR3 DRAM with no package change. Implemented in a 40-nm CMOS process, the x16 tri-modal interface achieves an energy efficiency of better than 5.0-mW/Gbps per data link at 12.8-Gbps.

22-4 A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface

An improved asymmetric bidirectional memory interface [1] implemented in 40-nm CMOS process achieves 20Gbps per data link, and can also communicate with DDR3 and GDDR5 DRAM at 1.6Gbps and 6.4Gbps, respectively. The low-power tri-modal high-speed interface is enabled by a continuous 1.6GHz to 10GHz clock generation mechanism, and substantial reuse of the circuit elements between the signaling modes, particularly at the driver output stage. In the high speed differential mode, the system utilizes a 1-tap transmit equalizer during a WRITE to the memory, while in memory READ it uses a linear equalizer (LEQ) with 3dB of peaking as well as a calibrated 1-tap predictive decision feedback equalizer (prDFE). The interface consisting of 16 data links achieves efficiency of better than 5.3mW/Gbps.

23-1 Platform Architecture for Solar, Thermal and Vibration Energy Combining with MPPT and Single Inductor

A 0.35um CMOS energy processor with multiple inputs from solar, thermal and vibration energy sources is presented. Dual-path architecture for energy harvesting is proposed that has up to 13% higher conversion efficiency compared to the conventional two stage storage-regulation architecture. To minimize the cost and form factor, a single inductor has been time shared for all converters. A novel low power maximum power point tracking (MPPT) scheme with 95% tracking efficiency is also introduced.

23-2 A Reconfigurable SITITO Boost/Buck Regulator with Sub- Threshold Cross-Regulation-Free Dual-Mode Control for Energy- Harvesting Applications

This paper describes a reconfigurable single-inductor triple-input triple-output regulator that is able to obtain power from three independent sources and provide multiple output regulations for energy-harvesting applications. A sub-threshold dual-mode controller can minimize power dissipation, avoid cross regulation between outputs, and provide predictable output noise spectrum. Implemented in a standard 0.35um CMOS, the proposed regulator provides high power efficiency over a wide load range from 0.3mW to 42mW with the peak power efficiency of 88%.

23-3 A Battery-free 225 nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control

A battery-free 225 nW buck converter is implemented by using 0.25 micro-m CMOS process with die area of 0.21 mm^2. The dynamic on/off time (DOOT) technique can predict the on/off time at different input voltage, as well as suppress static power in the idle period. In addition, the adaptive phase lead mechanism can improve the initial delay from the comparator and improve load regulation by 60 mV.

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23-4 A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications

A digitally enhanced low dropout regulator (LDO) supplying the digital core of an ultra-low-power MCU is presented. By making use of known system power information the LDO digitally adapts its maximum current drivability up to 2.56mA while its quiescent current is as low as 650nA in light load conditions. In this way, the LDO current efficiency remains above 97% over two decades of load current. Energy required for start-up is minimized by drastically reducing capacitance at the LDO output.

23-5 A 13.56MHz CMOS Rectifier with Switched-Offset for Reversion Current Control

A 13.56 MHz full-wave active rectifier for wirelessly powered high-current biomedical implants is presented. It employs switched-offset in reducing the comparator delay for reversion current control. The rectifier was fabricated in a standard 0.35 micro-meter CMOS process with an active area of 0.041 mm^2. The measured power conversion efficiency is better than 83% over a wide ac input range (1.5 to 4 V) and load range (5k to 500 Ohm), and reaches up to 90% at 3.5 V and 1.8 kOhm.

24-1 A 45nm 48-core IA Processor with Variation-Aware Scheduling and Optimal Core Mapping

This paper describes energy benefits of variation-aware dynamic voltage frequency scaling (VA-DVFS) schemes & presents measured WID Fmax, leakage & thermal variations for a 45nm 48-core IA processor. Measurements on a real system show that the proposed VA-DVFS & optimal core mapping schemes (VA-L & VA-LV) improve core computation energy by up to 21% & chip energy by up to 14.5% across varying voltage/frequency (V/F) operating points & core counts.

24-2 A 75uW, 16-Channel Neural Spike-Sorting Processor with Unsupervised Clustering

We describe a neural spike-sorting processor that provides unsupervised clustering simultaneously for 16 channels. The use of a two-stage clustering algorithm, noise-tolerant distance metric, and selectively clocked high-V_T register arrays makes online clustering feasible for implementation. The spike-sorting processor has a power consumption of 75uW at 270mV and an area of 2.45mm^2 in a 65nm CMOS.

24-3 A 7.4mW 200MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios

A 65nm CMOS spectrum sensing digital baseband processor for cognitive radios is integrated in 1.64mm^2. The processor achieves detection probability > 0.9 and false-alarm probability < 0.1 for the -5dB SNR regime within a 50ms sensing time. The chip dissipates 7.4mW for a 200MHz radio bandwidth. A 22x power reduction per sensing bandwidth is achieved compared to state-of-the-art designs.

24-4 Fully Integrated CMOS SoC for 3D Blu-ray Player Applications

A RF/Servo and backend Blu-ray player SoC providing 3D-rich playback is highly integrated on a 56.25mm^2 die in 55nm CMOS. Several cost-effective and high-throughput solutions are realized, leading to 3.85% and 23.13% of area and power reduction. This SoC includes 8x Read, 1080p at 30fps two-view decoding, stereo graphic and HDMI-1.4 output, and dissipates 3.147W from a 1.15/3.3V supply.

24-5 A 52mW Full HD 160-Degree Object Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications

A wearable 1920x1080 160-degree object viewpoint recognition SoC is realized on a 6.38mm^2 die with 65nm CMOS technology. This system focuses on enhancing the capability for wide viewpoint and long-distance recognition while reducing the computation of feature matching process. Object viewpoint prediction (OVP) supports 160-degree object viewpoint differences. 85% of power consumption and 75% of memory bandwidth are reduced by visual vocabulary processor (VVP). 52mW power consumption with 25.9GOPS/mm^2 area efficiency is achieved.

25-1 A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with Tri-Level Comparator

This paper presents an extremely low-voltage operation and power efficient successive-approximation-resistor (SAR) analog-to-digital converter (ADC). Tri-level comparator is proposed to relax the speed requirement of the comparator and decrease the resolution of internal Digital-to-Analog Converter (DAC) by 1-bit. The internal DAC employs unit capacitance of 0.5fF and ADC operates at nearly thermal noise limitation. To deal with the problem of capacitor mismatch, reconfigurable capacitor array and calibration procedure were developed. The prototype ADC fabricated using 40nm CMOS process achieves 46.8dB SNDR with 1.1MS/sec at 0.5V power supply. The FoM is 6.3-fJ/conversion step.

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25-2 A 1-V, 8b, 40MS/s, 113uW Charge-Recycling SAR ADC with a 14uW Asynchronous Controller

This paper presents an energy-efficient charge-sharing SAR ADC design that targets for 1-V, 8-bit 40MS/s performance. By reconfiguring the networks for the input sampling and the reference banks, the settling time at input sample-hold stage and the pre-charge energy for each evaluation phase can be alleviated, that is equivalent to power saving. In addition, a dedicated asynchronous controller is developed to precisely control the energy for each logic operation. With a 90nm CMOS process, the prototype achieves 113uW (20fJ/conv), 48.4dB SNDR. Digital controller only dissipates 12.4% system power.

25-3 Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells

An ADC is synthesized entirely from Verilog code in 90nm digital CMOS using a standard digital cell library. An analog comparator is generated by cross-coupling two 3-input NAND gates. The random comparator offsets are used as the ADC references and are Gaussian. An implicitly aligned three-section piecewise-linear inverse Gaussian CDF function on chip linearizes the output. SNDR of 35.9dB is achieved at 210MSPS.

25-4 A Reconfigurable 1GSps to 250MSps, 7-bit to 9-bit Highly Time-Interleaved Counter ADC in 0.13um CMOS

A reconfigurable highly time-interleaved ADC is realized by combining 128 counter ADCs and a global ramp-generator based on a rotating figure-of-8 resistor ring. Implemented in 0.13um CMOS, the ADC can be configured in real-time as a 1GSps 7-bit, 500MSps 8-bit, and 250MSps 9-bit converter. It achieves sub 400fJ/step in all these configurations.

25-5 A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation

A highly linear calibration free VCO-based ADC uses a two-level modulator to eliminate distortion caused by tuning non-linearity of the VCO. The proposed architecture does not require a multi-level feedback DAC and eases anti-aliasing requirements. Fabricated in 90nm CMOS process, the prototype ADC achieves better than 71dB SFDR and 59.1dB SNDR in 8MHz signal bandwidth and consumes 4.3mW.

26-1 Dual-Loop System of Distributed Microregulators with High DC Accuracy, Load Response Time Below 500ps, and 85mV Dropout Voltage

A dual-loop architecture employs 8 distributed microregulators (UREGs) to achieve response times below 500ps in 45nm SOI CMOS. The trip point of a comparator inside each UREG is tuned for high DC accuracy with a local charge pump, which receives UP/DOWN currents from an outer feedback loop. Measured DC load regulation is better than 10mV down to an 85mV dropout voltage, and jitter readings in a CMOS delay line application indicate output noise below 28mVpp.

26-2 MEMS-switch-based Power Management with Zero-power Voltage Monitoring for Energy Accumulation Architecture on Dust-size Wireless Sensor Nodes

A power management scheme using a MEMS switch is proposed as a way to accumulate charge even when the energy-harvesting device generates minute current of <10 pA. Voltage monitoring does not consume any power at all. A node prototype powered by the MEMS switch is implemented. Test chips were fabricated using the 0.35-um CMOS process and MEMS process. The MEMS-switch power management operation and wireless node operation with nanowatt vibration sensing are confirmed.

26-3 A 210nW 29.3 ppm/degree 0.7 V Voltage Reference with a Temperature Range of -50 to 130 degree in 0.13 um CMOS

A low-voltage, low-power CMOS voltage reference with high temperature stability in a wide temperature range is presented. The temperature dependence of mobility and oxide capacitance is removed by employing transistors in saturation and triode regions and the temperature dependence of threshold voltage is removed by exploiting the transistors in weak inversion region. Implemented in 0.13um CMOS, the proposed voltage reference achieves temperature coefficient of 29.3ppm/^{o}C against temperature variation of -50 - 130^{o}C and line sensitivity of 337ppm/V against supply variation of 0.7-1.8V, while consuming 210nW from 0.7V supply and occupying 0.023mm^{2}.

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Abstract

26-4 A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1-V Input Switched-Capacitor 1/2 Voltage Converter with Output Voltage Trimming by Hot Carrier Injection and Periodic Activation Scheme

A 1-V input, 0.45-V output switched-capacitor (SC) 2:1 voltage converter is developed in 65-nm CMOS. A proposed voltage-reference-free pulse density modulation (VRF-PDM) increased the efficiency from 17% to 73% at 50-uA output current by reducing the pulse density and eliminating the voltage reference circuit. An output voltage trimming by the hot carrier injection to a comparator and a periodic activation scheme of the SC converter are also proposed to solve the problems attributed to VRF-PDM.

26-5 A Fast-Transient DVS-Capable Switching Converter with ΔI_L-Emulated Hysteretic Control

ΔI_L-emulated hysteretic switching converter, achieving both low-ESR operation and fast load transient response, is presented. Designed with a 0.35É m CMOS process, it achieves sub-10mV output ripple and 7.6us/14.4us response times to 400mA load step-up/down changes. Reference tracking speed in DVS is less than 20us/V, which is 9.4 times faster on down-tracking than conventional counterparts, due to a charge recycling technique. It achieves a maximum efficiency of 92.7% and a fixed frequency that is adaptively controlled at 1.7MHz.

27-1 A Laser Ranging Radar Transceiver with Modulated Evaluation Clock in 65nm CMOS Technology

A novel ranging method utilizing modulated clock to count the time of flight (ToF) has been proposed. Substantially reducing the hardware and software complexity, this transceiver prototype achieves ranging resolution of less than 1.3mm while consuming only 50mW from a 1.2V supply.

27-2 10Gb/s Serial I/O Receiver Based on Variable Reference ADC

ADC-based serial I/O receiver draws growing interest with technology scaling. Power consumption remains among the key issues for both the high-speed ADC and the high-throughput DSP. This paper presents an ADC-based receiver that relaxes the ADC requirements with a simple mixed-mode pre-equalizer. Variable ADC reference level compensates for both the frontend non-ideality and the channel response while maintaining low ADC resolution.

27-3 10 Gbps, 530 fJ/b Optical Transceiver Circuits in 40 nm CMOS

This paper describes 10 Gbps optical modulator and receiver circuits designed for high energy efficiency in a 40 nm process. The transmitter consumes 135 fJ/b when bonded to an external silicon photonic ring modulator. The receiver, at -15 dBm sensitivity, consumes 395 fJ/b when bonded to an external photodiode.

27-4 A Direct Sampling Multi-Channel Receiver for DOCSIS 3.0 in 65nm CMOS

This paper presents a fully integrated direct sampling receiver for DOCSIS 3.0, consisting of a time-interleaved ADC, a digital multi-channel selection filter, and a PLL. The receiver can simultaneously receive 4 streams from arbitrary RF frequencies between 48 and 1002MHz and output these in a 13.5MS/s digital IQ format or at a low-IF through integrated DACs. It consumes 980mW from a split 1.2/1.3/1.6V supply when receiving 4 channels and occupies 16.8mm^2 in 65nm CMOS.

28-1 A 45nm 1Mb Embedded STT-MRAM with Design Techniques to Minimize Read-disturbance

1Mb embedded STT-MRAM macro using 45nm CMOS process includes two key design features; a dual-voltage row decoder with a charge sharing scheme for read operations and a sensing circuit with two equalizers and read-disturbance-free reference cells. These designs minimize read-disturbance and achieve fast read operation.

28-2 Fully Parallel 6T-2MTJ Nonvolatile TCAM with Single-Transistor-Based Self Match-Line Discharge Control

A six-MOS-transistor/two-MTJ-device (6T-2MTJ)-based cell circuit with an autonomous leakage-current control mechanism is proposed and fabricated for a fully parallel nonvolatile TCAM. A diode-connected nMOS transistor is inserted into each cell for match-line discharge control, which enables bit-parallel equality-search operation more than 144 bits. Since each match line is divided into three segments, the activity rate of cells is reduced to 2.8%. This almost eliminates leakage power while maintaining comparable search energy of 1.04 fJ/bit/search in comparison with a CMOS-based TCAM.

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Abstract

28-3 A Content Addressable Memory Using Magnetic Domain Wall Motion Cells

A 5-ns search operation of a spintronic content addressable memory (Spin-CAM) was demonstrated, which is the fastest to date and comparable to that of SRAM-based CAM. The 16-kb CAM macro was fabricated using 90-nm CMOS and domain wall (DW) motion processes. We also propose a multiple context CAM to enhance the SoC's performance. The estimated cell area is less than that of an SRAM-based CAM cell, when a four-context CAM is designed.

28-4 A Non-volatile Look-Up Table Design Using PCM (Phase-Change Memory) Cells

This paper describes the design and fabrication of a digital look-up table (LUT) circuit using phase-change random access memory (PCRAM) cells. The LUT, fabricated in IBM 90 nm CMOS technology with embedded GST ($Ge_2Sb_2Te_5$)-based phase-change memory (PCM) mushroom cell, performs pro-grammable and non-volatile logic functions with a 1V supply. The PCRAM cell provides > 100X resistance transformation ratio and the LUT achieves a 453.4ps (average) propagation delay.
