2015 Symposium on VLSI Circuits Short Course 1

VLSI Design for Big Data Management [Suzaku I]

Tuesday, June 16, 10:30-17:10

Organizers / Chairs: Y. Tomita, Fujitsu Laboratories Ltd.
H. Bergveld, NXP Semiconductors

10:30 **Introduction**

10:40 **The Four Components of Big Data Analytics,** K. Olukotun, Stanford Univ.

11:30 **CPU Design Challenges for Big-Data,** S. Borkar, Intel Corp.

12:20 **Lunch**

13:30 **Reconfigurable Computing in a Microsoft Datacenter,** A. Smith, Microsoft Research

14:20 **Memories in Big Data Era,** A. Kawasumi, Toshiba Corp.

15:10 **Break**

15:25 **Role of High Bandwidth I/O for Future Performance Growth of ICT Systems,** H. Tamura, Fujitsu Laboratories Ltd.

16:15 **Digital Control of Power Supplies for Server and Telecom Applications,** S. Choudhury, Texas Instruments Inc.

17:05 **Closing Remark**

17:10 **End of Short Course**

2015 Symposium on VLSI Circuits Short Course 2

Analog and Digital Circuit Design for IoT Swarms [Suzaku III]

Tuesday, June 16, 10:30-17:10

Organizers / Chairs: H. Noda, Renesas Electronics Corp.
E. Yeo, Marvell Semiconductor, Inc.

10:30 **Introduction**

10:40 **Overview of IoT Nodes for Physical Data Collection,** P. Urard, STMicroelectronics

11:30 **Ultra Low Power ADCs and Analog Front-Ends,** P. Harpe, Eindhoven Univ. of Technology

12:20 **Lunch**

13:30 **Green RF: Ultra Low Power RF for the Internet of Things (IoT),** A. Niknejad, Univ. of California, Berkeley

14:20 **Powering the IoT - Batteries Optional,** Y. K. Ramadass, Texas Instruments Inc.

15:10 **Break**

15:25 **Low Power Microcontrollers for IoT,** S. Ohtani, Renesas Electronics Corp.

16:15 **Normally-Off Computing: Synergy of Non-Volatile Memory and Power Management,** H. Nakamura, The Univ. of Tokyo

17:05 **Closing Remark**

17:10 **End of Short Course**

IEEE Solid-States Circuits Society Young Professionals and Grad Students Mentoring and Career coaching event [Suzaku III]

Tuesday, June 16, 17:30-18:30

This will be a special event for early career engineers and grad students, where several leading experts from industry and academia, IEEE Solid-States Circuits Society Executives and AdCom members will have a mentoring session on career coaching, entrepreneurship, publications and answer your questions. This special opportunity would be quite beneficial for the careers of young engineers and students.

Technology SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Tuesday, June 16, 8:20-10:05

Chairpersons: S. Inaba, Toshiba Electronics Korea Corp.
M. Khare, IBM

1-1 - 8:20
Welcome and Opening Remarks
T. Hiramoto, The Univ. of Tokyo
R. Jammy, Intermolecular

1-2 - 8:45 (Invited)
Robotics for Innovation, H. Hirukawa, AIST, Japan

Robotics has been expected to solve serious social problems including the lack of labor population and the increase of senior persons in Japan for recent years. It is estimated that several hundred million dollars have been invested annually for the research and development of robots in the past decade by robotic industries in Japan. The Japanese Government is going to start five years plan towards another industrial revolution by robotic technologies and will invest a comparable amount of the investment with the private sectors. This talk overview the recent research and development of robots mainly in Japan, tries to flush out their promising applications as well as the expectation for VLSI technologies from the robotics.

1-3 - 9:25 (Invited)
System Challenges and Hardware Requirements for Future Consumer Devices: From Wearable to Chrome Books and Devices in-between, E. Shiu and S. Prakash, Google, USA

Internet and mobile application have been driving force for semiconductor innovation in the past 10 years. It's also known that memory and energy walls have been limiting the end-user's perceivable performance. We will focus on the system requirement for today and future's consumer device, such as notebook, tablet, watch, glass or thermostat. Let's start with the user's desire for speed, simplicity and security at the application level, such as video capture, YouTube streaming, Hangout video call, online banking or fitness. Then break it down to what it means to programmers, system architects, technologists and engineers. Finally, a few future research areas in memory architecture, technology and circuit design will be discussed.

Symposium on VLSI Technology

35th Anniversary Celebration [Shunju II, III]

Tuesday, June 16, 19:30-20:00

Alcoholic and Non-Alcoholic beverages will be served.

Both Technology/Circuits Symposia attendees are cordially invited.

Technology / Circuits Joint Evening Panel Discussion

Semiconductor Industry in 2020: Evolution or Revolution? [Shunju II, III]

Tuesday, June 16, 20:00-22:00

Organizers: M. Yamaoka, Hitachi, Ltd.
A. Molnar, Cornell Univ.
N. Sugii, Hitachi, Ltd.
G. Jurczak, imec

Moderators: J. Tham, Broadcom Corp.
T. Piliszczuk, Soitec

Panelists: O. Nalamasu, Applied Materials
J. Hausner, Intel Mobile
S. Tanaka, Murata
T. Yamauchi, Renesas
S. Sivaram, SanDisk
C. Diaz, TSMC
W. Dai, VeriSilicon

Emerging markets such as IoT, M2M, and Big Data analysis will change the game rules of semiconductor industry in 2020. What kind of business models will be required for the players? It is becoming difficult for the Integrated Device Manufacturers (IDM) to make profits simply by fabricating devices. Not only the hardware, but services or solutions becomes more and more important. On the other hand, big players begins to put great effort on the LSI design and acquire many semiconductor design houses. Will the fabless be the best style in 2020? How foundry business will change? Panelists will present their opinions on this topic and discuss what is semiconductor industry in 2020.

SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Wednesday, June 17, 8:30-10:05

Chairpersons: M. Motomura, Hokkaido Univ.
G. Lehmann, Infineon Technologies AG

1-1 - 8:30
Welcome and Opening Remarks
H. Kabuo, Socionext Inc.
J. Gealow, Analog Devices, Inc.

1-2 - 8:45 (Invited)
Profiting From IoT: The Key is Very-Large-Scale Happiness Integration, K. Yano, T. Akitomi, K. Ara, J. Watanabe, S. Tsuji, N. Sato, M. Hayakawa and N. Moriwaki, Hitachi, Ltd., Japan

Big data without link to value is merely a cost. We have studied how to profit from data with Internet-of-Things technologies for over 10 years to reach the answer: the Wearable Happiness Meter. It allows us to integrate the measure of both wellbeing and productivity of 7-billion people worldwide, which was the dream of the 18th-century philosopher Jeremy Bentham, numeration of the greatest happiness of the greatest number to measure the right and wrong. Knowing right and wrong with the 10x speed over conventional financial feedback accelerates the growth of the enterprise, the economy, and the individual to maximize the worldwide happiness. Here the integration is not only on the chip, but in the distributed massive chips embedded in the society.

1-3 - 9:25 (Invited)
Automated Driving – Impacts on the Vehicle Architecture, M. Fausten, T. Huck, A. Rühle, T. Baysal, and R. Kornhaas, Robert Bosch GmbH, Germany

Automated Driving is currently one of the major trends in automotive industry. Almost every car maker has published a roadmap towards introducing automated driving in vehicles of their brand. Introduction of significant highly automated vehicles is expected within the next 10 years. Highly automated driving implies significant challenges to future control units. On the one hand side high performance is required to host the upcoming sophisticated SW which will evaluate the information of a multi sensor set, evaluate and interpret the current driving situation and finally take the decision about the vehicle behavior. On the other hand side, the control units have to be designed highly reliable and need to be composed into a fail operational vehicle architecture. The presentation will highlight the requirements for future electrical and electronics architectures of highly automated vehicles and discuss approaches how to fulfill these requirements.

Technology / Circuits Joint Focus Session 1

Ultra Low Power for IoT [Shunju II, III]

Wednesday, June 17, 10:30-12:35

Chairpersons: M. Tada, NEC Corp.
G. Yeric, ARM

JFS1-1 - 10:30 (Invited)
Automotive Low Power Technology for IoT Society, T. Yamauchi, H. Kondo and K. Nii, Renesas Electronics Corp., Japan

This paper addresses automotive low power technologies in Internet of Things (IoT) societies, where the interaction among cloud information, real-time recognition and vehicle control is a key. High reliability and high performance with low power under the harsh operating conditions are strongly demanded for automotive microcontroller units (MCUs). Our developed embedded Flash (eFlash) and SRAM achieved those required performance at up to Tj=170°C mainly for the vehicle control solution. To perform the highly robust computation in car information applications, the power management involving adaptive voltage scaling and real time power saving are adopted. Moreover other low-power schemes such as multi core CPUsystem with the easier parallelism and the digitally assisted ADC are introduced.

JFS1-2 - 10:55 (Invited)
IoT: the Impact of Things, J. de Boeck*.**, *imec and **KU Leuven, Belgium

Starting from the application perspective this paper expands on the needs for sensor node architecture, wireless communication, security and infrastructure for IoT.

JFS1-3 - 11:20
Transistor-Interconnect Mobile System-On-Chip Co-Design Method for Holistic Battery Energy Minimization, N. N. Mojumder, S. C. Song, K. Rim, J. Xu, J. Wang, J. Zhu, M. Vratonjic, K. Lin, M. Saint-Laurent, P. Bassett and G. Yeap, Qualcomm Technologies, Inc., USA

We present, first time, a holistic data-path-driven transistor-interconnect co-optimization method, which systematically isolates the logic-gate and interconnect-wire dominated data-paths in block-level-delay-bins (sub-binning of delay-based-bins) to significantly improve accuracy of static and dynamic power estimation. It captures the critical interdependence of transistor architecture (FEOL) including local interconnect, and BEOL metal stack optimization to achieve holistic 10nm (N10) technology optimization at target speeds. Using the proposed method, we drive >2.5x Performance/Watt (PpW) improvement for N10 FinFET SOC design over 14nm (N14). Even with ~3x higher wire resistance of min metal width, the PpW @target-speed for N10 improves >2.5x over N14 with proper design of metal/via stack, transistor Vt and fin-profile as well as standard-cell architecture. Reducing active fin-count and routing distance between standard-cells is a critical design knob for N10 mobile SOC enablement. The proposed methodology enables smartphone-usage (days-of-use) based technology optimization, driving longer battery-life in mobile SOCs, keeping process cost and complexity at minimum.

JFS1-4 - 11:45
Sub-μW Standby Power, <18 μW/DMIPS@25MHz MCU with Embedded Atom-Switch Programmable Logic and ROM, Y. Tsuji, X. Bai, M. Miyamura, T. Sakamoto, M. Tada, N. Banno, K. Okamoto, N. Iguchi, N. Sugii and H. Hada, LEAP, Japan

A non-volatile programmable logic (NPL) with atom switch significantly accelerates performance of micro-controller unit (MCU). A low-power 32bit-CPU using a 65 nm-node Silicon-on-Thin-Box (SOTB) CMOS performs 1.95 DMIPS/MHz and 33 μW/MHz on 25 MHz and V_{DD}=0.4 V. When a software process in the CPU is offloaded to NPL, the 9 times faster processing speed and 3 times higher energy efficiency are realized. A reverse body-bias on SOTB CMOS and a power-off of NPL block suppress a standby power down to 0.7 μW.

JFS1-5 - 12:10 (Invited)
Breakthrough Technologies and Reference Designs for New IoT Applications, P. Magarshack, STMicroelectronics, France

Internet of Things regroups numerous applications. Among those, a common critical point is definitely power, as well as energy efficiency. 28nm UTBB FDSOI (28FDSOI) has demonstrated its superiority in terms of energy efficiency through numerous publications. This paper demonstrates the extra mile 28FDSOI is able to offer to designers, enabling on one hand ultra-low power (ULP) system-on-chips for wearable and self-sustainable markets, as well as for medium performance and ultra-low power microprocessor units needed for data concentrators.

SESSION 2

Image Processing [Suzaku II]

Wednesday, June 17, 10:30-12:35

Chairpersons: H. Noda, Renesas Electronics Corp.
S. Sridhara, Apple

2-1 - 10:30
A 0.5-Degree Error 10mW CMOS Image Sensor-Based Gaze Estimation Processor with Logarithmic Processing, K. Bong, I. Hong, G. Kim and H.-J. Yoo, KAIST, Korea

A CMOS image sensor (CIS)-based gaze estimation processor (GEP) is proposed for the next generation user interface (UI) of the smart glasses. It integrates a functional CMOS image sensor (CIS), a RISC, and an ellipse fitting engine (EFE) on a single chip to reduce the power consumption. The functional CIS includes mixed-signal pre-processing circuits, pupil edge detection circuit (PEDC) and glint corner detection circuit (GCDC). Logarithmic processing elements (LPE) is used for EFE to reduce the power consumption further. As a result, PEDC/GCDC and LPE can reduce overall power by 55.2% and 14.1%, respectively. Implemented in 65nm CMOS technology, the 11.29mm^2 chip consumes 10mW power at 30fps real-time operation, and 0.5° error is achieved in a glass-type wearable system.

2-2 - 10:55
A 23mW Face Recognition Accelerator in 40nm CMOS with Mostly-Read 5T Memory, D. Jeon*,**, Q. Dong*, Y. Kim*, X. Wang***, S. Chen***, H. Yu***, D. Blaauw* and D. Sylvester*, *Univ. of Michigan, **Massachusetts Institute of Technology, USA and ***Nanyang Technological Univ., Singapore

This paper presents a face recognition accelerator for HD (1280x720) images. The proposed design detects faces from the input image using cascaded classifiers. A SVM (Support Vector Machine) performs face recognition based on features extracted by PCA (Principal Component Analysis). Algorithm optimizations including a hybrid search scheme that reduces the workload for face detection by 12x. A new mostly-read 5T memory reduces bitcell area by 7.2% compared to a conventional 6T bitcell while achieving significantly better read reliability and voltage scalability due to a decoupled read path. The resulting design consumes 23mW while processing both face detection and recognition in real time at 5.5 frames/s throughput.

2-3 - 11:20
A 640M pixel/s 3.65mW Sparse Event-Driven Neuromorphic Object Recognition Processor with On-Chip Learning, J. K. Kim, P. Knag, T. Chen and Z. Zhang, Univ. of Michigan, USA

A 1.82mm^2 65nm neuromorphic object recognition processor is designed using a sparse feature extraction inference module (IM) and a task-driven dictionary classifier. To achieve a high throughput, the 256-neuron IM is organized in four parallel neural networks to process four image patches and generate sparse neuron spikes. The on-chip classifier is activated by sparse neuron spikes to infer the object class, reducing its power by 88% and simplifying its implementation by removing all multiplications. A light-weight co-processor performs efficient on-chip learning by taking advantage of sparse neuron activity to save 84% of its workload and power. The test chip processes 10.16G pixel/s, dissipating 268mW. Integrated IM and classifier provides extra error tolerance for voltage scaling, lowering power to 3.65mW at a throughput of 640M pixel/s.

2-4 - 11:45
A 33 nJ/Vector Descriptor Generation Processor for Low-Power Object Recognition, D. Shin, I. Hong, G. Kim and H.-J. Yoo, KAIST, Korea

An energy efficient descriptor generation (DG) processor is proposed for low-power object recognition (OR) processor, it has 3 low-power schemes: descriptor reuse (DR) algorithm, hierarchical pipeline (HP) architecture, and look-up table (LUT)-based nonlinear operation circuits. The DR OR algorithm reuses 58% descriptors from the previous frame. The HP employs upper 3-stage keypoint-level pipeline with lower 4-stage fine-grained pixel-level pipeline for the high pipeline utilization. The LUT-based nonlinear operations enhance the energy efficiency. The chip is implemented in a 65nm CMOS process, and it shows average 5 mW power consumption and up to 33 nJ/vector energy efficiency. As a result, 21.6 times higher energy efficiency and 3.5 times higher area efficiency can be achieved compared to the state-of-the-art OR processor.

2-5 - 12:10
Single-Chip 4K 60fps 4:2:2 HEVC Video Encoder LSI with 8K Scalability, T. Onishi*, T. Sano*, Y. Nishida*, K. Yokohari*, J. Su*, K. Nakamura*, K. Nitta*, K. Kawashima**, J. Okamoto**, N. Ono*, R. Kusaba*, A. Sagata*, H. Iwasaki*, M. Ikeda* and A. Shimizu*, *NTT Media Intelligence Laboratories and **NTT Network Technology Laboratories, Japan

This paper proposes the world's first single-chip 4K 60fps 4:2:2 HEVC video encoder LSI (named "NARA") with 8K scalability for broadcasting with professional high image quality. It consists of a prediction core with a new prediction mode decision framework, dual coding cores, controlling RISCs, and high speed data buses with multichip 8K configuration, using 28nm CMOS process. The NARA LSI will lead to a new dimension in future high-quality 8K world.

SESSION 3

SARADCs & SC Filter [Suzaku III]

Wednesday, June 17, 10:30-12:35

Chairpersons: N. Miura, Kobe Univ.
R. Kapusta, Analog Devices, Inc.

3-1 - 10:30
A Sharp Programmable Passive Filter Based on Filtering by Aliasing, N. Sinha*, M. Rachid** and S. Pamarti*, *Univ. of California, Los Angeles and **Silvus Technologies Inc, USA

This paper presents the 1st integrated circuit demonstration of Filtering by Aliasing (FA). FA is a recent technique that uses linear periodically time varying (LPTV) analog circuitry prior to a sampler to provide a desired CT-to-DT transfer function. Such LPTV signal processing offers far superior programmability and performance relative to LTI design. The presented IC applies FA to a single-pole passive RC filter. The resistor, realized as a switched resistor ladder, is continuously varied using on-chip digital control while the output is sampled at a baseband rate. Measured CT-to-DT responses show tunable-bandwidth filter roll-off better than 60 dB/dec, stop-band suppression up to 60 dB, tunable carrier up to 800 MHz, up to 31 dBm out-of-band IIP3, and harmonic rejection.

3-2 - 10:55
A 120nW 8b Sub-Ranging SAR ADC with Signal-Dependent Charge Recycling for Biomedical Applications, S. Jeong*, W. Jung*, D. Jeon**, O. Berenfeld*, H. Oral*, G. Kruger*, D. Blaauw* and D. Sylvester*, *Univ. of Michigan and **Massachusetts Institute of Technology, USA

We present an 8-bit sub-ranging SAR ADC designed for bursty signals having long time periods with small code spread. A modified capacitive-DAC (CDAC) saves previous sample's MSB voltage and reuses it throughout subsequent conversions. This prevents unnecessary switching of large MSB capacitors as well as conversion cycles, reducing energy consumed in the comparator and digital logic and yielding total energy savings of 2.6×. In 0.18μm CMOS, the ADC consumes 120nW at 0.6V and 100kS/s with 46.9dB SNDR.

3-3 - 11:20
A 12b 70MS/s SAR ADC with Digital Startup Calibration in 14nm CMOS, C. C. Lee, C.-Y. Lu, R. Narayanaswamy and J. B. Rizk, Intel Corp., USA

A 12b 70MS/s sub-2 radix SAR ADC designed on Intel's 14nm tri-gate CMOS process is presented. It utilizes a startup calibration for correcting capacitor mismatches in its CDAC. The calibration is fully digital and doesn't require accurate references or input signals. The sub-2 radix architecture provides redundancy that improves speed. The comparator has a novel preamplifier that helps achieve low-noise and high-speed operation. The ADC achieves 68.1dB SNDR, 80dB SFDR, 70MS/s speed, and consumes 4.3mW power.

3-4 - 11:45
A 9.35-ENOB, 14.8 fJ/Conv.-Step Fully-Passive Noise-Shaping SAR ADC, Z. Chen, M. Miyahara and A. Matsuzawa, Tokyo Institute of Technology, Japan

This paper presents an opamp-free solution to implement noise shaping in a successive approximation register analog-to-digital convertor. The comparator noise, incomplete settling error of digital-to-analog convertor and mismatch are alleviated. Designed in a 65 nm CMOS technology, the prototype realizes 58 dB SNDR at 50 MS/s sampling frequency. It consumes 120.7 μW from a 0.8 V supply and achieves a FoM of 14.8 fJ per conversion step.

3-5 - 12:10
A 12-Bit 200-MS/s 3.4-mW CMOS ADC with 0.85-V Supply, J. P. Mathew, L. Kong and B. Razavi, Univ. of California, Los Angeles, USA

A SAR ADC incorporates two VCOs and a TDC as a multi-bit quantizer to improve the conversion speed. Using background calibration and realized in 45-nm technology, the ADC exhibits an SNDR of 68 dB and an FOM of 8 fJ per conversion step at Nyquist.

Technology / Circuits Joint Focus Session 2

Emerging NVM [Shunju II, III]

Wednesday, June 17, 13:55-16:00

Chairpersons: S. Chung, National Chiao Tung Univ.
B.-K. Liew, nVidia

JFS2-1 - 13:55 (Invited)
The Progresses of MRAM as a Memory to Save Energy Consumption and Its Potential for the Further Reduction, H. Yoda, N. Shimomura and S. Fujita, Toshiba Corp., Japan

Several non-volatile memories have been developed to save the energy waste. Among them, MRAM is thought as a promising candidate because of its fast read/write performance and unlimited endurance. Recently critical switching current, I_{sw}, of STT (Spin Transfer Torque)-MRAM has been reduced by several orders and MRAM starts to save the energy waste. In this study, the progresses of MRAM are reviewed and its further potential is discussed from an energy saving point of view.

JFS2-2 - 14:20 (Invited)
Challenges for High-Density 16Gb ReRAM with 27nm Technology, S. Sills*, S. Yasuda**, A. Calderoni*, C. Cardon*, J. Strand*, K. Aratani** and N. Ramaswamy*, *Micron Technology, Inc., USA and **Sony Corp., Japan

Enabling a high-density ReRAM product requires: developing a cell that meets a stringent bit error rate, BER, at low program current, integrating the cell without material damage, and providing a high-drive selector at scaled nodes. We discuss ReRAM performance under these constraints and present a 16Gb, 27nm ReRAM capable of 10^5 cycles with BER < $7x10^{-5}$.

JFS2-3 - 14:45
Low-Power Embedded ReRAM Technology for IoT Applications, M. Ueki, K. Takeuchi, T. Yamamoto, A. Tanabe, N. Ikarashi, M. Saitoh, T. Nagumo, H. Sunamura, M. Narihiro, K. Uejima, K. Masuzaki, N. Furutake, S. Saito, Y. Yabe, A. Mitsuiki, K. Takeda, T. Hase and Y. Hayashi, Renesas Electronics Corp., Japan

A low-power 2Mb ReRAM macro was developed in 90 nm CMOS platform, demonstrating lower power data-writing (x1/7) and faster data-reading (x2~3) as compared to a conventional flash. The memory window at -6σ for 10 years was confirmed with a high speed 1-bit ECC considering operating temperature ranging from -40 to 85°C, where the worst conditions are high-temperature (85°C) “Off” writing and low-temperature (-40°C) “On” writing followed by high-temperature (85°C) retention. A pulse-modulated Off-state verify and an interface control of Ru electrode are effective for suppressing random fluctuation of R_{off} readout and for sustaining the On-state retention, respectively.

JFS2-4 - 15:10
RRAM-Based 7T1R Nonvolatile SRAM with 2x Reduction in Store Energy and 94x Reduction in Restore Energy for Frequent-Off Instant-On Applications, A. Lee*, M.-F. Chang*, C.-C. Lin*, C.-F. Chen*,**, M.-S. Ho***, C.-C. Kuo****, P.-L. Tseng****, S.-S. Sheu**** and T. K. Ku****, *National Tsing Hua Univ., **NDL, ***National Chung Hsin Univ. and ****ITRI, Taiwan

This study proposes a 7T1R nonvolatile SRAM (nvSRAM) to 1) reduce store energy by using a single NVM device, 2) suppress DC-short current during restore operations through the use of a pulsed-overwrite (POW) scheme, and 3) achieves high restore yield by using a differentially supplied initialization (DSI) scheme. This initialization-and-overwrite (IOW) 7T1R nvSRAM improves breakeven-time (BET) by 6+x, compared to previous nvSRAMs. We fabricated a 16Kb IOW-7T1R nvSRAM macro using HfO RRAM and a 90nm process. This represents the first ever silicon verified single-NVM nvSRAM macro. Measurements obtained in test-mode confirm that the proposed nvsRAM reduces store energy by 2x and restore energy by 94x, compared to 2R-based nvSRAMs.

JFS2-5 - 15:35
Reliability Enhancement of 1Xnm TLC for Cold Flash and Millennium Memories, S. Yamazaki, S. Tanakamaru, S. Suzuki, T. O. Iwasaki, S. Hachiya and K. Takeuchi, Chuo Univ., Japan

Endurance and retention are measured in 1Xnm Triple Level Cell (TLC) NAND. To improve reliability, a flexible nLC scheme (flex-nLC) enables the lowest-cost TLC NAND to be used, as is, in long term storage applications, such as cold flash and digital archive: millennium memory, which require 20 and 1000 years retention, and 100 and 1 W/E cycling endurance, respectively. Previously, n-out-of-8 level cell (nLC) technology was applied to 2Xnm TLC for long term storage with 1-time write. Reliability is further enhanced with the new flex-nLC proposal, which combines asymmetric coding and nLC with an additional vertical flag area. Because all data conversion and flag calculations are handled in the SSD controller, the highest-density, lowest-cost 1Xnm TLC NAND can be used, as is. Optimization of flexible-nLC for 1Xnm TLC reduces errors in the extreme retention applications by 66% and 71%, compared to conventional nLC.

SESSION 4

Image Sensors [Suzaku II]

Wednesday, June 17, 13:55-16:00

Chairpersons: H. Wakabayashi, Sony Corp.
D. Sylvester, Univ. of Michigan

4-1 - 13:55
Image Sensor/Digital Logic 3D Stacked Module Featuring Inductive Coupling Channels for High Speed/Low-Noise Image Transfer, M. Ikebe*, D. Uchida*, Y. Take**, M. Someya*, S. Chikuda*, K. Matsuyama*, T. Asai*, T. Kuroda** and M. Motomura*, *Hokkaido Univ. and **Keio Univ., Japan

This paper proposes 3D stacked module consisting of image sensor and digital logic dies connected through inductive coupling channels. Evaluation of a prototype module revealed radiation noise from the inductive coils to the image sensor is less than 0.4-LSB range along with ADC code, *i.e.*, negligible. Aiming at high frame rate image sensor/processing module exploiting this attractive off-die interface, we also worked on resolving another throughput-limiter, namely power consuming TDC used in column parallel ADCs. Novel intermittent TDC operation scheme presented in this paper can reduce its power dissipation 57% from conventional ones.

4-2 - 14:20
A 0.66e^-_{rms} Temporal-Readout-Noise 3D-Stacked CMOS Image Sensor with Conditional Correlated Multiple Sampling (CCMS) Technique, S.-F. Yeh, K.-Y. Chou, H.-Y. Tu, C. Y.-P. Chao and F.-L. Hsueh, TSMC, Taiwan

A conditional correlated multiple sampling (CCMS) technique for low noise CMOS image sensor (CIS) is proposed to reduce noise and address low frame rate issue caused by the conventional correlated multiple sampling (CMS) technique. An 8Mpixel 3D-stacked CIS with 1.1um pixel pitch is designed and verified. Measurement results show this technique can achieve 0.66e^-_{rms} at 36.1 kHz A/D sampling rate per pixel with analog gain at 16 and 5-times multiple sampling. The resulting DNL is within -0.49/+0.45LSB.

4-3 - 14:45
A 0.4V Self-Powered CMOS Imager with 140dB Dynamic Range and Energy Harvesting, A. Y.-C. Chiou and C.-C. Hsieh, National Tsing Hua Univ., Taiwan

This PWM imager operates at a lowest reported supply 0.4V with a 0.42x smaller pixel size, 1.5x larger fill factor, 0.58 smaller random noise, and 3x better iFoM than previous work. With proposed dual-exposure extended-counting (DEEC) scheme, the prototype achieves a high dynamic range of 140dB with a 58dB boost. Optical energy harvesting (OEH) design is implemented to generate 60.3pW per lux per mm^2 and 1.28x higher efficient than current design. A self-powered imager is demonstrated with 15fps under 100klux.

4-4 - 15:10
A Linear Response Single Exposure CMOS Image Sensor with 0.5e^- Readout Noise and 76ke^- Full Well Capacity, S. Wakashima, F. Kusuhara, R. Kuroda and S. Sugawa, Tohoku Univ., Japan

A linear response single exposure CMOS image sensor approaching to the photon countable sensitivity and a high full well capacity is developed using lateral overflow integration capacitor architecture with dual gain column amplifiers, small floating diffusion capacitance and low noise in-pixel source follower signal readout technologies. The fabricated 5.5 um pitch 360^H x 1680^V pixel prototype image sensor exhibited 240 μV/e^- conversion gain with 76 ke^- FWC resulting in 0.5 e^-_{rms} readout noise and 104 dB dynamic range under room temperature operation.

4-5 - 15:35
A 3D Stacked CMOS Image Sensor with 16Mpixel Global-Shutter Mode and 2Mpixel 10000fps Mode Using 4 Million Interconnections, T. Kondo, Y. Takemoto, K. Kobayashi, M. Tsukimura, N. Takazawa, H. Kato, S. Suzuki, J. Aoki, H. Saito, Y. Gomi, S. Matsuda and Y. Tadaki, Olympus, Japan

A 16Mpixel 3D stacked CMOS image sensor with pixel level interconnections using 4,008,960 micro bumps at a 7.6μm pitch, which set no layout restriction and causes no harm to sensor characteristics, was developed to achieve both a 16Mpixel global-shutter mode with a -180dB PLS and 2Mpixel 10000fps high speed image capturing mode.

SESSION 5

Low Power Wireless Transceivers [Suzaku III]

Wednesday, June 17, 13:55-16:00

Chairpersons: K. Agawa, Toshiba Corp.
G. Gammie, MediaTek USA

5-1 - 13:55
A 3.5mW 315/400MHz IEEE802.15.6/Proprietary Mode Digitally-Tunable Radio SoC with Integrated Digital Baseband and MAC Processor in 40nm CMOS, C. Bachmann*, M. Vidojkovic*, X. Huang*, M. Lont*, Y.-H. Liu*, M. Ding*, B. Busze*, J. Gloudemans*, H. Giesen*, A. Sbai*, G.-J. van Schaik*, N. Kiyani*, K. Kanda**, K. Oishi**, S. Masui**, K. Philips* and H. de Groot*, *imec, The Netherlands and **Fujitsu Laboratories, Japan

An energy-efficient, flexible radio SoC with RF front-end (RFFE), digital baseband (DBB) and microcontroller (MCU) for medical/healthcare applications in 315/400 MHz bands is presented. The SoC is fully-compliant with the IEEE 802.15.6 standard in 400MHz bands, and also supports proprietary modes, including high data rate (HDR) modes with x2/4/8 data rates (max 3.6Mb/s) to support applications like EEG, and low-power modes with 1/16 data rate to minimize sensor node power consumption. The total power consumption of 3.5mW (RX, 3.6Mb/s, -77dBm sensitivity) enables best-in-class power efficiency of 1nJ/bit.

5-2 - 14:20
A 1Gb/s Energy Efficient Triple-Channel UWB-Based Cognitive Radio, N.-S. Kim and J. M. Rabaey, Univ. of California, Berkeley, USA

A triple-channel BPSK UWB-based cognitive radio provides energy efficient 1Gb/s short-range connectivity by scavenging triple discrete inactive frequency bands in 3.1-10.6GHz ISM bands. The developed transceiver in 65nm CMOS achieves the minimum energy consumption of 59.7pJ/b with $1.97X10^{-4}$ BER. Die area is $4.6mm^2$ with on-die PLLs.

5-3 - 14:45
A 0.6V All-Digital Body-Coupled Wakeup Transceiver for IoT Applications, P. N. Whatmough*, G. Smart**, S. Das*, Y. Andreopoulos** and D. M. Bull*, *ARM Ltd. and **Univ. College London, UK

A body-coupled symmetric wakeup transceiver is proposed for always-on device discovery in IoT applications requiring security and low-power consumption. The wakeup transceiver (WTRx) is implemented in 65nm CMOS, using digital logic cells and operates at 0.6V. A directly-modulated open-loop DCO generates an OOK-modulated 10MHz carrier, with a frequency-locked loop for intermittent calibration. A passive receiver incorporates a digital IO cell as hysteretic comparator, with a two-phase correlator bank. A novel MAC scheme allows for duty-cycling in both transmitter and receiver. Measured power consumption is 3.54μW, with sensitivity of 88mV and maximum wakeup latency of 150ms.

5-4 - 15:10
A Self-Powered IPv6 Bidirectional Wireless Sensor & Actuator Network for Indoor Conditions, P. Urard*, G. Romagnello*, A. Banciu*, J. C. Grasset*, V. Heinrich*, M. Boulemnakher*, F. Todeschni*, L. Damon*, R. Guizzetti*, L. Andre** and A. Cathelin*, *STMicroelectronics and **CEA-LETI, France

This paper demonstrates an IPv6 self-powered bidirectional wireless network system solution, compatible with indoor conditions, based on a IEEE 802.15.4/802.14.4e 2.4GHz radio (5.4mA Rx / 7.3mA Tx) and a 130nA quiescent current Power Management Unit (PMU). Other key elements are a 32bits Cortex M3 microcontroller and MEMs for sensors. This chipset enables self-powered sensors and actuators as well as over-the-air programing. It is able to sustain a working/home environment (100 lux CLF light during 6 hours a day), able to harvest as low as 1uW energy, and keep operating in the dark during more than 2 months.

5-5 - 15:35
A 794Mbps 135mW Iterative Detection and Decoding Receiver for 4x4 LDPC-Coded MIMO Systems in 40nm, W.-H. Wu*, W.-C. Sun*, C.-H. Yang** and Y.-L. Ueng*, *National Tsing Hua Univ. and **National Chiao Tung Univ., Taiwan

A low-density parity-check (LDPC)-coded multiple-input multiple-output (MIMO) systems with iterative detection and decoding (IDD) chip is integrated in $1.33mm^2$ in 40nm CMOS. The maximum gross throughput is 794Mb/s for a 4x4 16-QAM configuration at 288MHz. The chip dissipates 135mW at 0.9V, achieving an energy efficiency of 170pJ/bit. Compared to non-IDD receivers, composed of state-of-the art MIMO detectors and LDPC decoders, this work achieves even higher area and energy efficiencies, despite the improved error performance.

SESSION 6

Bio Monitoring Circuits [Suzaku II]

Wednesday, June 17, 16:15-17:55

Chairpersons: C.-Y. Lee, National Chiao Tung Univ.
J. DeBrosse, IBM

6-1 - 16:15
A 16-Channel Wireless Neural Interfacing SoC with RF-Powered Energy-Replenishing Adiabatic Stimulation, S. Ha, A. Akinin, J. Park, C. Kim, H. Wang, C. Maier, G. Cauwenberghs and P. P. Mercier, Univ. of California, San Diego, USA

This paper presents a fully-integrated 16-channel wireless neural interfacing SoC that employs an adiabatic stimulator powered directly from a 190-MHz on-chip antenna to eliminate bulky external components while simultaneously avoiding rectifier and regulator losses. Using a charge replenishing architecture, the stimulator outputs up to 145-μA, while achieving a 63.1% charge replenishing ratio and a stimulation efficiency factor of 6.0. Analog front-ends and telemetry circuitry are also included.

6-2 - 16:40
Enabling Closed-Loop Neural Interface: A Bi-Directional Interface Circuit with Stimulation Artifact Cancellation and Cross-Channel CM Noise Suppression, A. E. Mendrela, J. Cho, J. A. Fredenburg, C. A. Chestek, M. P. Flynn and E. Yoon, Univ. of Michigan, USA

We present the first bi-directional neural interface chip that employs a stimulation artifact cancellation circuit to allow concurrent recording and stimulation. In order to further suppress cross-channel common-mode noise, we incorporated a novel common average referencing (CAR) circuit in conjunction with range-adapting (RA) SAR ADC for low-power implementation. The fabricated prototype attenuates stimulation artifacts by up to 42 dB and suppresses common noise among channels by up to 39.8 dB at 330 nW and in an area of 0.17 mm^2 per channel.

6-3 - 17:05
Neurochemical Thermostat: A Neural Interface SoC with Integrated Chemometrics for Closed-Loop Regulation of Brain Dopamine, B. Bozorgzadeh*, D. Schuweiler**, M. Bobak**, P. A. Garris** and P. Mohseni*, *Case Western Reserve Univ. and **Illinois State Univ., USA

A 3.3 × 3.2mm^2 SoC in 0.35μm two-poly four-metal CMOS combines 400Vs^{-1} fast-scan cyclic voltammetry (FSCV) sensing, on-the-fly chemometrics, and feedback-controlled microstimulation to realize a “neurochemical thermostat” for closed-loop regulation of brain dopamine. The SoC employs principal component regression (PCR)-based chemometrics for real-time differentiation of dopamine levels from common interferents encountered in vivo such as pH change and background-current drift, and maintains the levels between two user-set thresholds via closed-loop neuromodulation. The SoC features duty cycling in intermittent FSCV sensing and digital signal processing to dissipate 127.5μW at 2.5V.

6-4 - 17:30
Toward 1024-Channel Parallel Neural Recording: Modular Δ-ΔΣ Analog Front-End Architecture with 4.84fJ/C-s•mm^2 Energy-Area Product, S.-Y. Park, J. Cho, K. Na and E. Yoon, Univ. of Michigan, USA

We report an energy- and area-efficient modular analog front-end (AFE) architecture incorporating Δ-modulated ΔΣ (Δ-ΔΣ) signal acquisition for 1,024-channel brain activity monitoring platforms. The AFE employs spectrum-equalizing and continuous-time (CT)-ΔΣ quantization to make use of the inherent spectral characteristics of brain signals. The dynamic range (DR) of the neural signals has been compressed by 27dB (spectrum equalization). The energy-area product is the most critical figure of merit for massively-parallel recordings and the AFE achieves 4.84fJ/C-s•mm^2, the smallest ever reported. The fabricated circuits consume 0.05mm^2 and 3.05μW/channel, exhibiting 63.8dB SNDR, 3.02 NEF, and 4.56NEF^2V_{DD}.

SESSION 7

Optical Links [Suzaku III]

Wednesday, June 17, 16:15-17:55

Chairpersons: K. Sunaga, NEC Corp.
T. Fiez, Oregon State Univ.

7-1 - 16:15
A 19.6-Gbps CMOS Optical Receiver with Local Feedback IIR DFE, A. Sharif-Bakhtiar and A. C. Carusone, Univ. of Toronto, Canada

This paper describes a low power optical receiver for discrete photodiodes. The receiver utilizes an input stage bandwidth of only 2GHz, affording high gain with low power consumption while limiting input-referred noise. The resulting ISI is eliminated and data recovered using an IIR DFE. The IIR DFE utilizes a local feedback to relax the timing criteria of the DFE loop. The 65-nm CMOS chip consumes 14.7 mW at 19.6Gbps.

7-2 - 16:40
56Gb/s PAM4 and NRZ SerDes Transceivers in 40nm CMOS, J. Lee, P.-C. Chiang and C.-C. Weng, National Taiwan Univ., Taiwan

This paper presents 56Gb/s PAM4 and NRZ SerDes transceivers (TRXs), designed and fabricated in advance CMOS technology. Incorporating broadband techniques, noise suppression skills, and clock extraction circuits, this work demonstrates feasibility of 56Gb/s SerDes and compares tradeoffs between the two data format.

7-3 - 17:05
A 25-Gb/s, -10.8-dBm Input Sensitivity, PD-Bandwidth Tolerant CMOS Optical Receiver, S.-H. Huang and W.-Z. Chen, National Chiao Tung Univ., Taiwan

This paper describes a 25-Gb/s energy-efficient CMOS optical receiver with high input sensitivity. By incorporating a current boosting preamplifier with time-interleaved integrating-type optical receiver, it also circumvents CID issue with high PD bandwidth tolerance. Experimental results show that the receiver can achieve 25-Gb/s operation by integrating with a 9-GHz or 17-GHz GaAs PD. Input sensitivities in the two cases are -7.2 dBm (w/i 9-GHz PD) and -10.8 dBm (w/i 17-GHz PD) respectively for BER of less than 10^{-12}. The energy efficiency is 1.13 pJ/bit. Fabricated in TSMC 40-nm CMOS technology, the core circuit occupies a chip area of 0.007 mm^2 only.

7-4 - 17:30
A 45nm SOI Monolithic Photonics Chip-to-Chip Link with Bit-Statistics-Based Resonant Microring Thermal Tuning, C. Sun*.**, M. Wade***, M. Georgas**, S. Lin*, L. Alloatti**, B. Moss**, R. Kumar***, A. Atabaki**, F. Pavanello***, R. Ram**, M. Popović*** and V. Stojanović*, *Univ. of California, Berkeley, **Massachusetts Institute of Technology and ***Univ. of Colorado, USA

A new thermal tuning circuit for optical ring modulators enables demonstration of an optical chip-to-chip link for the first time with monolithically integrated photonic devices in a commercial 45nm SOI process, without any process changes. The tuning circuit uses independent 1/0 level-tracking and 1/0 bit counting to remain resilient against laser self-heating transients caused by non-DC-balanced transmit data. A 30fJ/bit transmitter and 374fJ/bit receiver with $6\mu A_{pk\text{-}pk}$ photocurrent sensitivity complete the 5Gb/s link. The thermal tuner consumes 275fJ/bit and achieves a 600 GHz tuning range with a heater tuning efficiency of 3.8μW/GHz.

Technology / Circuits Joint Banquet [Shunju I, II, III]

Wednesday, June 17, 19:00-21:00

SESSION 8

Circuits Focus Session - Systems for Big Data Management [Suzaku II]

Thursday, June 18, 8:30-10:10

Chairpersons: M. Yamaoka, Hitachi, Ltd.
C. Dray, Intel Mobile Communications GmbH

8-1 - 8:30 (Invited)
FPGA-Accelerated Complex Event Processing, T. Takenaka, H. Inoue, T. Hosomi and Y. Nakamura, NEC Corp., Japan

This paper introduces an example of real-time “big data” processing systems accelerated by field-programmable gate arrays (FPGAs), which will open up a novel design field for digital circuit engineers. Contrary to the perception that software on commodity servers dominates such large-scale processing requirements, there are various chances for utilizing hardware for the acceleration. One of the most promising applications is complex event processing (CEP), which requires hardware-based acceleration due to it having to process massive amounts of data in real time. We propose a design flow for compiling software-oriented event language into highly parallelized and pipelined CEP circuits, which enables our system to achieve a strikingly high performance of 20 Gbps. A sophisticated mechanism for integrating archives of previously arrived data with streams of current events also makes the FPGA-accelerated processing system applicable to a wide range of realistic “big data” applications.

8-2 - 8:55
Inductively-Powered Wireless Solid-State Drive (SSD) System with Merged Error Correction of High-Speed Non-Contact Data Links and NAND Flash Memory, A. Kosuge*, J. Hashiba*, T. Kawajiri*, S. Hasegawa*, T. Shidei*, H. Ishikuro*, T. Kuroda* and K. Takeuchi**, *Keio Univ. and **Chuo Univ., Japan

This paper presents a wireless solid-state drive (SSD) system for future applications of large volume storage in mobile devices or data center. The wireless interface in the developed system consists of an inductive-coupling power link with a fast transmitting power control and high-speed data links with transmission line couplers (TLCs). The wireless power link can deliver 1W from the host side to the SSD side. The full duplex wireless data interface achieved raw data rate of 1.6Gbps/link. The error correction block for NAND flash memory system can also correct the error in wireless data links. The data link has tolerance to the interference from the power link, and both the data and power links show the waterproof property of the system.

8-3 - 9:20
Privacy-Protection Solid-State Storage (PP-SSS) System: *Automatic Lifetime Management of Internet-Data’s Right to be Forgotten,* S. Tanakamaru, H. Yamazawa and K. Takeuchi, Chuo Univ., Japan

A privacy-protection solid-state storage (PP-SSS) system with 1Xnm 3bit/cell triple-level cell (TLC) NAND flash memory is proposed to comply with the recent “Right to be forgotten” data trend. In PP-SSS, private data is automatically corrupted within the hardware itself based on expiration dates that are individually selectable for each file. PP-SSS consists of two proposals: partial bit-flip (PBF) and NPBF page-allocation scheme for rough and precise control of the data-expiration dates, respectively. In PBF, a part of the data is bit-flipped and errors are intentionally injected. Therefore, the data lifetime is limited due to failure of error correction. The larger the number of PBF (NPBF) is, the sooner the data becomes unreadable. Since the reliability of each page is different, and to more precisely control the data lifetime, NPBF page-allocation refers to a pre-recorded table which stores the measured NPBF of each page with different data-expiration date and write/erase cycles.

8-4 - 9:45 (Invited)
Caching Mechanisms towards Single-Level Storage Systems for Internet of Things, Y. Bando, K. Watanabe, K. Maeda, H. Kudo, M. Ishiyama, A. Kunimatsu, H. Nakai, M. Takahashi and Y. Oowaki, Toshiba Corp., Japan

Internet of Things (IoT) involves coping with enormous number of distributed devices. This paper introduces three pieces of caching technology as steps towards single-level storage systems that can host and map numerous IoT devices on a single vast address space: 1) a caching mechanism for making solid-state storage appear as huge main memory, 2) speeding up access to resource-limited IoT devices by caching the address translation table of solid-state storage chips, and 3) ad hoc device-to-device data relay, which can be used as effective network caching for mapping IoT devices.

SESSION 9

Phase and Delay Locked Loops [Suzaku III]

Thursday, June 18, 8:30-10:10

Chairpersons: S. H. Cho, KAIST
A. Momtaz, Broadcom Corp.

9-1 - 8:30
An All-Digital Bang-Bang PLL Using Two-Point Modulation and Background Gain Calibration for Spread Spectrum Clock Generation, S. Jang, S. Kim, S.-H. Chu, G.-S. Jeong, Y. Kim and D.-K. Jeong, Seoul National Univ., Korea

An all-digital spread spectrum clock generator (SSCG) using two-point modulation is presented. To calibrate the gain mismatch between two modulation paths, a background gain calibration method is proposed. To reduce power consumption and design complexity, the bang-bang phase-frequency detector (BBPFD) is used instead of the time-to-digital converter (TDC). The prototype chip has been fabricated in a 65-nm CMOS process and it consumes 6 mW at 2.5 GHz. The core area is 0.05 mm^2 and the measured minimum rms jitter is 1.58 ps.

9-2 - 8:55
A Digital Bang-Bang Phase-Locked Loop with Automatic Loop Gain Control and Loop Latency Reduction, T.-K. Kuan and S.-I. Liu, National Taiwan Univ., Taiwan

This paper presents a digital bang-bang phase-locked loop that employs automatic loop gain control and loop latency reduction techniques to enhance the jitter performance. The chip is fabricated in a 40nm CMOS process. This bang-bang phase-locked loop achieves 290fs_{rms} integrated jitter and reference spurs <-72.89dBc. It consumes 3.8mW from a 1.1V supply while operating at 3.96GHz. This translates to an FOM of -245dB.

9-3 - 9:20
A 0.4-1.6GHz Spur-Free Bang-Bang Digital PLL in 65nm with a D-Flip-Flop Based Frequency Subtractor Circuit, B. Kim*,**, S. Kundu* and C. H. Kim*, *Univ. of Minnesota and **Rambus Inc., USA

A 0.4-1.6GHz spur-free bang-bang PLL (BBPLL) is demonstrated in a 65nm CMOS process where a standard D-flip/flop (DFF) based frequency subtractor is used in lieu of a conventional divider, for down-converting the feedback clock frequency. The inherent firstorder noise-shaping property allows the proposed frequency subtraction circuit to mitigate spur-noise issues found in conventional digital BBPLLs. The fabricated BBPLL including a 10bit ring-DCO circuit has an in-band phase noise of -97dBc/Hz at 100kHz and an integrated RMS jitter (from 20kHz to 2MHz) of 2.8ps while consuming 2.7mW at 1.6GHz and occupying 0.019mm^2. The PLL circuit has an FoM of -226.7dB.

9-4 - 9:45
A 450-fs Jitter PVT-Robust Fractional-Resolution Injection-Locked Clock Multiplier Using a DLL-Based Calibrator with Replica-Delay-Cells, M. Kim, S. Choi and J. Choi, Ulsan National Institute of Science and Technology (UNIST), Korea

This paper presents a PVT-robust, low-jitter, injection-locked clock multiplier with the frequency resolution of one tenth of the reference frequency, using a DLL-based PVT-calibrator. As the key idea, the ring-VCO and the DLL consist of identical delay cells and share the same control voltage. Since the DLL continually corrects the delay of the unit delay cells, the degradation of jitter due to the drift of the free-running VCO frequency can be prevented. The proposed clock multiplier was fabricated in a 65-nm CMOS technology, and the active area was 0.041 mm^2. The phase noise at the 1-MHz offset and the RMS-jitter of a 1.76-GHz signal were -122.3 dBc/Hz and 448 fs, respectively. Their variations with temperature (30 - 90 degrees Celsius) were regulated to be less than 0.5 dB and plus-minus 4%, respectively. Based on a DLL, the proposed calibrator greatly reduced the frequency-switching time to less than 500 ns.

SESSION 10

Circuits Focus Session - IoT and Smart Systems [Suzaku II]

Thursday, June 18, 10:30-12:35

Chairpersons: S. Nimmagadda, Intel Technology India Pvt Ltd.
A. Cathelin, STMicroelectronics

10-1 - 10:30 (Invited)
Embedded Image Recognition Systems for Advanced Safety Vehicles, M. Takemura, T. Shima and S. Muramatsu, Hitachi, Ltd., Japan

Driver safety continues to be improved by advances in active safety technologies. In various advanced countries, regulations and New Car Assessment Program soon will require Autonomous Emergency Braking (AEB) and Lane Departure Warning (LDW). The market of recognition systems for active safety is continually expanding, in which a key element is image recognition technology for advanced safety vehicle. We have been developing core image recognition technologies for autonomous vehicle. These core technologies can be divided into 3 categories which are front, rear-view, and SurroundEye camera systems. First, we describe the SurroundEye view monitoring system using 4 cameras for parking assistance. Second, we describe the rear-view camera sensing system which is used on both rear-view monitoring and active safety technologies. Finally, we introduce active safety technologies using a front stereo camera. These kind of systems require real-time processing, and robust sensing in outdoor environments.

10-2 - 10:55
High-Level Video Analytics PC Subsystem Using SoC with Heterogeneous Multi-Core Architecture, Y. Sasagawa and A. Mori, Panasonic Corp., Japan

The High-level video analytics PC sub-system as PCIe add-in card had been developed for surveillance, retail marketing tool and various applications which require acceleration of computer vision analytics for real-time video. The PC subsystem has multi-core architecture SoC, which comprises proposed Computer Vision Engine (CVE) based on pre-processor, target detector, and target tracker. The target detector has the capability of on-line learning from images so that it can give robustness of tracking targets. Heterogeneous structure with the multi-core processor and CVE accelerator achieves performance at 3515GOPS, and power efficiency at 1871GOPS/W, it is approximately 10x higher performance and 3x higher efficiency than other processors.

10-3 - 11:20
A Throughput-Agnostic 11.9-13.6GOPS/mW Multi-Signal Classification SoC for Cognitive Radios in 40nm CMOS, F.-L. Yuan*, R. K. Palani**, S. Basir-Kazeruni*, H. Shih**, A. Saha**, R. Harjani** and D. Marković*, *Univ. of California, Los Angeles and **Univ. of Minnesota, USA

A blind classification SoC for cognitive radios, featuring multi-signal channelization, 16-core dynamic parallelism-frequency scaling and GALS-based multithreading, is realized in 40nm CMOS. Targeting ≥95% detection probability and <0.5% false-alarm rate, the SoC achieves a throughput-insensitive energy efficiency of 11.9-13.6GOPS/mW for multiple 7.8-125MHz bandwidth-agnostic signals in a 500MHz channel. The SoC shows 2.1x lower energy, >2.7x less efficiency variation, 1.2x baseband area and up to 4x processing time reduction compared to prior work. Throughput-matched scheduling of spatial resources enables operation at peak energy efficiency without the need for any voltage adjustment.

10-4 - 11:45
A Multi-Chip System Optimized for Insect-Scale Flapping-Wing Robots, X. Zhang, M. Lok, T. Tong, S. Chaput, S. K. Lee, B. Reagen, H. Lee, D. Brooks and G.-Y. Wei, Harvard Univ., USA

We demonstrate a battery-powered multi-chip system optimized for insect-scale flapping wing robots that meets the tight weight limit and the high real-time performance demand of autonomous flight. Measured results show successful open-loop lift off and improved energy efficiency enabled by hardware acceleration.

10-5 - 12:10 (Invited)
Sensor-Hub Sweet-Spot Analysis for Ultra-Low-Power Always-on Operation, A. Fuks, NXP Semiconductors, USA

With the increasing use of sensors in mobile devices, processing the data coming from these sensors continuously requires ultra-low power consumption of the system. The microcontroller unit (MCU) is central in this system. This paper presents an MCU for Internet of Things (IoT) applications and in particular it addresses how to operate the MCU in efficiency sweet spots to achieve the overall lowest possible power consumption.

SESSION 11

Nyquist ADC and DAC [Suzaku III]

Thursday, June 18, 10:30-12:35

Chairpersons: M. Ito, Renesas Electronics Corp.
E. Fogleman, MaxLinear

11-1 - 10:30
A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS, S. Cai, E. Z. Tabasy, A. Shafik, S. Kiran, S. Hoyos and S. Palermo, Texas A&M Univ., USA

A 25GS/s 8-way time-interleaved binary search ADC employs a novel soft-decision selection algorithm to improve metastability tolerance and relax T/H settling requirements. The T/H design is further relaxed with reduced loading from a new shared-input three comparator structure. Fabricated in GP 65nm CMOS, the ADC achieves 4.62-bits ENOB at Nyquist and 143 fJ/conv.-step FOM, while consuming 88mW and occupying 0.24mm^2 core ADC area.

11-2 - 10:55
A 3-10fJ/Conv-Step 0.0032mm^2 Error-Shaping Alias-Free Asynchronous ADC, S. Patil*, A. Ratiu**,***, D. Morche** and Y. Tsividis*, *Columbia Univ., USA, **CEA-LETI and ***Univ. de Lyon, France

We present a programmable, quantization error spectral shaping, alias-free asynchronous ADC suited for clockless, continuous-time DSP in receivers with modest SNDR requirements and a tight power budget. Implemented in 0.65V 28nm FDSOI, the 0.0032mm^2 ADC achieves 32dB-42dB SNDR over a 10MHz-50MHz BW while consuming 24μW, giving a 3-10fJ/conv-step FoM.

11-3 - 11:20
A 6b 46GS/s ADC with >23GHz BW and Sparkle-Code Error Correction, Y. Duan and E. Alon, Univ. of California, Berkeley, USA

This paper presents a 6b 46GS/s 72-way hierarchically time-interleaved asynchronous SAR ADC utilizing cascode samplers to achieve >23GHz BW. A back-end meta-stability correction circuit enables sparkle-code error-free operation over 1e10 samples. The 28nm FDSOI ADC achieves 27dB SNDR (low frequency)/25.2dB (at 23.5GHz) while consuming 381mW from 1.05V/1.6V supplies and occupies 0.14mm^2.

11-4 - 11:45
A 14b 750MS/s DAC in 20nm CMOS with <-168dBm/Hz Noise Floor beyond Nyquist and 79dBc SFDR Utilizing a Low Glitch-Noise Hybrid R-2R Architecture, S. M. Lee, D. Seo, S. M. Taleie, D. Kong, M. J. McGowan, T. Song, G. Saripalli, J. Kuo and S. Bazarjani, Qualcomm Technologies, Inc., USA

A 14b 750MS/s 21.1mW current steering digital-to-analog converter (DAC) is presented, which maintains <-168dBm/Hz noise spectral density beyond the Nyquist frequency to minimize TX leakage in SAW-less FDD LTE. A hybrid wideband R-2R LSB segmentation with an impedance attenuator minimizes glitch noise across process and temperature without requiring accurate scaling of switches and switch drivers. SFDR of 79dBc is achieved at 15MHz with a distortion cancellation circuit. The DAC occupies 0.47mm^2 in a 20nm CMOS process with an on-chip calibration engine which guarantees 14b monotonicity.

11-5 - 12:10
A 16-bit 10Gsps Current Steering RF DAC in 65nm CMOS Achieving 65dBc ACLR Multi-Carrier Performance at 4.5GHz Fout, G. Engel, M. Clara, H. Zhu and P. Wilkins, Analog Devices, Inc., USA

This paper presents an RF DAC fabricated in a 65nm 1p7m CMOS process. The DAC is capable of >10Gsps operation dissipating ~800mW. At 3Gsps the SFDR > 70dBc beyond 1GHz and the IM3 performance is < -80dBc within the same range. Signal processing is incorporated into the DAC providing interpolation and modulation through the full Nyquist band. Features and performance enable a wide application range including cable infrastructure, wireless communications, instrumentation, defense & aerospace. These performance capabilities are enabled by a modified DAC switch output structure and a novel current source calibration scheme.

Luncheon Talk [Suzaku I]

Thursday, June 18, 12:45-14:05

Organizers: S. Inaba, Toshiba Electronics Korea Corp.
M. Motomura, Hokkaido Univ.

DASSAI: Innovating Sake Brewing with Massive Usage of Data and IT, K. Sakurai, Asahi Shuzo Co., Ltd.

It has been believed that Sake, a Japanese traditional rice wine, can only be brewed by people called TOJI, the Sake specialists experienced for more than several 10s of years. To the contrary, DASSAI, award winning Sake famous for its fruity flavor and smooth taste, does not rely on TOJI at all: It is brewed using a really scientific approach based on data measurement and analytics, during the whole process of brewing (polishing, washing, steaming, fermenting, etc.), as well as for controlling the quality of the ingredients (rice, water and koji). Asahishuzou, the DASSAI brewer, is now encompassing cloud-based rice farming for shipping DASSAI at even better quality with larger quantity. We can learn a lot from their story on their Sake innovation, such as what was a key for making a small business in a small village into world famous one, etc. During this luncheon, you can also taste, a little bit, how good DASSAI really is.

Technology / Circuits Joint Focus Session 3

Advanced Technology and Circuits for IoT [Suzaku II]

Thursday, June 18, 14:20-16:00

Chairpersons: H. Noda, Micron Memory Japan
E. Yeo, Marvell Semiconductor

JFS3-1 - 14:20 (Invited)
Technology Innovation in an IoT Era, A. Steegen, imec, Belgium

The further growth of billions of wirelessly connected devices requires a technology infrastructure that can handle a massive increase in storage, computing power and bandwidth, some of it available via cloud computing , to enable number crunching at very large scale and at high volume, low cost and low power. The IoT applications or 'smart devices' require the following technology enablers: ultra-low power, integration of memory and processing power to drive context awareness, security, advanced communication using smart antennas and improved analog performance, compactness by co-integration or stacking of heterogeneous systems.

JFS3-2 - 14:45
Fabrication of a 3000-6-Input-LUTs Embedded and Block-Level Power-Gated Nonvolatile FPGA Chip Using p-MTJ-Based Logic-in-Memory Structure, D. Suzuki, M. Natsui, A. Mochizuki, S. Miura, H. Honjo, H. Sato, S. Fukami, S. Ikeda, T. Endoh, H. Ohno and T. Hanyu, Tohoku Univ., Japan

A nonvolatile FPGA (NVFPGA) test chip, where 3000 6-input lookup table (LUT) circuits are embedded, is fabricated under 90nm CMOS/75nm perpendicular magnetic tunnel junction (p-MTJ) technologies. The use of a p-MTJ device makes data-backup-limitation free, which essentially eliminates damage control to nonvolatile storage devices. The use of a p-MTJ device also enables the extension towards dynamically reconfigurable logic paradigm. Since hardware components are shared among all the p-MTJ devices by the use of logic-in-memory structure, the effective area of the 6-input LUT circuit is reduced by 56% compared to that of an SRAM-based one. Moreover, block-level power gating, in which all the idle function blocks are optimally turned off in accordance with the operation mode, can minimize static power consumption of each tile. As a result, the total average power of the proposed NVFPGA is reduced by 81% in comparison with that of an SRAM-based FPGA under typical benchmark-circuit realizations.

JFS3-3 - 15:10
Low-Voltage Metal-Fuse Technology Featuring a 1.6V-Programmable 1T1R Bit Cell with an Integrated 1V Charge Pump in 22nm Tri-gate Process, S. H. Kulkarni, Z. Chen, B. Srinivasan, B. Pedersen, U. Bhattacharya and K. Zhang, Intel Corp., USA

This work introduces the first high-volume manufacturable metal-fuse technology in a 22nm tri-gate high-k metal-gate CMOS process. A high-density array featuring a 16.4μm^2 1T1R bit cell is presented that delivers a record low program voltage of 1.6V. This low-voltage operability allows the array to be coupled with logic-voltage power delivery circuits. A charge pump voltage doubler operating on a 1V voltage rail is demonstrated in this paper with healthy fusing yield.

JFS3-4 - 15:35
Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC, S. C. Song, J. Xu, N. N. Mojumder, K. Rim, D. Yang, J. Bao, J. Zhu, J. Wang, M. Badaroglu, V. Machkaoutsan, P. Narayanasetti, B. Bucki, J. Fischer and G. Yeap, Qualcomm Technologies, Inc., USA

We systematically investigated the impact of R and C scaling to 7nm node (N7) by accounting for FEOL and BEOL holistically. Speed-power performance of plainly scaled N7 turns out to be degraded compared to previous node. BEOL wire resistance (R_{wire}) multiplied by logic gate input pin cap (C_{pin}), $R_{wire}\times C_{pin}$, is identified as a major limiter of performance and power at N7. Reducing C_{pin} is crucial to mitigate abruptly rising BEOL R_{wire} effect. Depopulation of fin is one of most effective methods to reduce Cpin, and scale the logic gate area. Air Spacer (AS) on transistor sidewall further reduces C_{pin}. Careful choice of routing metal stack ameliorates adverse effect of R_{wire}. Wrap-Around-Contact (WAC) over Source and Drain of scaled fin pitch (P_{fin}) is needed to reduce transistor resistance (R_{tr}). Fin depopulation with other cost effective process innovations significantly improve Power-Performance-Area-Cost (PPAC) of N7, enabling continued scaling of mobile SoC.

SESSION 12

DRAM [Suzaku III]

Thursday, June 18, 14:20-16:00

Chairpersons: K. Sohn, Samsung Electronics Co., Ltd.
J. T. Pawlowski, Micron Technology, Inc.

12-1 - 14:20
A 4×9 Gb/s 1 pJ/b NRZ/Multi-Tone Serial-Data Transceiver with Crosstalk Reduction Architecture for Multi-Drop Memory Interfaces in 40nm CMOS, K. Gharibdoust*, A. Tajalli*,** and Y. Leblebici*, *EPFL and **Kandou Bus, Switzerland

An aggregated 36Gb/s 4-lanes mixed NRZ/multi-tone transceiver for multi-drop bus (MDB) memory interfaces is designed and fabricated in 40nm CMOS technology. The proposed architecture achieves 1 pJ/bit power efficiency for a MDB channel with 45 dB loss at 3 GHz. The multi-tone nature of the proposed transceiver is employed to properly reduce crosstalk (Xtalk) induced noise and to improve overall power efficiency.

12-2 - 14:45
A 6.4Gb/s/pin at Sub-1V Supply Voltage TX-Interleaving Technique for Mobile DRAM Interface, C.-K. Lee, M. Ahn, D. Moon, K. Kim, Y.-J. Eom, W.-Y. Lee, J. Kim, S. Yoon, B. Choi, S. Kwon, J.-Y. Park, S.-J. Bae, Y.-C. Bae, J.-H. Choi, S.-J. Jang and G. Jin, Samsung Electronics Co., Ltd., Korea

A 6.4Gb/s TX-interleaving (TI) technique at sub-1V supply voltage is implemented with 25nm DRAM process for the future mobile DRAM interface which requires 51.2 GBps (2X Bandwidth of LPDDR4). A newly proposed 2-channel TX interleaving technique with a bootstrapping switch can save power consumption drastically by eliminating repeaters, while operating at 6.4 Gb/s with 40 % enhancement of I/O power efficiency compared to that of the LPDDR4.

12-3 - 15:10
A 4.35Gb/s/pin LPDDR4 I/O Interface with Multi-VOH Level, Equalization Scheme, and Duty-Training Circuit for Mobile Applications, H.-K. Jung, J. Yang, J. Lee, H. Ko, H. Lee, T. Song, J. Shim, S.-K. Lee, K. Song, D.-K. Kim, H. Kim and Y. Kim, SK hynix, Korea

A 4.35Gb/s/pin LPDDR4 I/O interface with multi-VOH level, equalization scheme and Duty-Training Circuit (DTC) is presented. A Low Voltage-Swing Terminated Logic (LVSTL) driver using 4-to-1 multiplexer is implemented to the transmitter. A DTC to adjust the CK duty is implemented to the receiver. In addition, a ZQ calibration scheme for Multi-VOH level is also presented. Designed schemes are compatible with the LPDDR4 standard. Power efficiency for the I/O interface is about 2.3mW/Gb/s/pin with 1.1V supply in 2y-nm DRAM process, which is 31% lower than that of LPDDR3.

12-4 - 15:35
A Computer Designed Half Gb 16-Channel 819Gb/s High-Bandwidth and 10ns Low-Latency DRAM for 3D Stacked Memory Devices Using TSVs, P.-W. Luo*, C.-K. Chen*, Y.-H. Sung**, W. Wu***, H.-C. Shih*, C.-H. Lee*, K.-H. Lee**, M.-W. Li**, M.-C. Lung**, C.-N. Lu**, Y.-F. Chou*, P.-L. Shih**, C.-H. Ke**, C. Shiah**, P. Stolt***, S. Tomishima***, D.-M. Kwai*, B.-D. Rong**, N. Lu**, S.-L. Lu*** and C.-W. Wu*, *ITRI, **Etron Technology, Taiwan and ***Intel Corp., USA

Presented is a novel half Gb DRAM device for 3D stacked systems utilizing TSV. It is designed through the use of a new computer-aided design methodology and which realizes 819 Gb/s bandwidth across 16 channels and <10ns read latency on a 45nm DRAM process. The architecture is based on small subarrays with short WL and BL to realize the low latency and energy efficiency. We also integrated several circuit techniques, including adaptive power to speed-up access time and banks rotation to reduce thermal issues. The proposed device is also estimated in a system simulation that shows that the power efficiency is higher than comparable systems.

Technology / Circuits Joint Focus Session 4

3D and Heterogeneous Integration [Suzaku II]

Thursday, June 18, 16:15-17:55

Chairpersons: B. Sheu, TSMC
J. L. Nilles, Texas Instruments

JFS4-1 - 16:15
Active-Lite Interposer for 2.5 & 3D Integration, G. Hellings, M. Scholz, M. Detalle, D. Velenis, M. de Potter de ten Broeck, C. Roda Neve, Y. Li, S. Van Huylenbroek, S.-H. Chen, E.-J. Marinissen, A. La Manna, G. Van der Plas, D. Linten, E. Beyne and A. Thean, imec, Belgium

Adding functionality to a passive Si interposer used in 2.5/3D integration, can result in system cost reductions. In this work, active components (diodes, BJT, ...) have been integrated on Si interposer using a new low-mask process flow. This low-cost process enables: (1) to move part of the area hungry ESD protection from the stacked dies to the interposer; (2) the realization of pre-bond testable interposers (DFT); and (3) components for analog circuits (diodes, npn, SCR, resistor).

JFS4-2 - 16:40
An 82%-Efficient Multiphase Voltage-Regulator 3D Interposer with On-Chip Magnetic Inductors, K. Tien*, N. Sturcken**, N. Wang***, J.-W. Nah***, B. Dang***, E. O'Sullivan***, P. Andry***, M. Petracca****, L. P. Carloni*, W. Gallagher*** and K. Shepard*, *Columbia Univ., **Ferric Inc., ***IBM T. J. Watson Research Center and ****Cadence Design Systems, USA

This paper presents a three-dimensional (3D) fully integrated high-speed multiphase voltage regulator. A complete switched-inductor regulator is integrated with a four-plane NoC in a two-high chip stack combining integrated magnetics, through-silicon vias (TSVs), and 45-nm SOI CMOS devices. Quasi-V^2 hysteretic control is implemented over eight injection-locked fixed-frequency phases to achieve fast response, steady-state regulation, and fixed switching frequency. Peak efficiency of 82% for conversion from 1.66 V to 0.83 V is observed at a 150 MHz per-phase switching frequency. This is the first demonstration of high-speed voltage regulation using on-chip magnetic-core inductors in a 3D stack and achieves sub-µs dynamic supply voltage scaling for high-density embedded processing applications.

JFS4-3 - 17:05
15 dB Conversion Gain, 20 MHz Carrier Frequency AM Receiver in Flexible a-IGZO TFT Technology with Textile Antennas, K. Ishida*, R. Shabanpour*, T. Meister*, B. K. Boroujeni*, C. Carta*, L. Petti**, N. Münzenrieder**, G. A. Salvatore**, G. Tröster** and F. Ellinger*, *Technische Universität Dresden, Germany and **Swiss Federal Institute of Technology Zurich, Switzerland

This paper presents an AM receiver implemented in a flexible a-IGZO TFT technology. The circuit consists of a four-stage cascode amplifier at the RF input, a detector based on a source follower, and a common source circuit for the baseband amplification. The measured conversion gain is very flat and exceeds 15 dB from 2 to 20 MHz carrier frequency range, which covers a relevant portion of the shortwave radio band. The 3 dB-bandwidth of the audio signal is 400 Hz to 10 kHz, which is comparable to the so-called voice band, and it is also suitable to low-rate data communication. In addition, an integrated demonstration of the AM receiver and textile antennas is carried out. The flexible a-IGZO receiver successfully detected the baseband signal through the textile antennas, demonstrating for the first time wireless transmission for this class of technologies.

JFS4-4 - 17:30
Reconstruction of Multiple-User Voice Commands Using a Hybrid System Based on Thin-Film Electronics and CMOS, L. Huang, J. Sanz-Robinson, T. Moy, Y. Hu, W. Rieutort-Louis, S. Wagner, J. C. Sturm and N. Verma, Princeton Univ., USA

This paper presents a system consisting of an array of thin-film microphone channels on glass, which can be formed on large substrates. Each microphone channel consists of a polyvinylidene difluoride (PVDF) piezoelectric transducer as well as amplifier and scan circuits based on amorphous-silicon (a-Si) thin-film transistors (TFTs). The scan circuits multiplex signals from multiple channels to a CMOS IC for readout. By spatially distributing the channels on a large substrate, audio signals from multiple simultaneous speakers in a space can be both acquired in closer proximity and separated, enabling a multi-user human-computer interface based on voice commands. To overcome low TFT performance in the scan circuits (which limits channel sampling to below the Nyquist rate), a signal reconstruction algorithm is proposed. An 8-channel system demonstrates acquisition and reconstruction of 2 simultaneous audio signals at 2m distance from the array.

SESSION 13

Sensors & Bio Imaging [Suzaku I]

Thursday, June 18, 16:15-17:55

Chairpersons: M. Ikeda, The Univ. of Tokyo
N. Verma, Princeton Univ.

13-1 - 16:15
A Self-Referenced VCO-Based Temperature Sensor with 0.034°C/mV Supply Sensitivity in 65nm CMOS, T. Anand*, K. A. A. Makinwa** and P. K. Hanumolu*, *Univ. of Illinois, USA and **Delft Univ. of Technology, The Netherlands

A VCO-based temperature sensor with low supply sensitivity is presented. Fabricated in a 65nm CMOS process, the 0.004mm^2 prototype operates with 1V supply and achieves a supply sensitivity of 0.034°C/mV and an inaccuracy of +0.9°C/-0.9°C and +2.3°C/-2.3°C from 0-100°C after 2-point calibration, with and without static non-linearity correction, respectively. For (programmable) resolutions of 1°C-to-0.3°C, the sensor draws 1nJ-to-3.4nJ per conversion, respectively.

13-2 - 16:40
A 10.6mm^3 Fully-Integrated, Wireless Sensor Node with 8GHz UWB Transmitter, H. Kim, G. Kim, Y. Lee, Z. Foo, D. Sylvester, D. Blaauw and D. Wentzloff, Univ. of Michigan, USA

This paper presents a complete, autonomous, wireless temperature sensor, fully encapsulated in a 10.6mm^3 volume. The sensor includes solar energy harvesting with an integrated 2 μAh battery, optical receiver for programming, microcontroller and memory, 8GHz UWB transmitter, and miniaturized custom antennas with a wireless range of 7 meters. Full, stand-alone operation was demonstrated for the first time for a system of this size and functionality.

13-3 - 17:05
A 4.84mW 30fps Dual Frequency Division Multiplexing Electrical Impedance Tomography SoC for Lung Ventilation Monitoring System, Y. Lee, K. Song and H.-J. Yoo, KAIST, Korea

Lung ventilation monitoring electrical impedance tomography (EIT) SoC is implemented in 0.18μm CMOS technology. A dual frequency division multiplexing (DFDM) method is proposed to extract accurate lung ventilation. To realize the DFDM, the proposed EIT SoC adopts a dual frequency current generator (DFCG) and a dual frequency read-out front-end (DFRF) to process the two frequencies in one channel at once. Consequently, 65.1% of power consumption and 71.5% of area are reduced in each channel. In the DFCG, dynamic element matching (DEM) and adaptive quantization (AQ) techniques are adopted to achieve -46dBc total harmonic distortion. In the DFRF, a weaver demodulator (WD) and a trimmed notch filter combined with low-pass filter (TN-LPF) reduce the settling time of the sensor front-end by 83.3% (0.17ms) to achieve the 30fps real-time operation with 32 electrodes. The proposed EIT SoC is successfully verified by both in-vitro and in-vivo test and achieved 95.35% accuracy.

13-4 - 17:30
A Fully Integrated CMOS Fluorescence Biosensor with On-Chip Nanophotonic Filter, L. Hong, S. McManus, H. Yang and K. Sengupta, Princeton Univ., USA

Affinity-based fluorescence sensing has been one of the key enabling technologies in biomolecular sensing, used for detection of proteins, DNAs, toxins, bacteria, etc, and remains one of the most sensitive, specific, robust, and widely used diagnostics methodology. In absence of high-performance integrated optical filters, miniaturization of a fluorescence sensing system in CMOS has relied on time-resolved techniques with synchronized sources or externally grown optical filters and/or collimators. This paper presents a nanophotonic-electronic co-design approach towards fully-integrated fluorescence biosensor with on-chip copper-interconnect based nanoplasmonic filters. The filters demonstrate a measured extinction ratio of greater than 51dB in the excitation/emission bands for a class of quantum-dot based fluorescence tags. Integrated with these filters, the sensor platform is a correlated double sampling architecture which achieves femtowatt photon sensitivity. Detection sensitivity of 47 zeptomoles of quantum-dots was experimentally demonstrated, making the chip a low-cost, fully integrated, high-performance, and fully scalable biosensor for point-of-care applications.

SESSION 14

Application-Specific IOs [Suzaku III]

Thursday, June 18, 16:15-17:55

Chairpersons: J.-Y. Sim, POSTECH
R. Navid, Rambus Inc.

14-1 - 16:15
An Efficient and Resilient Ultra-High Speed Galvanic Data Isolator Leveraging Broad-Band Multi Resonant Tank Electro-Magnetic Coupling, S. Sankaran*, B. Kramer*, G. Howard, B. Sutton*, R. Walberg*, V. Khanolkar*, R. Payne* and M. Morgan*, *Texas Instruments Inc., USA

A novel technology for galvanic data isolation is demonstrated. The integrated high-speed isolated data transfer system-in-package (SIP) supports a maximum data-rate of 2.5Gbps at ~20pJ/bit and is resilient to common-mode-transients (CMTs) >150kV/μs at speeds <600Mbps, both while meeting a bit-error-rate (BER) $<10^{-12}$. The SIP exceeds the standards body requirements on isolation rating for human safety and extends state-of-art by ~4X in speed and >3X in immunity to CMT.

14-2 - 16:40
A 100-GbE Reverse Gearbox IC in 40nm CMOS for Supporting Legacy 10- and 40-GbE Standards, T. Yoon*, J.-Y. Lee*, K. Han**, J. Lee**, S. Lee**, T. Kim**, H. Won*, J. Park** and H.-M. Bae*, *KAIST and **TeraSquare Inc., Korea

This paper presents the industry's first low-power 100-Gigabit Ethernet (GbE) multi-link gearbox (MLG) IC, which facilitates transport of independent 10-GbE and 40-GbE signals to 4×25G physical layers implementing 100GBASE-R. The IC consumes only 1.37-W while implementing complicated reverse gearbox functionality. The measured TX jitter from the 25-Gb/s lane is 1.6-ps_{rms}, and the recovered clock jitter is 0.5-ps_{rms}. The measured RX input sensitivity for a BER 10^{-12} is 42-mV_{ppd}. The proposed gearbox IC, fabricated in a 40nm CMOS process, occupies 3.7×3.4-mm^2. The power consumption of RX and TX in 25G interfaces are 47-mW and 51-mW, respectively, and those of a 10G interfaces are 24-mW and 25-mW, respectively. Gearbox functionalities are verified with embedded self-test logics.

14-3 - 17:05
A 2.7mW/Channel 48-to-1000MHz Direct Sampling Full-Band Cable Receiver, J. Wu*, G. Cusmai*, A. (W.-T.) Chou*, T. Wang*, B. Shen*, V. Periasamy*, M.-H. Hsieh**, C.-Y. Chen*, L. He*, L. Tan*, A. Padyana*, C.-H. Yang**, G. Unruh*, J. (K. L.) Wong*, J.-J. Hung*, M. Brandolini*, S.-T. Lin**, X. Chen*, Y. Ding**, Y.-J. Ko**, Y. Shin*, A. Hung*, B. Chen*, C. Dang*, D. Lakshminarasimhan*, I. (H.) Liu*, J. Lin*, K. Lai*, L. Wassermann*, A. Shrivastava*, C.-M. Hsiao**, C.-S. Huang**, J. Chen*, L. Krishnan*, N.-Y. Wang*, P.-E. Su*, T. Li*, W.-T. Shih**, Y.-C. Yang**, P. Cangiane*, R. Perlow*, W. Ngai*, H.-S. Huang**, J. Y. C. Chang*, X. Jiang*, A. Venes* and R. Gomez*, *Broadcom Corp., USA and **Broadcom Corp., Taiwan

We present a direct sampling full-band capture receiver for cable and digital TV applications. It consists of a 28nm CMOS ADC-based direct sampling receiver and a 0.18μm BiCMOS LNA. It is capable of receiving 158 channels from 48MHz to 1000MHz simultaneously, achieving up to 10Gb/s data throughput, while exceeding DOCSIS requirements. The CMOS receiver occupies 1mm^2 area while consuming 300mW. The LNA consumes 130mW. The total power dissipation from the receiver is 2.7mW per 6MHz channel.

14-4 - 17:30
A Fully Integrated IEEE 802.15.7 Visible Light Communication Transmitter with On-Chip 8-W 85% Efficiency Boost LED Driver, B. Hussain, F. Che, F. Zhang, T. S. Yim, L. Cheng, W.-H. Ki, C. P. Yue and L. Wu, The Hong Kong Univ. of Science and Technology, China

This paper presents the first IEEE 802.15.7 PHY-I standard compliant visible light communication (VLC) transmitter and LED driver SoC for location-based applications using standard white LED lights as beacons or broadcasters. Implemented in a 0.35μm CMOS process with 20-V high-voltage device, the mixed-signal SoC integrates a baseband DSP unit, a VLC modulator, and a switching boost converter with an on-chip power MOSFET. Designed to drive an array of up to 4x5 LEDs using batteries, the boost converter generates an output at 6-20 V from an input at 3-5V with a 92% peak efficiency and an 8-W rating. Measured VLC data rate up to 266 kb/s with 2^{11}-1 PRBS inputs is achieved at a PER of <10% and transmission efficiency of 5 nJ/bit. The LED driver can simultaneously support nine dimming levels and VLC.

Circuits Evening Panel Discussion 1

Is University Circuit Design Research and Education Keeping Up with Industry Needs? [Suzaku I]

Thursday, June 18, 20:00-22:00

Organizers: P. Yue, Hong Kong Univ. of Science and Technology
R. Navid, Rambus Inc.

Moderator: P. Yue, Hong Kong Univ. of Science and Technology

Panelists: B. Sheu, TSMC
A. Matsuzawa, Tokyo Institute of Technology
K. Asada, The Univ. of Tokyo
L. Loh, MediaTek Inc.
K. Makinwa, Delft Univ. of Technology
S. Borkar, Intel Corp.
V. Stojanovic, Univ. of California, Berkeley

As traditional circuit design reaches a higher level of maturity, the role of educational institutions is changing. For new graduate students entering the field, system-level research that caters to novel emerging applications provides an attractive alternative to traditional circuit-focused topics for PhD dissertations. In response to this paradigm shift, some institutions have opted to slow down faculty hiring in traditional circuit design areas in favor of emerging technologies and applications including 3D IC, MEMS, bio-technology, wearable electronics and internet of things. Is this trend detrimental to the industry as it is still very much in need of constant flow of fresh circuits talent? A panel of experts from industry and academia will tackle this question along with other concerns such as: Is it necessary for students to carry out their circuit research in advanced technologies or should they focus on just fundamentals? Are professors training students to design ICs for better Figure of Merits or to be creative designers?

Circuits Evening Panel Discussion 2

Wearable Electronics: Still an Oasis or Just a Mirage for the Semiconductor Industry? [Suzaku II, III]

Thursday, June 18, 20:00-22:00

Organizers: Y. Shu, MediaTek Inc.
N. Verma, Princeton Univ.

Moderator: N. Verma, Princeton Univ.

Panelists: K. Yano, Hitachi, Ltd.
T. Someya, The Univ. of Tokyo
H.-J. Yoo, KAIST
K. Vasanth, Texas Instruments Inc.
D. Blaauw, Univ. of Michigan
L. Krishnamurthy, Intel Corp.
S. J. Kim, Samsung Electronics Co., Ltd.

Wearable devices have been on the mind of the semiconductor industry for several years now. The vision was of a highly sensorized human, with electronic devices providing localized, always-available functionality for a range of applications, including medical, health and wellness, lifestyle, etc. But, has this vision panned out? Is the technology there? Was there any application-level value to begin with? What is the relationship with broader sensing visions (e.g., IoT)? The collective wisdom of industrial and academic research over the last five years has made some progress in these areas - what have we learned? and how might the vision be revised? This session brings together panelists representing commercialization, emerging technologies, medical applications, and broader questions facing the domain of wearable electronics to tackle some of these questions.

SESSION 15

Ultra-High Speed Receivers [Suzaku I]

Friday, June 19, 8:30-10:10

Chairpersons: Y. Tomita, Fujitsu Laboratories Ltd.
P. Hanumolu, Univ. of Illinois

15-1 - 8:30
A 32 Gb/s 0.55 mW/Gbps PAM4 1-FIR 2-IIR Tap DFE Receiver in 65-nm CMOS, O. Elhadidy, A. Roshan-Zamir, H.-W. Yang and S. Palermo, Texas A&M Univ., USA

A PAM4 serial I/O receiver efficiently implements a decision feedback equalizer (DFE) that employs 1-FIR and 2-IIR taps for first post-cursor and long-tail ISI cancellation, respectively. The use of a single-clock phase two-stage regenerative comparator simplifies the quarter-rate receiver design and allows for sufficient gain to support PAM4 DFE. Optimization of the direct-feedback design's timing is achieved by cancelling the critical first post-cursor multi-levelISI directly at the comparator, while performing the remaining taps' ISI subtraction in a preceding current integration summer for improved sensitivity. Fabricated in GP 65-nm CMOS, the receiver occupies 0.0138 mm^2 area and achieves power efficiencies of 0.55 and 0.52 mW/Gbps with 32 Gb/s and 25 Gb/s PAM4 data, respectively.

15-2 - 8:55
A 40-Gb/s 9.2-mW CMOS Equalizer, A. Manian and B. Razavi, Univ. of California, Los Angeles, USA

A 40-Gb/s equalizer incorporates a one-stage CTLE with 5.5-dB boost, a one-tap discrete-time linear equalizer with 5.4-dB boost, a two-tap half-rate/quarter-rate DFE, and charge-steering techniques. Realized in 45-nm CMOS technology, the equalizer achieves BER < 10^{-12} with a clock phase margin of 0.28 UI with a channel loss of 20 dB at Nyquist.

15-3 - 9:20
A 5.9mW/Gb/s 7Gb/s/pin 8-Lane Single-Ended RX with Crosstalk Cancellation Scheme Using a XCTLE and 56-Tap XDFE in 32nm SOI CMOS, A. Cevrero*, C. Aprile**, P. A. Francese*, U. Bapst*, C. Menolfi*, M. Braendli*, M. Kossel*, T. Morf*, L. Kull*, H. Yueksel*, I. Oezkaya*, Y. Leblebici**, V. Cevher** and T. Toifl*, *IBM Research and **EPFL, Switzerland

This work reports an 8-lane single-ended RX featuring compact and low power far-end crosstalk (FEXT) cancellation circuits. The RX data-path consists of a cross continuous-time linear equalizer (XCTLE) to remove FEXT by nearest aggressors within the channel bundle. Residual post-cursor FEXT is suppressed by a direct feedback 7x8-tap cross decisionfeedback equalizer (XDFE). A CTLE and 8-tap DFE equalize single-ended channels with 28dB insertion loss at Nyquist frequency without TX FFE. The circuit, fabricated in 32nm SOI CMOS, was measured to receive 7Gb/s/pin PRBS11 data at BER< 10^{-12} with 12.5%UI margin. It occupies 300x350μm^2 with an energy efficiency of 5.9mW/Gb/s.

15-4 - 9:45
A 60Gb/s 173mW Receiver Frontend in 65nm CMOS Technology, J. Han*, Y. Lu**, N. Sutardja*, K. Jung* and E. Alon*, *Univ. of California, Berkeley and **Qualcomm Atheros Inc., USA

This paper presents a 65nm CMOS 60Gb/s receiver frontend incorporating CTLE, FFE, DFE, output slicers and clock generation as well as distribution circuits. Current-integration along with cascode gain control is used to maintain equalizer linearity under varying gain without sacrificing power consumption. Interleaved deserializing slicers achieve the high gain required for adaptive error sampling. The receiver operates error free over >1e12 bits at 60Gb/s, occupies 0.16mm^2, and consumes 173mW.

SESSION 16

Oscillators [Suzaku II]

Friday, June 19, 8:30-10:10

Chairpersons: J. Lee, National Taiwan Univ.
A. Molnar, Cornell Univ.

16-1 - 8:30
A Dithering-Less 54.79-to-63.16GHz DCO with 4-Hz Frequency Resolution Using an Exponentially-Scaling C-2C Switched-Capacitor Ladder, Z. Huang and H. C. Luong, Hong Kong Univ. of Science and Technology, China

An exponentially-scaling C-2C switched-capacitor ladder is proposed for mm-Wave DCOs to achieve high frequency resolution with small chip area. The 65nm-CMOS DCO prototype measures frequency resolution of 4Hz over a frequency range from 54.79 to 63.16GHz with phase noise of -90.7~-94.1dBc/Hz at 1MHz frequency offset while consuming 18mW, corresponding to FOM_T from -176.6 to -180dBc/Hz. The DCO occupies a core area of 0.1 mm^2 with only 0.012mm^2 for the C-2C switched ladder capacitor.

16-2 - 8:55
A -194 dBc/Hz FOM Interactive Current-Reused QVCO (ICR-QVCO) with Capacitor-Coupling Self-Switching Sinusoidal Current Biasing (CSSCB) Phase Noise Reduction Technique, K.-I. Wu*, I.-S. Shen**, C. F. Jou** and C. C.-P. Chen*, *National Taiwan Univ. and **National Chiao Tung Univ., Taiwan

This paper proposed a novel interactive current-reused QVCO (ICR-QVCO) architecture based on capacitor-coupling self-switching sinusoidal current biasing (CSSCB) phase noise reduction technique. These interactive generated quadrature outputs have minimum phase error arising from the mismatch due to process variation and construct the better quadrature phase relationship than ones with conventional QVCO structures. The measured phase noise at an offset of 1 MHz from 4.84 GHz is -125.84 dBc/Hz, which correspond to FOM of -194 dBc/Hz.

16-3 - 9:20
A 99nW 70.4kHz Resistive Frequency Locking On-Chip Oscillator with 27.4ppm/ºC Temperature Stability, M. Choi, S. Bang, T.-K. Jang, D. Blaauw and D. Sylvester, Univ. of Michigan, USA

We present a low power on-chip oscillator for system-on-chip designs. The oscillator introduces a resistive frequency locking loop topology where the equivalent resistance of a switch-capacitor is match to a temperature compensated resistor. The approach eliminates the traditional comparator from the oscillation loop which constitutes a major portion of the power consumption and limits temperature stability in conventional relaxation oscillators. The oscillator is fabricated in 0.18μm CMOS and exhibits 27.4ppm/°C and <7ppm long terms stability while consuming 99.4nW at 70.4 kHz.

16-4 - 9:45
4.2 pW Timer for Heavily Duty-Cycled Systems, P. M. Nadeau, A. Paidimarri and A. P. Chandrakasan, Massachusetts Institute of Technology, USA

An ultra-low energy wake-up timer suitable for heavily duty-cycled systems is presented. A prototype implemented in 0.18μm CMOS consumes 4.2pW of power for 18Hz of oscillation (0.23pJ/cycle). A dynamic 3-stage architecture, duty-cycled current-source, and low operating voltage (0.6V) enabled by a voltage boost circuit all contribute to the improved efficiency.

SESSION 17

Low-Power and Secure Design [Suzaku III]

Friday, June 19, 8:30-10:10

Chairpersons: K. Fujii, NTT Microsystem Integration Labs.
J. Tschanz, Intel Corp.

17-1 - 8:30
A Low-PDP and Low-Area Repeater Using Passive CTLE for On-Chip Interconnects, M.-S. Chen, M.-C. F. Chang and C.-K. K. Yang, Univ. of California, Los Angeles, USA

On-chip interconnects play an important role in large digital systems. To accommodate the dissipative wire channels and to achieve an acceptable latency, inverter repeaters are extensively used in on-chip links under the cost of increased power, area, and routing complexity. This paper presents an improved repeater circuit that preserves the advantages of the inverter repeater and achieves a lower power, delay, and area by applying proper equalization. Designed and measured in 65nm CMOS technology, the proposed repeater achieves 44% lower power-delay product (PDP) while occupies 46% lower area. The proposed circuit shows a great potential for improving the performance of modern integrated circuit design.

17-2 - 8:55
1.32GHz High-Throughput Charge-Recovery AES Core with Resistance to DPA Attacks, S. Lu, Z. Zhang and M. Papaefthymiou, Univ. of Michigan, USA

A 128-bit Advanced Encryption Standard (AES) core targeted for high-performance security applications is fabricated in a 65nm CMOS technology. A novel charge-recovery logic family, called Bridge Boost Logic (BBL), is introduced in this design to achieve switching-independent energy dissipation for an intrinsic high resistance against Differential Power Analysis (DPA) attacks. Based on measurements, the AES core achieves a throughput of 16.90Gbps and power consumption of 98mW, exhibiting 720x higher DPA resistance and 30% lower power than its conventional CMOS counterpart at the same clock frequency.

17-3 - 9:20
A Robust -40 to 120°C All-Digital True Random Number Generator in 40nm CMOS, K. Yang, D. Blaauw and D. Sylvester, Univ. of Michigan, USA

An all-digital True Random Number Generator (TRNG) harvesting entropy from the collapse of 2 edges injected into one even-stage ring is fabricated in 40nm CMOS. A configurable ring and tuning loop provides robustness across a wide range of temperature (-40 to 120°C), voltage (0.6 to 0.9V), process variation, and external attack. The dynamic tuning loop automatically configures the ring to meet a sufficient collapse time, thereby maximizing entropy. All dies pass all NIST randomness tests across all measured operating conditions and power supply attacks. The all-digital TRNG occupies only 836μm^2 and consumes 23pJ/bit at nominal 0.9V and 11pJ/bit at 0.6V.

17-4 - 9:45
A 3.07μm^2/Bitcell Physically Unclonable Function with 3.5% and 1% Bit-Instability across 0 to 80°C and 0.6 to 1.2V in a 65nm CMOS, J. Li and M. Seok, Columbia Univ., USA

This paper presents a circuitry for physically unclonable function, generating a unique and stable key for security-oriented applications. The key is generated from an array of pairs of voltage-compensated proportional-to-absolute-temperature generators. The difference between two analog outputs of a pair is voltage- and temperature-compensated yet sensitive mostly only to random threshold-voltage variation. As compared to the state of the art [3-4], the proposed design has an 8.3X smaller bitcell or 3.66X higher robustness against noise and environmental variations.

SESSION 18

Wideband Over-Sampled ADCs [Suzaku I]

Friday, June 19, 10:30-12:35

Chairpersons: S. Dosho, Tokyo Institute of Technology
B. P. Ginsburg, Texas Instruments

18-1 - 10:30
A 75 MHz BW 68dB DR CT-ΣΔ Modulator with Single Amplifier Biquad Filter and a Broadband Low-Power Common-Gate Summing Technique, C. Briseno-Vidrios, A. Edward, A. Shafik, S. Palermo and J. Silva-Martinez, Texas A&M Univ., USA

A wide bandwidth, power efficient continuous-time ΣΔ modulator (CTΣΔM) is presented. The modulator introduces a 3rd order filter implemented with a lossless integrator and a multiple-feedback (MFB) single-amplifier biquad (SAB) with embedded loop stability compensation. An active summing block is implemented with a common-gate amplifier followed by a transimpedance amplifier (TIA) that achieves optimum bandwidth (BW) vs power consumption tradeoff, making it suitable for over GHz operation. Fabricated in 40 nm CMOS, and clocked at 3.2 GHz, the CTΣΔM achieves a signal-to-noise and distortion ratio (SNDR) of 64.9 dB over 75 MHz BW while consuming 22.8 mW of power. The obtained Walden's Figure of Merit (FoM) is 106 fJ/conv-step.

18-2 - 10:55
A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-Based CT ΔΣ ADC Using Dual Phase/Frequency Feedback in 65nm CMOS, K. Reddy*, S. Dey*, S. Rao*, B. Young*, P. Prabha* and P. K. Hanumolu**, *Oregon State Univ. and **Univ. of Illinois, USA

A wide bandwidth VCO-based continuous-time ΔΣ modulator that uses combined phase and frequency feedback to mitigate VCO non-linearity and ease DEM timing requirement is presented. Fabricated in 65nm CMOS process, the prototype modulator operates at 1.2GS/s and achieves 71.5dB SNDR in 50MHz bandwidth while consuming 54mW of power, which translates to an FoM of 176fJ/conv-step.

18-3 - 11:20
A 7.2 mW 75.3 dB SNDR 10 MHz BW CT Delta-Sigma Modulator Using Gm-C-Based Noise-Shaped Quantizer and Digital Integrator, T. Kim, C. Han and N. Maghari, Univ. of Florida, USA

A 3rd order continuous-time delta-sigma modulator using a Gm-C based noise-shaped integrating quantizer (NSIQ) with a digital back-end integrator is presented in this paper. By incorporating the back-end digital integrator, the conventional tradeoff between resolution and speed in time-based quantization is alleviated. Therefore by using only three clock edges and a low-power Gm-C, effective 4-bit quantization is achieved which also provides first order noise-shaping. The zero-crossing comparator is replaced by a preamplifier and three latches. The proposed modulator was fabricated in a 0.13μm CMOS process with an active area of 0.08mm^2. It operates at 640 MHz and achieves a peak SNDR of 75.3 dB and a peak SFDR of 94.1 dB in a 10 MHz bandwidth while consuming 7.2 mW from a 1.2V power supply.

18-4 - 11:45
A 16nm FinFet 19/39MHz 78/72dB DR Noise-Injected Aggregated CTSDM ADC for Configurable LTE Advanced CCA/NCCA Application, T.-K. Kao, P. Chen, J.-Y. Tsai and P.-C. Chiu, MediaTek Inc., Taiwan

A 39MHz bandwidth (BW) CTSDM ADC realized by aggregating two 19MHz BW CTSDM ADCs with a noise-injected technique is presented. The in-band noise is improved by 4.77dB by this technique. The ADC samples at 832MS/s, achieves 72dB DR in 39MHz BW and 78dB DR in 19MHz BW. This aggregated ADC is implemented in 16-nm FinFet technology with 0.23 mm^2 active area and 6.2 mW per ADC, and thereby achieves FoM_{DR} of 167.1dB in 39MHz BW, and FoM_{DR} of 173.4dB in 19MHz BW.

18-5 - 12:10
A 10/20/30/40 MHz Feed-Forward FIR DAC Continuous-Time ΔΣ ADC with Robust Blocker Performance for Radio Receivers, S. Loeda, J. Harrison, F. Pourchet and A. Adams, Broadcom Corp., Australia

The first (single-bit) feed-forward (FF) FIR DAC continuous-time (CT)-ΔΣ ADC is presented for cellular radio applications. It provides a robust loop delay compensation with no performance degradation in the presence of radio out-of-band blockers; a known drawback of FF CT-ΔΣ ADCs. At 20/30/40 MHz operation, the FOM is less than or equal to 36 fJ/conv. At 10 MHz operation, the FOM is 50 fJ/conv. The equivalent FOM for a 20-MHz-only design is 28 fJ/conv. It occupies 0.0194 mm^2 in 40 nm CMOS.

SESSION 19

SRAM and CAM [Suzaku II]

Friday, June 19, 10:30-12:35

Chairpersons: H. Yamauchi, Fukuoka Institute of Technology
V. Chandra, ARM Ltd.

19-1 - 10:30
A 0.094um^2 High Density and Aging Resilient 8T SRAM with 14nm FinFET Technology Featuring 560mV V_{MIN} with Read and Write Assist, K.-H. Koo, L. Wei, J. Keane, U. Bhattacharya, E. A. Karl and K. Zhang, Intel Corp., USA

A 0.094μm^2 8T SRAM bitcell is developed for a 14nm technology featuring FinFET transistors with a 70nm contacted gate pitch. The bitcell and supporting circuitry are optimized for high density and aging tolerance. Supply collapse and wordline boosting techniques are applied for write V_{MIN} assist. A delayed keeper is used for read V_{MIN} improvement. A 400MHz V_{MIN} of 560mV is achieved with the proposed design at −10°C in volume manufacturing.

19-2 - 10:55
14nm FinFET Based Supply Voltage Boosting Techniques for Extreme Low Vmin Operation, R.V. Joshi*, M. Ziegler*, H. Wetter**, C. Wandel** and H. Ainspan*, *IBM Research, USA and **IBM, STG, Germany

This paper presents new dynamic supply and interconnect boosting techniques for low voltage SRAMs and logic in deep 14nm FinFET technologies. The capacitive coupling in a FinFET device is used to dynamically boost the virtual logic and array supply voltage, improving V_{min}. Hardware measurements show a 2.5-3x access time improvement at lower voltages and a functional V_{min} down to 0.3V. Results are supported by novel physics-based capacitance extraction and novel superfast statistical circuit simulations.

19-3 - 11:20
A Reconfigurable Sense Amplifier with 3X Offset Reduction in 28nm FDSOI CMOS, M. Khayatzadeh*,****, F. Frustaci**, D. Blaauw*, D. Sylvester* and M. Alioto***, *Univ. of Michigan, USA, **Univ. of Calabria, Italy, ***National Univ. of Singapore, Singapore and ****Oracle, USA

This work proposes an area-efficient approach to fully exploit redundancy in reconfigurable sense amplifiers (SAs). The proposed SA can combine/invert offsets of sub-unit SAs, reducing offset by up to 3.1× at iso-area in 28nm FDSOI.

19-4 - 11:45
A Configurable TCAM / BCAM / SRAM Using 28nm Push-Rule 6T Bit Cell, S. Jeloka*, N. Akesh**, D. Sylvester* and D. Blaauw*, *Univ. of Michigan and **Oracle, USA

Conventional Content Addressable Memory (BCAM and TCAM) uses specialized 10T / 16T bit cells that are significantly larger than 6T SRAM cells. We propose a new BCAM/TCAM that can operate with standard push-rule 6T SRAM cells, reducing array area by 2-5× and allowing reconfiguration of the CAM as an SRAM. Using a 6T 28nm FDSOI SRAM bit cell, the 64x64 (4kb) BCAM achieves 370 MHz at 1V and consumes 0.6fJ/search/bit.

19-5 - 12:10
1.8 Mbit/mm^2 Ternary-CAM Macro with 484 ps Search Access Time in 16 nm Fin-FET Bulk CMOS Technology, Y. Tsukamoto, M. Morimoto, M. Yabuuchi, M. Tanaka and K. Nii, Renesas Electronics Corp., Japan

A new bit-cell (BC) layout for ternary content-addressable memory (TCAM) is developed in a 16 nm Fin-FET process. The proposed BC is 15.8% smaller than the conventional BC. We design a 10kb TCAM macro which achieves the highest density of 1.8 Mbit/mm^2. Measurement shows that total active power in our proposed macro is 8% less than that in the conventional one. A 484 ps of search access time is observed at 0.8 V, which marks the world fastest operation cycle of 1.25 G search per second at this time.

SESSION 20

Power Management Circuits [Suzaku III]

Friday, June 19, 10:30-12:35

Chairpersons: C. Yoo, Hanyang Univ.
H. J. Bergveld, NXP Semiconductors

20-1 - 10:30
A 0.78mW/cm^2 Autonomous Thermoelectric Energy-Harvester for Biomedical Sensors, D. Rozgić and D. Marković, Univ. of California, Los Angeles, USA

A thin-film array-based thermoelectric energy-harvester (TEH) is integrated with heat-sink in 0.83cm^2 and attached to a power management unit built in 65nm CMOS. Analog-based maximum-power-point tracking leads to a 68% peak end-to-end efficiency and <20ms tracking time. A 645μW regulated output power is harvested from the head of a rat (effective 3.5K) implanted with our TEH, to demonstrate true energy autonomy in real environment while achieving a 7.9x improvement in regulated power density.

20-2 - 10:55
Solar Energy Harvesting System with Integrated Battery Management and Startup Using Single Inductor and 3.2nW Quiescent Power, D. El-Damak and A. P. Chandrakasan, Massachusetts Institute of Technology, USA

This paper presents a 3.2nW quiescent power solar energy harvesting system. The control circuit is designed in an asynchronous fashion that scales the effective switching frequency of the converter with the level of the power transferred. The on-time of the converter switches adapts dynamically to the input and output voltages for peak-current control and zero-current switching. The chip integrates self-startup, battery management, supplies 1V regulated rail with single inductor and supports power range of 10nW to 1μW. For input power of 500nW, the proposed system achieves an efficiency of 82%, including the control circuit overhead, while charging a battery at 3V from 0.5V input. In buck mode, it achieves a peak efficiency of 87% and maintains efficiency greater than 80% for output power of 50nW-1μW with input voltage of 3V and output voltage of 1V.

20-3 - 11:20
A 2.5-V, 160-μJ-Output Piezoelectric Energy Harvester and Power Management IC for Batteryless Wireless Switch (BWS) Applications, J. Yang, M. Lee, M.-J. Park, S.-Y. Jung and J. Kim, Seoul National Univ., Korea

A piezoelectric-based energy harvesting and power management IC that can supply a total energy of 160-μJ at 2.5V from a single button-pressing action to realize a batteryless wireless remote switch (BWS) is presented. The IC uses a 6:1 series-parallel switched-capacitor converter and a bias-flipping inductor to match the impedance, down-convert the voltage, and maximize the total energy harvested from a 300-mm^2 PMN-PT disc. Also, a step-down buck regulator employs a variable on-time PFM control to keep the initial charging loss below 12-μJ without degrading load regulation at 2.5V. Using this IC fabricated in a 0.25-μm HV CMOS, a batteryless wireless switch that can successfully transmit a 4-byte-long message over a 10-m distance is demonstrated.

20-4 - 11:45
A 144MHz Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation, C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier and G. Cauwenberghs, Univ. of California, San Diego, USA

This paper presents a CMOS fully-integrated resonant regulating rectifier (IR^3) for inductive power telemetry in implantable devices. Employing PWM and PFM feedback, the IR^3 achieves 1.87% of $\Delta V_{DD}/V_{DD}$ ratio despite a tenfold change in load with a 1nF decoupling capacitor. At 1V regulation of a 100μW load from a 144MHz RF input, the measured voltage conversion efficiency is greater than 92% at under 5.2mV_{pp} ripple and 54% power conversion efficiency. Implemented in 180nm SOI CMOS, the IR^3 circuit occupies 0.078mm^2 active area.

20-5 - 12:10
A 5.5W AC Input Converter-Free LED Driver with 82% Low-Frequency-Flicker Reduction, 88.2% Efficiency and 0.92 Power Factor, Y. Gao, L. Li and P. K. T. Mok, The Hong Kong Univ. of Science and Technology, China

This paper presents a $95V_{AC}$-$120V_{AC}$ mains powered converter-free LED driver for general lighting application. A quasi-constant power control scheme is proposed to significantly reduce the low-frequency-flicker, combined with a valley fill circuit to maintain good power factor performance. The driver achieves 88.2% efficiency and 0.92 PF with only 18% flicker at $110V_{AC}$ 60Hz input and does not require any magnetics or electrolytic capacitors.

SESSION 21

Delta-Sigma Modulators and Analog Techniques [Suzaku I]

Friday, June 19, 13:55-16:00

Chairpersons: Y.-S. Shu, MediaTek Inc.
Y. Chiu, Univ. of Texas at Dallas

21-1 - 13:55
A 0.7 V 256 µW ΔΣ Modulator with Passive RC Integrators Achieving 76 dB DR in 2 MHz BW, J. L. A. de Melo, J. Goes and N. Paulino, Universidade Nova de Lisboa, Portugal

A continuous-time (CT) delta-sigma modulator (ΔΣM), with 27.5 fJ/conv.-step energy efficiency, employing passive RC integrators is proposed. A simple differential pair is incorporated in the loop-filter between each passive RC integrator and, the extra required gain in the loop is obtained in the comparator. Due to the many design issues, such as the trade-off between RC variations and loop stability, the modulator is optimized using genetic algorithms (GAs). The 65 nm CMOS ΔΣM, occupying only 0.013 mm^2, dissipates 256 µW from a 0.7 V supply and achieves a peak SNDR of 69.1 dB with 2 MHz bandwidth (BW). The dynamic range (DR) reaches 76.2 dB, which corresponds to a $FoM_{Schreier}$ of 175.1 dB.

21-2 - 14:20
A 13-ENOB, 5 MHz BW, 3.16 mW Multi-Bit Continuous-Time ΔΣ ADC in 28 nm CMOS with Excess-Loop-Delay Compensation Embedded in SAR Quantizer, G. Wei, P. Shettigar, F. Su, X. Yu and T. Kwan, Broadcom Corp., USA

A 13-ENOB, 5 MHz BW, 3.16 mW 3-bit continuous-time ΔΣ ADC sampling at 432 MHz is presented. For power efficiency, this design utilizes a hybrid feedback feed-forward loop topology with SAR quantizer, feed-forward compensated amplifiers, and push-pull DACs. Further power efficiency is gained by performing excess-loop-delay compensation (ELDC) using the SAR quantizer SC-DAC, which reduces power overhead from ELDC to a negligible level. A 94 dB SFDR is achieved through feedback-DAC calibration. The 0.066 mm^2 design is fabricated in 28 nm CMOS and achieves FoMs of 36.4 fJ/step and 175.9 dB.

21-3 - 14:45
A Low-Power Gm-C-Based CT-ΔΣ Audio-Band ADC in 1.1V 65nm CMOS, I. Ahmed, J. Cherry, A. Hasan, A. Nafee, D. Halupka, Y. Allasasmeh and M. Snelgrove, Kapik Integration Toronto, Canada

A low power CT-ΔΣ is presented which achieves 92dBA of dynamic range while consuming only 110µA from a 1.1V supply in 65nm. The ADC exploits the inherent virtual ground of the ΔΣ loop to enable low power Gm-C integrators, and a simplified excess loop-delay compensation scheme. A common-mode feedback circuit which enables low voltage operation is also presented.

21-4 - 15:10
7.4µW Ultra-High Slew-Rate Pseudo Single-Stage Amplifier Driving 0.1-to-15nF Capacitive Load with >69° Phase Margin, S.-W. Hong*,** and G.-H. Cho**, *Samsung Electronics Co., Ltd. and **KAIST, Korea

To achieve ultra-high slew-rate with stable operation under wide capacitive load range, pseudo single-stage amplifier is proposed in this paper. The proposed amplifier achieves widest capacitive load drivability (x150). Also, this work achieves at least 151 times larger FOM for slew-rate compared to state-of-the-art works. This chip was fabricated using a 0.18 *µm* CMOS process with area of 0.0021 mm^2.

21-5 - 15:35
A Fully Integrated ±5A Current-Sensing System with ±0.25% Gain Error and 12µA Offset from −40°C to +85°C, S. H. Shalmany*, G. Beer**, D. Draxelmayr*** and K. Makinwa*, *Delft Univ. of Technology, The Netherlands, **Infineon Technologies, Germany and ***Infineon Technologies, Austria

This paper presents a fully integrated current-sensing system (CSS) that is 10x more accurate than the state-of-the-art. It consists of a 10mΩ on-chip shunt resistor, a ΔΣ ADC and a bandgap reference, which also senses shunt temperature. The CSS was realized in a standard 0.13µm CMOS process. It occupies 1.15mm^2 and draws 55µA from a 1.5V supply. For ±5A currents, it exhibits 12µA offset and ±0.25% gain error from −40 to +85°C. This level of accuracy is achieved with the help of multiple dynamic error correction techniques, a shunt temperature compensation scheme and chip-scale packaging for low thermal and electrical resistance.

SESSION 22

High Speed and High Frequency TX/RX [Suzaku II]

Friday, June 19, 13:55-16:00

Chairpersons: H. Ishikuro, Keio Univ.
J. Paramesh, Carnegie Mellon Univ.

22-1 - 13:55
410-GHz CMOS Imager Using a 4th Sub-Harmonic Mixer with Effective NEP of 0.3 fW/Hz$^{0.5}$ at 1-kHz Noise Bandwidth, W. Choi*, Z. Ahmad*, A. Jha*, J.-Y. Lee**, I. Kim*** and Kenneth K. O*, *Univ. of Texas at Dallas, USA, **Electronics and Telecommunications Research Institute, Korea and ***Samsung Telecommunications America, USA

A 410-GHz imager consisting of a 4th sub-harmonic mixer formed with an anti-parallel diode-connected NMOS transistor pair, and an on-chip antenna with 4.4-dB simulated gain is demonstrated in 65-nm CMOS. At –1.6-dBm power delivered to the LO input bond pad, the imager achieves 16.8-dB voltage conversion loss and 34.1-dB DSB noise figure. When the noise bandwidth is 1 kHz, sensitivity is –110 dBm, which is 30 dB better than the previously reported CMOS imagers operating near or above 300 GHz. The corresponding effective noise equivalent power is 0.3 fW/Hz$^{0.5}$.

22-2 - 14:20
A CMOS 4-Channel MIMO Baseband Receiver with 65dB Harmonic Rejection over 48MHz and 50dB Spatial Signal Separation over 3MHz at 1.3mW, C. Kim*, S. Joshi*, C. Thomas*, S. Ha*, A. Akinin*, L. Larson** and G. Cauwenberghs*, *Univ. of California, San Diego, and **Brown Univ., USA

A CMOS integrated 4-channel capacitive harmonic rejection baseband receiver and 4x4 MIMO analog core spatial filter demonstrate >65dB harmonic folding rejection over 48MHz, and >48.5dB signal separation across 3MHz baseband. The 65nm CMOS IC occupies 3.27mm^2 active area and consumes 0.67mW - 1.28mW.

22-3 - 14:45
A 60GHz Wireless Transceiver Employing Hybrid Analog/Digital Beamforming with Interference Suppression for Multiuser Gigabit/s Radio Access, K. Takinami, N. Shirakata, K. Tanaka, T. Tsukizawa, H. Motozuka, Y. Morishita, K. Miyanaga, T. Sakamoto, T. Urushihara, M. Kobayashi, H. Takahashi, M. Irie, H. Yoshikawa, A. Yoshimoto, M. Irie, M. Nakamura, T. Watanabe, H. Komori and N. Saito, Panasonic Corp., Japan

This paper presents a 60GHz hybrid analog/digital beamforming transceiver that effectively suppresses interference signals, targeting IEEE802.11ad/WiGig for dense small cell environment. A prototype has been built with low-power 40nm CMOS analog front-ends (316mW in TX and 276mW in RX without PLL) as well as offline baseband digital signal processing. Measurement shows 3dB EVM advantage over the conventional two-stream diversity during a packet collision situation.

22-4 - 15:10
A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS, I. Madadi*, M. Tohidian*, K. Cornelissens**, P. Vandenameele** and R. B. Staszewski*,***, *Delft Univ. of Technology, The Netherlands, **M4S/Hisilicon, Belgium and ***University College Dublin, Ireland

A SAW-less discrete-time superheterodyne receiver (RX) with multi-stage harmonic rejection in 28nm CMOS, featuring highly linear LNTA, employs a novel blocker-resilient octal charge-sharing band-pass filter to achieve low power consumption. The RX features NF of 2.1 to 2.6 dB, and IIP3 of 8 to 14 dBm, while drawing only 24 to 37 mW in different operating modes.

22-5 - 15:35
0.65-0.73THz Quintupler with an On-Chip Antenna in 65-nm CMOS, Z. Ahmad and Kenneth K. O., The Univ. of Texas at Dallas, USA

A passive frequency quintupler using a symmetric accumulation MOS varactor is demonstrated for the first time in CMOS. The broadband (0.65-0.73THz) quintupler with an on-chip antenna fabricated in a 65-nm bulk CMOS process reaches a setup limited peak Effective Isotropic Radiated Power (EIRP) of -22dBm at 726GHz, and a minimum conversion loss of 34dB. This highest order multiplier realized in CMOS has the highest EIRP among any lens-less silicon based signal generation circuit operating above 500GHz.

SESSION 23

Advanced Technologies for Processors [Suzaku III]

Friday, June 19, 13:55-16:00

Chairpersons: M. Hariyama, Tohoku Univ.
S. Dillen, Qualcomm Inc.

23-1 - 13:55
Broadwell : A Family of IA 14nm Processors, A. Nalamalpu, N. Kurd, A. Deval, C. Mozak, J. Douglas, A. Khanna, F. Paillet, G. Schrom, B. Phelps, Intel Corp., USA

Intel Core™ M and 5th generation of Core™ processors (code named Broadwell) are fabricated on an optimized 14 nm process technology node resulting in a 49% reduction in feature-neutral die area. 14nm created a new optimized process flavor for Core™ M to improve energy efficiency for mobile devices. Techniques and optimizations were implemented to deliver 2.5x TDP reduction coupled with up-to 60% higher graphics performance. Broadwell introduces the second generation of Fully Integrated Voltage Regulator with better droop control and parallel boot LVR along with other power-reduction features resulting in 35% reduction in active and standby power over first generation. 3DL inductor technology introduced for the first time in Broadwell, enables 30 % reduction in package thickness and improved low-load efficiency. IO re-partitioning of the SOC and a major re-design of DDR system resulted in 30% reduction in I/O power.

23-2 - 14:20
A RISC-V Vector Processor with Tightly-Integrated Switched-Capacitor DC-DC Converters in 28nm FDSOI, B. Zimmer*, Y. Lee*, A. Puggelli*, J. Kwak*, R. Jevtic*, B. Keller*, S. Bailey*, M. Blagojevic*,**, P.-F. Chiu*, H.-P. Le*, P.-H. Chen*, N. Sutardja*, R. Avizienis*, A. Waterman*, B. Richards*, P. Flatresse**, E. Alon*, K. Asanović* and B. Nikolić*, *Univ. of California, Berkeley, USA and **STMicroelectronics, France

This work demonstrates a RISC-V vector microprocessor implemented in 28nm FDSOI with fully-integrated non- interleaved switched-capacitor DCDC (SC-DCDC) converters and adaptive clocking that generates four on-chip voltages between 0.5V and 1V using only 1.0V core and 1.8V IO voltage inputs. The design pushes the capabilities of dynamic voltage scaling by enabling fast transitions (20ns), simple packaging (no off-chip passives), low area overhead (16%), high conversion efficiency (80-86%), and high energy efficiency (26.2 DP GFLOPS/W) for mobile devices.

23-3 - 14:45
A 16-Core Voltage-Stacked System with an Integrated Switched-Capacitor DC-DC Converter, S. K. Lee, T. Tong, X. Zhang, D. Brooks and G.-Y. Wei, Harvard Univ., USA

A 16-core voltage-stacked IC integrated with a switched-capacitor DC-DC converter demonstrates efficient power delivery. To overcome inter-layer voltage noise issues, the test chip implements and evaluates the benefits of self-timed clocking and clock-phase interleaving. The integrated converter offers minimum voltage guarantees and further reduces voltage noise.

23-4 - 15:10
Fully Integrated DC-DC Converter and a 0.4V 32-bit CPU with Timing-Error Prevention Supplied from a Prototype 1.55V Li-Ion Battery, M. Turnquist*, M. Hiienkari**, J. Mäkipää***, R. Jevtic****, E. Pohjalainen*, T. Kallio*and L. Koskinen**, *Aalto Univ., **Univ. of Turku, ***VTT National Research Center of Finland, Finland and ****Univ. Carlos III of Madrid, Spain

We introduce an ultra-low-energy system comprised of a prototype 1.55V Li-ion battery, fully integrated switched-capacitor (SC) DC-DC 3:1 converter, and a 32-bit RISC CPU with timing-error prevention (TEP). The DC-DC converter and CPU are manufactured in 28nm UTBB FD-SOI. The DC-DC converter uses the battery's flat discharge curve and low nominal voltage to achieve a peak efficiency of 85%. The CPU operates from 0.3V-0.5V and with energy as low as 4.9pJ/cyc. The battery, DC-DC converter, and CPU system is able to operate with an average energy of 8pJ/cyc over 95% of the battery's discharge curve in the temperature range of -20°C to 70°C.

23-5 - 15:35
Resonant Clock Mega-Mesh for the IBM z13™, D. Shan*, P. Restle**, D. Malone*, R. Groves*, E. Lai*, M. Koch***, J. Hibbeler*, Y. Kim*, C. Vezyrtzis**, J. Feder**, D. Hogenmiller* and T. Bucelot**, *IBM Systems, **IBM T. J. Watson Research Center, USA and ***IBM Systems, Germany

The IBM z13™ microprocessor utilizes a large resonant “mega-mesh” global clock distribution saving 50% of the final-stage clock mesh power and 8% of the total chip power in the desired frequency range of 4.5 to 5.5 GHz compared to a simulated, non-resonant base-line design. The mega-mesh is driven by pulsed buffers. Measurement of the mega-mesh’s robustness is enabled by skew gradients created by programmable delays. The design is implemented in IBM’s high-performance 22nm high-k CMOS SOI technology with 17 metal layers.

SESSION 24

Displays and Sensors [Suzaku I]

Friday, June 19, 16:15-17:55

Chairpersons: Y. Kato, Panasonic Corp.
N. Van Helleputte, imec

24-1 - 16:15
Hybrid Driver IC for Real-Time TFT Non-Uniformity Compensation of Ultra High-Definition AMOLED Display, J.-S. Bang*, H.-S. Kim**, S.-H. Park*, K.-D. Kim*, S.-W. Choi*, O.-J. Kwon**, C.-S. Shin**, J. Lee**, G.-H. Cho*, *KAIST and **Samsung Display, Korea

An UHD AMOLED display driver IC, enabling real-time TFT non-uniformity compensation, is presented with a hybrid driving scheme. The proposed hybrid driving scheme drives a mobile UHD (3840x1920) AMOLED panel, whose scan time is 7.7μs at a scan frequency of 60Hz, through the load of 30kohm resistance and 30pF capacitance. A proposed accurate current sensor embedded in the column driver and a back-end compensation scheme reduce maximum current error between emulated TFTs within 0.94 LSB (37nA) of 8-bit gray scales. Since the TFT variation is externally compensated, a simple 3T1C pixel circuit is employed in each pixel.

24-2 - 16:40
An AMLED Microdisplay Driver SoC with Built-In 1.25-Mb/s VLC Transmitter, L. Wu, X. Li, W. C. Chong, Z. Liu, F. Che, B. Hussain, K. M. Lau and C. P. Yue, The Hong Kong Univ. of Science and Technology, China

This paper presents the first active matrix LED (AMLED) microdisplay driver with built-in visible light communication (VLC) transmitter. The wide quarter-VGA (WQVGA) display features 400x240 pixels of 30x30 μm^2 micro-LEDs (μLED) on a single GaN IC flip-chip bonded to the proposed driver SoC. Pulse-width modulation (PWM) superimposed with on-off keying (OOK) modulation are employed for controlling the display grayscale and modulating the pixels with VLC data simultaneously. Implemented in 0.5-μm CMOS, the SoC enables a microdisplay module featuring 4-bit grayscale at 100-Hz frame rate while achieving 1.25-Mb/s lensless VLC up to 25 cm.

24-3 - 17:05
Wide Input Range 1.7µW 1.2kS/s Resistive Sensor Interface Circuit with 1 Cycle/Sample Logarithmic Sub-Ranging, M. Choi, J. Gu, D. Blaauw, D. Sylvester, Univ. of Michigan, USA

A wide input range 1.7µW, 1.2kS/s resistive sensor interface circuit fabricated in 0.18µm CMOS is presented. This circuit consumes 6.6× lower power and 31.8× less energy than previous state-of-the-art work, considering the worst-case cycle count required for correct conversion. The proposed design uses a logarithmic subrange detector based on comparator metastability to convert an input resistance ranging from 10kΩ to 10MΩ in 1 cycle per sample.

24-4 - 17:30
A Near-Field Modulation Chopping Stabilized Injection-Locked Oscillator Sensor for Protein Conformation Detection at Microwave Frequency, J.-C. Chien*, E.-C. Yeh*, L. P. Lee*, M. Anwar** and A. M. Niknejad*, *Univ. of California, Berkeley and **Univ. of California, San Francisco, USA

A near-field modulation chopping technique is implemented in an injection-locked oscillator sensor for the detection of protein conformation changes. With the addition of shielding electrodes, the signal is chopped by electronically switching the paths of the displacement sensing currents while minimizing the up-conversion of the 1/f noise. To maximize the dynamic range, feedback-around-sensor utilizing embedded varactors is applied. A 16-GHz prototype in 65-nm CMOS demonstrates the techniques lower the 1/f corner frequency from 10 to 0.25 kHz while achieving 74.5 dB of dynamic range. Bio-molecular sensing is validated with thermal-cycled bovine serum albumin (BSA) solutions at different conditions.

SESSION 25

DC-DC Converters [Suzaku II]

Friday, June 19, 16:15-17:55

Chairpersons: M. Takamiya, The Univ. of Tokyo
T. Burd, Advanced Micro Devices

25-1 - 16:15
A Fully-Integrated 40-Phase Flying-Capacitance-Dithered Switched-Capacitor Voltage Regulator with 6mV Output Ripple, S. Bang*, J.-S. Seo**, I. Lee*, S. Jeong*, N. Pinckney*, D. Blaauw*, D. Sylvester* and L. Chang***, *Univ. of Michigan, **Arizona State Univ. and ***IBM T. J. Watson Research Center, USA

A switched-capacitor voltage regulator (SCVR) that dithers flying capacitance (C_{FLY}) to reduce output ripple is presented. The proposed technique is implemented in a 40-phase SCVR with 4b C_{FLY} modulation in 65nm CMOS. At 2.3V input, on-chip ripple magnitude of 6~16mV at 1V output is measured for 11~142mA load. Peak efficiency is 70.8% at a power density of 0.187W/mm^2.

25-2 - 16:40
A 1W 8-ratio Switched-Capacitor Boost Power Converter in 140nm CMOS with 94.5% Efficiency, 0.5mm Thickness and 8.1mm^2 PCB Area, G. V. Piqué, H. J. Bergveld and R. Karadi, NXP Semiconductors, The Netherlands

This paper presents a boost switched-capacitor power converter (SCPC) in 140nm CMOS converting a wide input voltage range (2.6V to 4.2V) to an output voltage of 5V at 1W output power. It achieves the highest applicable number of conversion ratios with the lowest number of floating capacitors to date. With 8 conversion ratios and only 4 small floating capacitors, a high peak efficiency of 94.5%, a very small PCB area of 8.1mm^2, and a low thickness of 0.5mm are achieved.

25-3 - 17:05
A Battery-Connected 24-Ratio Switched Capacitor PMIC Achieving 95.5%-Efficiency, L. G. Salem and P. P. Mercier, Univ. of California, San Diego, USA

A switched-capacitor (SC) PMIC is presented that achieves up to a 6.6-bit resolution with only 5 flying capacitors for inductive PMIC replacement. The flying capacitors are reused in a frequency-scaled gear train as well as charge-feedback SC topologies to attain a 2.4× reduction in capacitors number compared to prior art. In 0.25µm bulk, the PMIC operates from an input voltage of 2.5-5V, can generate an output voltage ranging from 0.2-2V, and features an average efficiency of 90.2% across the entire range and a peak efficiency of 95.5%.

25-4 - 17:30
86.55% Peak Efficiency Envelope Modulator for 1.5W 10MHz LTE PA without AC Coupling Capacitor, S. Sung*, S.-W. Hong**, J.-S. Bang*, J.-S. Paek**, S.-C. Lee**, T. B.-H. Cho** and G.-H. Cho*, *KAIST and **Samsung Electronics Co., Ltd., Korea

For achieving boost capability and wideband with high efficiency in Envelope Modulator (EM), a newly proposed topology is introduced in this paper. The proposed EM consists of two converters: one is Low Frequency Converter (LFC) with Single Inductor Dual Output (SIDO) and the other is High Frequency Converter (HFC) with wideband capability. The two converters are combined directly in parallel without AC coupling capacitor by employing Low Frequency Current Balancing (LFCB) technique. The chip is implemented in 0.18µm CMOS process achieving 86.55% peak efficiency while tracking a 10MHz LTE envelope signal.

SESSION 26

Low-Power Wireline Transceivers [Suzaku III]

Friday, June 19, 16:15-17:55

Chairpersons: C. P. Yue, Hong Kong Univ. of Science and Technology
E. Alon, Univ. of California, Berkeley

26-1 - 16:15
A 0.5-to-0.75V, 3-to-8 Gbps/lane, 385-to-790 fJ/b, Bi-Directional, Quad-Lane Forwarded-Clock Transceiver in 22nm CMOS, R. Inti*, S. Shekhar**, G. Balamurugan*, J. Jaussi*, C. Roberts*, T.-C. Hsueh* and B. Casper*, *Intel Corp., USA and **Univ. of British Columbia, Canada

A highly digital, low-power, forwarded clock transceiver is presented. It employs source shunt terminated transmit driver and all-digital delay line based I/Q generator based clock deskew suitable for fast wakeup, low-voltage operation. A quad-lane test chip fabricated in 22nm CMOS process operates between 3-to-8 Gbps over a FR4 channel with 12dB loss and achieves BER<10^{-12} while consuming 385-to-790fJ/b.

26-2 - 16:40
A 3.8 mW/Gbps Quad-Channel 8.5-13 Gbps Serial Link with a 5-Tap DFE and a 4-Tap Transmit FFE in 28 nm CMOS, T. Ali, L. Rao, U. Singh, M. Abdul-Latif, Y. Liu, A. A. Hafez, H. Park, A. Vasani, Z. Huang, A. Iyer, B. Zhang, A. Momtaz and N. Kocaman, Broadcom Corp., USA

This paper presents a quad-lane serial link that supports virtually all data center system-side and line-side communications standards from 8.5 – 13 Gbps, implemented in 28 nm CMOS. The Tx is series source terminated with a 4-tap FFE. Its swing ranges from 33 mV to 1 Vppd. The Rx has CTLE, 5-tap DFE and CDR with 2x-oversampling, and baud-rate timing recovery options. At 13 Gbps, the link can equalize 35 dB loss at Nyquist frequency with BER of 10^{-12}. The link consumes 49 mW per lane at 13 Gbps. This is the lowest reported power in its class to date, and with comprehensive programmability for a wide range of standards.

26-3 - 17:05
A 1.2-5Gb/s 1.4-2pJ/b Serial Link in 22nm CMOS with a Direct Data-Sequencing Blind Oversampling CDR, S. Shekhar*, R. Inti**, J. Jaussi**, T.-C. Hsueh** and B. Casper**, *Univ. of British Columbia, Canada and **Intel Corp., USA

A scalable-rate serial link - comprising of a bidirectional transmitter (TX)/receiver (RX) and two all-digital PLLs (ADPLLs) - operates at 1.2-5Gb/s from 0.55-0.7V DC supply with 1.4-2pJ/b total energy efficiency, respectively. Power efficiency is improved by avoiding the use of any analog circuitry, a low swing voltage-mode transmitter, and a direct data-sequencing blind oversampling (DDS-BOS) clock and data recovery (CDR). Using DDS in feed-forward BOS-CDR obviates area and power consuming FIFOs, improves jitter tolerance (JTOL), and permits up to 7500ppm frequency tolerance (FTOL) between the TX-RX clocks − rendering it attractive for fast-locking continuous/burst operation.

26-4 - 17:30
A 2.8mW/Gb/s 14Gb/s Serial Link Transceiver in 65nm CMOS, S. Saxena, G. Shu, R. K. Nandwana, M. Talegaonkar, A. Elkholy, T. Anand, S. J. Kim, W.-S. Choi and P. K. Hanumolu, Univ. of Illinois, USA

A low power 14Gb/s transceiver using partially segmented voltage-mode driver, charge-based analog front-end, and low power clock and data recovery circuit that also minimizes clock distribution power is presented. Fabricated in a 65nm CMOS process, the transceiver achieves a power efficiency of 2.8mW/Gb/s and BER<10^{-12} while operating at 14Gb/s with 12dB channel loss.