2015 Symposia on VLSI Technology and Circuits June 14th (Sunday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	Registration (Technology and Silicon Nanoelectronics WS) *Symposia Digests will be distributed from Monday, June 15th					
8:30-18:30					8:30-18:30 2015 Silicon Nanoelectronics Workshop (Poster)	8:30-18:30 2015 Silicon Nanoelectronics Workshop (Day 1)

2015 Symposia on VLSI Technology and Circuits June 15th (Monday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-17:00	Registration (Technology and Circuits) *Press Release Timing: 7:30am JST, Monday, June 15th					
8:30-17:00	11:30-12:45 Short Course Lunch Break			8:30-17:00 Technology Short Course **More-than-Moore and More Moore for IoT**		8:30-17:30 **2015 Silicon Nanoelectronics Workshop (Day 2)**
17:00-17:30						
19:00-22:10			19:00-22:10 **2015 Spintronics Workshop on LSI**			

2015 Symposia on VLSI Technology and Circuits June 16th (Tuesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-17:00	Registration (Technology and Circuits)					
8:20-10:05				**T1 "Welcome and Plenary Session"** T1-1 8:20-8:45 ***Welcome and Opening Remarks*** T1-2 8:45-9:25 (**Plenary**) AIST Robotics for Innovation T1-3 9:25-10:05 (**Plenary**) Google System Challenges and Hardware Requirements for Future Consumer Devices: From Wearable to ChromeBooks and Devices in-between		
10:30-12:10	10:30-17:10 Circuits Short Course 2 **Analog and Digital Circuit Design for IoT Swarms**		10:30-17:10 Circuits Short Course 1 **VLSI Design for Big Data Management**	**T2: Highlight** T2-1 10:30-10:55 Intel A 14 nm SoC Platform Technology Featuring 2nd Generation Tri-Gate Transistors, 70 nm Gate Pitch, 52 nm Metal Pitch, and 0.0499 um2 SRAM Cells, Optimized for Low Power, High Performance and High Density SoC Products T2-2 10:55-11:20 Panasonic Highly Reliable TaOx ReRAM with Centralized Filament for 28-nm Embedded Application T2-3 11:20-11:45 IBM High-Mobility High-Ge-Content Si1-xGex-OI PMOS FinFETs with Fins Formed Using 3D Germanium Condensation with Ge Fraction Up to x~ 0.7, Scaled EOT~8.5Å and ~10nm Fin Width T2-4 11:45-12:10 The Univ. of Tokyo Design and Demonstration of Reliability-Aware Ge Gate Stacks with 0.5 nm EOT		
12:20-13:30		12:20-13:30 Short Course Lunch Break				
13:30-15:35		15:10-15:25 Short Course Coffee Break		**T3: (FS) 7nm Node Logic Technology and Beyond** T3-1 13:30-13:55 (**Invited**) The Univ. of Tokyo III-V and Ge/strained SOI Tunneling FET Technologies for Low Power LSIs T3-2 13:55-14:20 Intel Variation-Tolerant Dense TFET Memory with Low VMIN Matching Low-Voltage TFET Logic T3-3 14:20-14:45 (**Invited**) imec Vertical Device Architecture for 5nm and Beyond: Device & Circuit Implications T3-4 14:45-15:10 Massachusetts Institute of Technology 15-nm Channel Length MoS2 FETs with Single- and Double-Gate Structures T3-5 15:10-15:35 imec A Comparison of Arsenic and Phosphorus Extension by Room Temperature and Hot Ion Implantation for NMOS Si Bulk-FinFET at N7 (7nm) Technology Relevant Fin Dimensions	**T4: Reliability** T4-1 13:30-13:55 Liverpool John Moores Univ. AC NBTI of Ge pMOSFETs: Impact of Energy Alternating Defects on Lifetime Prediction T4-2 13:55-14:20 Liverpool John Moores Univ. A Test-Proven As-Grown-Generation (A-G) Model for Predicting NBTI under Use-Bias T4-3 14:20-14:45 The Univ. of Tokyo Impact of Random Telegraph Noise on Write Stability in Silicon-on-Thin-BOX (SOTB) SRAM Cells at Low Supply Voltage in Sub-0.4V Regime T4-4 14:45-15:10 Toshiba Further Investigations on Traps Stabilities in Random Telegraph Signal Noise and the Application to a Novel Concept Physical Unclonable Function (PUF) with Robust Reliabilities T4-5 15:10-15:35 Univ. of Minnesota High Frequency AC Electromigration Lifetime Measurements from a 32nm Test Chip
15:50-17:30				**T5: (FS) 3D Systems and Packaging** T5-1 15:50-16:15 (**Invited**) TSMC A New Integration Technology Platform: Integrated Fan-Out Wafer-Level-Packaging for Mobile Applications T5-2 16:15-16:40 (**Invited**) CEA-LETI 3DVLSI with CoolCube Process: An Alternative Path to Scaling T5-3 16:40-17:05 CEA-LETI High Performance Low Temperature Activated Devices and Optimization Guidelines for 3D VLSI Integration of FD, TriGate, FinFET on Insulator T5-4 17:05-17:30 EPFL Ultra Fine-Pitch TSV Technology for Ultra-Dense High-Q RF Inductors	**T6: Advanced CMOS Technology: Ge FinFET / Compact Model** T6-1 15:30-16:15 imec Strained Germanium Quantum Well p-FinFETs Fabricated on 45nm Fin Pitch Using Replacement Channel, Replacement Metal Gate and Germanide-Free Local Interconnect T6-2 16:15-16:40 Purdue Univ. First Experimental Demonstration of Ge 3D FinFET CMOS Circuits T6-3 16:40-17:05 imec Characterization of Self-Heating in High-Mobility Ge FinFET pMOS Devices T6-4 17:05-17:30 Univ. of California New Industry Standard FinFET Compact Model for Future Technology Nodes
17:30-18:30	**IEEE Solid-States Circuits Society Young Professionals and Grad Students Mentoring and Career coaching event**					
19:30-20:00				**19:30-20:00** **Symposium on VLSI Technology** **35th Anniversary Celebration**		
20:00-22:00		**20:00-22:00 Technology Evening Panel Discussion** **Post Scaling: What Will be Next?**		**20:00-22:00 Joint Evening Panel Discussion** **Semiconductor Industry in 2020: Evolution or Revolution?**		

Technology Short Course: June 15th (Monday) 8:30-17:00 / Shunju II, III
2015 Silicon Nanoelectronics Workshop: June 14th (Sunday) 8:30-18:30, 15th (Monday) 08:30-17:30 / Shunju I (for oral sessions), Shunju II (for posters)
2015 Spintronics Workshop on LSI: June 15th (Monday) 19:00-22:10 / Suzaku I

2015 Symposia on VLSI Technology and Circuits June 17th (Wednesday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
7:30-17:00	**Registration (Technology and Circuits)**					
8:30-10:05				**C1 "Welcome and Plenary Session"** C1-1 8:30-8:45 ***Welcome and Opening Remarks*** C1-2 8:45-9:25 (**Plenary**) Hitachi: Profiting from IoT: The Key is Very-Large-Scale Happiness Integration C1-3 9:25-10:05 (**Plenary**) Robert Bosch GmbH: Automated Driving – Impacts on the Vehicle Architecture		
10:30-12:35	**C3: SARADCs & SC Filter** C3-1 10:30-10:55 Univ. of California: A Sharp Programmable Passive Filter Based on Filtering by Aliasing C3-2 10:55-11:20 Univ. of Michigan: A 120nW 8b Sub-Ranging SAR ADC with Signal-Dependent Charge Recycling for Biomedical Applications C3-3 11:20-11:45 Intel: A 12b 70MS/s SAR ADC with Digital Startup Calibration in 14nm CMOS C3-4 11:45-12:10 Tokyo Institute of Technology: A 9.35-ENOB, 14.8 fJ/Conv.-Step Fully-Passive Noise-Shaping SAR ADC C3-5 12:10-12:35 Univ. of California: A 12-Bit 200-MS/s 3.4-mW CMOS ADC with 0.85-V Supply	**C2: Image Processing** C2-1 10:30-10:55 KAIST: A 0.5-Degree Error 10mW CMOS Image Sensor-Based Gaze Estimation Processor with Logarithmic Processing C2-2 10:55-11:20 Univ. of Michigan: A 23mW Face Recognition Accelerator in 40nm CMOS with Mostly-Read 5T Memory C2-3 11:20-11:45 Univ. of Michigan: A 640M pixel/s 3.65mW Sparse Event-Driven Neuromorphic Object Recognition Processor with On-Chip Learning C2-4 11:45-12:10 KAIST: A 33 nJ/Vector Descriptor Generation Processor for Low-Power Object Recognition C2-5 12:10-12:35 NTT Media Intelligence Laboratories: Single-Chip 4K 60fps 4:2:2 HEVC Video Encoder LSI with 8K Scalability		**JFS1: Ultra Low Power for IoT** JFS1-1 10:30-10:55 (**Invited**) Renesas Electronics: Automotive Low Power Technology for IoT Society JFS1-2 10:55-11:20 (**Invited**) imec: IoT: the Impact of Things JFS1-3 11:20-11:45 Qualcomm Technologies: Transistor-Interconnect Mobile System-On-Chip Co-Design Method for Holistic Battery Energy Minimization JFS1-4 11:45-12:10 LEAP: Sub-μW Standby Power, <18 μW/DMIPS@25MHz MCU with Embedded Atom-Switch Programmable Logic and ROM JFS1-5 12:10-12:35 (**Invited**) STMicroelectronics: Breakthrough Technologies and Reference Designs for New IoT Applications	**T7: Memory Technology: PC RAM** T7-1 10:30-10:55 Hitachi: 2.8-GB/s-Write and 670-MB/S-Erase Operations of a 3D Vertical Chain-Cell-Type Phase-Change-Memory Array T7-2 10:55-11:20 Macronix International: Greater than 2-bits/Cell MLC Storage for Ultra High Density Phase Change Memory Using a Novel Sensing Scheme T7-3 11:20-11:45 LEAP: A 50-nm 1.2-V GexTe1-x/Sb2Te3 Superlattice Topological-Switching Random-Access Memory (TRAM) T7-4 11:45-12:10 CEA-LETI: Operation Fundamentals in 12Mb Phase Change Memory Based on Innovative Ge-Rich GST Materials Featuring High Reliability Performance T7-5 12:10-12:35 Macronix International: A Novel Self-Converging Write Scheme for 2-bits/Cell Phase Change Memory for Storage Class Memory (SCM) Application
13:55-16:00	**C5: Low Power Wireless Transceivers** C5-1 13:55-14:20 imec: A 3.5mW 315/400MHz IEEE802.15.6/Proprietary Mode Digitally-Tunable Radio SoC with Integrated Digital Baseband and MAC Processor in 40nm CMOS C5-2 14:20-14:45 Univ. of California: A 1Gb/s Energy Efficient Triple-Channel UWB-Based Cognitive Radio C5-3 14:45-15:10 ARM: A 0.6V All-Digital Body-Coupled Wakeup Transceiver for IoT Applications C5-4 15:10-15:35 STMicroelectronics: A Self-Powered IPv6 Bidirectional Wireless Sensor & Actuator Network for Indoor Conditions C5-5 15:35-16:00 National Tsing Hua Univ.: A 794Mbps 135mW Iterative Detection and Decoding Receiver for 4x4 LDPC-Coded MIMO Systems in 40nm	**C4: Image Sensors** C4-1 13:55-14:20 Hokkaido Univ.: Image Sensor/Digital Logic 3D Stacked Module Featuring Inductive Coupling Channels for High Speed/Low-Noise Image Transfer C4-2 14:20-14:45 TSMC: A 0.66e-rms Temporal-Readout-Noise 3D-Stacked CMOS Image Sensor with Conditional Correlated Multiple Sampling (CCMS) Technique C4-3 14:45-15:10 National Tsing Hua Univ.: A 0.4V Self-Powered CMOS Imager with 140dB Dynamic Range and Energy Harvesting C4-4 15:10-15:35 Tohoku Univ.: A Linear Response Single Exposure CMOS Image Sensor with 0.5e- Readout Noise and 76ke- Full Well Capacity C4-5 15:35-16:00 Olympus: A 3D Stacked CMOS Image Sensor with 16Mpixel Global-Shutter Mode and 2Mpixel 10000fps Mode Using 4 Million Interconnections		**JFS2: Emerging NVM** JFS2-1 13:55-14:20 (**Invited**) Toshiba: The Progresses of MRAM as a Memory to Save Energy Consumption and Its Potential for Further Reduction JFS2-2 14:20-14:45 (**Invited**) Micron Technology: Challenges for High-Density 16Gb ReRAM with 27nm Technology JFS2-3 14:45-15:10 Renesas Electronics: Low-Power Embedded ReRAM Technology for IoT Applications JFS2-4 15:10-15:35 National Tsing Hua Univ.: RRAM-Based 7T1R Nonvolatile SRAM with 2x Reduction in Store Energy and 94x Reduction in Restore Energy for Frequent-Off Instant-On Applications JFS2-5 15:35-16:00 Chuo Univ.: Reliability Enhancement of 1Xnm TLC for Cold Flash and Millennium Memories	**T8: Process Technology: Contact / Interconnect** T8-1 13:55-14:20 STMicroelectronics: Considerations for Efficient Contact Resistivity Reduction via Fermi Level Depinning - Impact of MIS Contacts on 10nm Node nMOSFET DC Characteristics T8-2 14:20-14:45 Applied Materials: Ultra-Low Contact Resistivity with Highly Doped Si:P Contact for nMOSFET T8-3 14:45-15:10 IBM T. J. Watson Research Center: Resistivity of Copper Interconnects Beyond The 7 nm Node T8-4 15:10-15:35 Stanford Univ.: Cu Diffusion Barrier: Graphene Benchmarked to TaN for Ultimate Interconnect Scaling T8-5 15:35-16:00 KAIST: Improved Electromigration-Resistance of Cu Interconnects by Graphene-Based Capping Layer
16:10-17:55	**C7: Optical Links** C7-1 16:15-16:40 Univ. of Toronto: A 19.6-Gbps CMOS Optical Receiver with Local Feedback IIR DFE C7-2 16:40-17:05 National Taiwan Univ.: 56Gb/s PAM4 and NRZ SerDes Transceivers in 40nm CMOS C7-3 17:05-17:30 National Chiao Tung Univ.: A 25-Gb/s, -10.8-dBm Input Sensitivity, PD-Bandwidth Tolerant CMOS Optical Receiver C7-4 17:30-17:55 Univ. of California: A 45nm SOI Monolithic Photonics Chip-to-Chip Link with Bit-Statistics-Based Resonant Microring Thermal Tuning	**C6: Bio Monitoring Circuits** C6-1 16:15-16:40 Univ. of California: A 16-Channel Wireless Neural Interfacing SoC with RF-Powered Energy-Replenishing Adiabatic Stimulation C6-2 16:40-17:05 Univ. of Michigan: Enabling Closed-Loop Neural Interface: A Bi-Directional Interface Circuit with Stimulation Artifact Cancellation and Cross-Channel CM Noise Suppression C6-3 17:05-17:30 Case Western Reserve Univ.: Neurochemical Thermostat: A Neural Interface SoC with Integrated Chemometrics for Closed-Loop Regulation of Brain Dopamine C6-4 17:30-17:55 Univ. of Michigan: Toward 1024-Channel Parallel Neural Recording: Modular Δ-ΔΣ Analog Front-End Architecture with 4.84fJ/C-s•mm2 Energy-Area Product		**T9: Memory Technology: ReRAM** T9-1 16:15-16:40 Crossbar: Self-Limited RRAM with ON/OFF Resistance Ratio Amplification T9-2 16:40-17:05 A*STAR: Novel Selector for High Density Non-Volatile Memory with Ultra-Low Holding Voltage and 10^7 On/Off Ratio T9-3 17:05-17:30 imec: a-VMCO: A Novel Forming-Free, Self-Rectifying, Analog Memory Cell with Low-Current Operation, Nonfilamentary Switching and Excellent Variability T9-4 17:30-17:55 imec: A Novel CBRAM Integration Using Subtractive Dry-Etching Process of Cu Enabling High-Performance Memory Scaling Down to 10nm Node	**T10: Advanced CMOS Technology: Nanowire FET / 2D Materials** T10-1 16:15-16:40 imec: Gate-All-Around NWFETs vs. Triple-Gate FinFETs: Junctionless vs. Extensionless and Conventional Junction Devices with Controlled EWF Modulation for Multi-VT CMOS T10-2 16:40-17:05 IBM T. J. Watson Research Center: Si Nanowire CMOS Fabricated with Minimal Deviation from RMG FinFET Technology Showing Record Performance T10-3 17:05-17:30 imec: Si-cap-free SiGe p-Channel FinFETs and Gate-All-Around Transistors in a Replacement Metal Gate Process: Interface Trap Density Reduction and Performance Improvement by High-Pressure Deuterium Anneal T10-4 17:30-17:55 Massachusetts Institute of Technology: MoS2 FET Fabrication and Modeling for Large-Scale Flexible Electronics
19:00-21:00				**19:00-21:00** **Joint Banquet**		

2015 Symposia on VLSI Technology and Circuits June 18th (Thursday)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I
8:00-17:00	Registration (Technology and Circuits)					
8:30-10:10	**C9: Phase and Delay Locked Loops**	**C8: (FS) Systems for Big Data Management**		**T11: Advanced CMOS Technology: Si FinFET Device & Process**		**T12: Memory Technology: MTJ and Related Devices**
	C9-1 8:30-8:55	C8-1 8:30-8:55 (**Invited**)		T11-1 8:30-8:55		T12-1 8:30-8:55
	Seoul National Univ. — An All-Digital Bang-Bang PLL Using Two-Point Modulation and Background Gain Calibration for Spread Spectrum Clock Generation	NEC — FPGA-Accelerated Complex Event Processing		imec — RMG nMOS 1st Process Enabling 10x Lower Gate Resistivity in N7 Bulk FinFETs		Tohoku Univ. — Novel Oxygen Showering Process (OSP) for Extreme Damage Suppression of Sub-20nm High Density p-MTJ Array without IBE Treatment
	C9-2 8:55-9:20	C8-2 8:55-9:20		T11-2 8:55-9:20		T12-2 8:55-9:20
	National Taiwan Univ. — A Digital Bang-Bang Phase-Locked Loop with Automatic Loop Gain Control and Loop Latency Reduction	Keio Univ. — Inductively-Powered Wireless Solid-State Drive (SSD) System with Merged Error Correction of High-Speed Non-Contact Data Links and NAND Flash Memory		Intel — High Sigma Measurement of Random Threshold Voltage Variation in 14nm Logic FinFET Technology		Tohoku Univ. — 10 nmφ Perpendicular-Anisotropy CoFeB-MgO Magnetic Tunnel Junction with Over 400°C High Thermal Tolerance by Boron Diffusion Control
	C9-3 9:20-9:45	C8-3 9:20-9:45		T11-3 9:20-9:45		T12-3 9:20-9:45
	Univ. of Minnesota — A 0.4-1.6GHz Spur-Free Bang-Bang Digital PLL in 65nm with a D-Flip-Flop Based Frequency Subtractor Circuit	Chuo Univ. — Privacy-Protection Solid-State Storage (PP-SSS) System: Automatic Lifetime Management of Internet-Data's Right to be Forgotten		TSMC — High Voltage I/O FinFET Device Optimization for 16nm System-on-a-Chip (SoC) Technology		Univ. of Minnesota — An 8-bit Analog-to-Digital Converter Based on the Voltage-Dependent Switching Probability of a Magnetic Tunnel Junction
	C9-4 9:45-10:10	C8-4 9:45-10:10 (**Invited**)		T11-4 9:45-10:10		T12-4 9:45-10:10
	UNIST — A 450-fs Jitter PVT-Robust Fractional-Resolution Injection-Locked Clock Multiplier Using a DLL-Based Calibrator with Replica-Delay-Cells	Toshiba — Caching Mechanisms towards Single-Level Storage Systems for Internet of Things		IBM Research — A Novel ALD SiBCN Low-k Spacer for Parasitic Capacitance Reduction in FinFETs		TDK-Headway Technologies — Demonstration of an MgO Based Anti-Fuse OTP Design Integrated With a Fully Functional STT-MRAM at the Mbit Level
10:30-12:35	**C11: Nyquist ADC and DAC**	**C10 (FS): IoT and Smart Systems**		**T13: Advanced CMOS Technology: X-On Insulator (X-OI) Devices**		**T14: Memory Technology: 3D NAND Flash & Other NVM**
	C11-1 10:30-10:55	C10-1 10:30-10:55 (**Invited**)		T13-1 10:30-10:55		T14-1 10:30-10:55
	Texas A&M Univ. — A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS	Hitachi — Embedded Image Recognition Systems for Advanced Safety Vehicles		STMicroelectronics — 14nm FDSOI Upgraded Device Performance for Ultra-Low Voltage Operation		Macronix International — A Novel Dichotomic Programming Algorithm Applied to 3D NAND Flash
	C11-2 10:55-11:20	C10-2 10:55-11:20		T13-2 10:55-11:20		T14-2 10:55-11:20
	Columbia Univ. — A 3-10fJ/Conv-Step 0.0032mm2 Error-Shaping Alias-Free Asynchronous ADC	Panasonic — High-Level Video Analytics PC Subsystem Using SoC with Heterogeneous Multi-Core Architecture		LEAP — Novel Single p+Poly-Si/Hf/SiON Gate Stack Technology on Silicon-on-Thin-Buried-Oxide (SOTB) for Ultra-Low Leakage Applications		Seoul National Univ. — Comprehensive Analysis of Retention Characteristics in 3-D NAND Flash Memory Cells with Tube-Type Poly-Si Channel Structure
	C11-3 11:20-11:45	C10-3 11:20-11:45		T13-3 11:20-11:45		T14-3 11:20-11:45
	Univ. of California — A 6b 46GS/s ADC with >23GHz BW and Sparkle-Code Error Correction	Univ. of California — A Throughput-Agnostic 11.9-13.6GOPS/mW Multi-Signal Classification SoC for Cognitive Radios in 40nm CMOS		IBM Research — Confined Epitaxial Lateral Overgrowth (CELO): A Novel Concept for Scalable Integration of CMOS-Compatible InGaAs-on-Insulator MOSFETs on Large-Area Si Substrates		National Chiao Tung Univ. — Low Power 1T DRAM/NVM Versatile Memory Featuring Steep Sub-60-mV/decade Operation, Fast 20-ns Speed, and Robust 85oC-Extrapolated 1016 Endurance
	C11-4 11:45-12:10	C10-4 11:45-12:10		T13-4 11:45-12:10		T14-4 11:45-12:10
	Qualcomm Technologies — A 14b 750MS/s DAC in 20nm CMOS with <-168dBm/Hz Noise Floor beyond Nyquist and 79dBc SFDR Utilizing a Low Glitch-Noise Hybrid R-2R Architecture	Harvard Univ. — A Multi-Chip System Optimized for Insect-Scale Flapping-Wing Robots		The Univ. of Tokyo — High Hole Mobility Front-Gate InAs/InGaSb-OI Single Structure CMOS on Si		Carnegie Mellon Univ. — High Performance, Integrated 1T1R Oxide-Based Oscillator: Stack Engineering for Low-Power Operation in Neural Network Applications
	C11-5 12:10-12:35	C10-5 12:10-12:35 (**Invited**)		T13-5 12:10-12:35		T14-5 12:10-12:35
	Analog Devices — A 16-bit 10Gsps Current Steering RF DAC in 65nm CMOS Achieving 65dBc ACLR Multi-Carrier Performance at 4.5GHz Fout	NXP Semiconductors — Sensor-Hub Sweet-Spot Analysis for Ultra-Low-Power Always-on Operation		IBM Research — An InGaAs on Si Platform for CMOS with 200 mm InGaAs-OI Substrate, Gate-first, Replacement Gate Planar and FinFETs Down to 120 nm Contact Pitch		imec — Quantitative Endurance Failure Model for Filamentary RRAM
12:45-14:05			**12:45-14:05 Luncheon Talk** DASSAI: Innovating Sake Brewing with Massive Usage of Data and IT			
14:20-16:00	**C12: DRAM**	**JFS3: Advanced Technology and Circuits for IoT**		**T15: Non-Si Substrates: III-V HEMT/FET/TFET**		**T16: Beyond CMOS and New Concepts**
	C12-1 14:20-14:45	JFS3-1 14:20-14:45 (**Invited**)		T15-1 14:20-14:45		T16-1 14:20-14:45
	EPFL — A 4×9 Gb/s 1 pJ/b NRZ/Multi-Tone Serial-Data Transceiver with Crosstalk Reduction Architecture for Multi-Drop Memory Interfaces in 40nm CMOS	imec — Technology Innovation in an IoT Era		Intel — High-Performance Low-Leakage Enhancement-Mode High-K Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF Power Amplifiers for Low-Power Mobile SoCs		The Univ. of Tokyo — Device Design Guideline for Steep Slope Ferroelectric FET Using Negative Capacitance in Sub-0.2V Operation: Operation Speed, Material Requirement and Energy Efficiency
	C12-2 14:45-15:10	JFS3-2 14:45-15:10		T15-2 14:45-15:10		T16-2 14:45-15:10
	Samsung Electronics — A 6.4Gb/s/pin at Sub-1V Supply Voltage TX-Interleaving Technique for Mobile DRAM Interface	Tohoku Univ. — Fabrication of a 3000-6-Input-LUTs Embedded and Block-Level Power-Gated Nonvolatile FPGA Chip Using p-MTJ-Based Logic-in-Memory Structure		TSMC — In0.53Ga0.47As MOSFETs with High Channel Mobility and Gate Stack Quality Fabricated on 300 mm Si Substrate		Toshiba — Silicon-Compatible Low Resistance S/D Technologies for High-Performance Top-Gate Self-Aligned InGaZnO TFTs with UTBB (Ultra-Thin Body and BOX) Structures
	C12-3 15:10-15:35	JFS3-3 15:10-15:35		T15-3 15:10-15:35		T16-3 15:10-15:35
	SK hynix — A 4.35Gb/s/pin LPDDR4 I/O Interface with Multi-VOH Level, Equalization Scheme, and Duty-Training Circuit for Mobile Applications	Intel — Low-Voltage Metal-Fuse Technology Featuring a 1.6V-Programmable 1T1R Bit Cell with an Integrated 1V Charge Pump in 22nm Tri-gate Process		The Pennsylvania State Univ. — Demonstration of p-type In0.7Ga0.3As/GaAs0.35Sb0.65 and n-type GaAs0.4Sb0.6/In0.65Ga0.35As Complimentary Heterojunction Vertical Tunnel FETs for Ultra-Low Power Logic		Semiconductor Energy Laboratory — 30-nm-Channel-Length C-Axis Aligned Crystalline In–Ga–Zn–O Transistors with Low Off-State Leakage Current and Steep Subthreshold Characteristics
	C12-4 15:35-16:00	JFS3-4 15:35-16:00		T15-4 15:35-16:00		T16-4 15:35-16:00
	ITRI — A Computer Designed Half Gb 16-Channel 819Gb/s High-Bandwidth and 10ns Low-Latency DRAM for 3D Stacked Memory Devices Using TSVs	Qualcomm Technologies — Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC		The Pennsylvania State Univ. — Indium Arsenide (InAs) Single and Dual Quantum-Well Heterostructure FinFETs		EPFL — Energy Efficient 1-Transistor Active Pixel Sensor (APS) with FD SOI Tunnel FET
16:15-17:55	**C14: Application-Specific IOs**	**JFS4: 3D and Heterogeneous Integration**	**C13: Sensors & Bio Imaging**			
	C14-1 16:15-16:40	JFS4-1 16:15-16:40	C13-1 16:15-16:40			
	Texas Instruments — An Efficient and Resilient Ultra-High Speed Galvanic Data Isolator Leveraging Broad-Band Multi Resonant Tank Electro-Magnetic Coupling	imec — Active-Lite Interposer for 2.5 & 3D Integration	Univ. of Illinois — A Self-Referenced VCO-Based Temperature Sensor with 0.034oC/mV Supply Sensitivity in 65nm CMOS			
	C14-2 16:40-17:05	JFS4-2 16:40-17:05	C13-2 16:40-17:05			
	KAIST — A 100-GbE Reverse Gearbox IC in 40nm CMOS for Supporting Legacy 10- and 40-GbE Standards	Columbia Univ. — An 82%-Efficient Multiphase Voltage-Regulator 3D Interposer with On-Chip Magnetic Inductors	Univ. of Michigan — A 10.6mm3 Fully-Integrated, Wireless Sensor Node with 8GHz UWB Transmitter			
	C14-3 17:05-17:30	JFS4-3 17:05-17:30	C13-3 17:05-17:30			
	Broadcom — A 2.7mW/Channel 48-to-1000MHz Direct Sampling Full-Band Cable Receiver	Technische Universität Dresden — 15 dB Conversion Gain, 20 MHz Carrier Frequency AM Receiver in Flexible a-IGZO TFT Technology with Textile Antennas	KAIST — A 4.84mW 30fps Dual Frequency Division Multiplexing Electrical Impedance Tomography SoC for Lung Ventilation Monitoring System			
	C14-4 17:30-17:55	JFS4-4 17:30-17:55	C13-4 17:30-17:55			
	The Hong Kong Univ. of Sci. &Tech. — A Fully Integrated IEEE 802.15.7 Visible Light Communication Transmitter with On-Chip 8-W 85% Efficiency Boost LED Driver	Princeton Univ. — Reconstruction of Multiple-User Voice Commands Using a Hybrid System Based on Thin-Film Electronics and CMOS	Princeton Univ. — A Fully Integrated CMOS Fluorescence Biosensor with On-Chip Nanophotonic Filter			
20:00-22:00	**20:00-22:00 Circuits Evening Panel Discussion 2** **Wearable Electronics: Still an Oasis or Just a Mirage for the Semiconductor Industry?**		**Circuits Evening Panel Discussion 1** **Is University Circuit Design Research and Education Keeping Up with Industry Needs?**			

2015 Symposia on VLSI Technology and Circuits June 19th (Friday)

Time	Suzaku III		Suzaku II		Suzaku I		Shunju III	Shunju II	Shunju I
8:00-15:00	Registration (Circuits only)								
8:30-10:10	**C17: Low-Power and Secure Design**		**C16: Oscillators**		**C15: Ultra-High Speed Receivers**				
	C17-1	8:30-8:55	C16-1	8:30-8:55	C15-1	8:30-8:55			
	Univ. of California	A Low-PDP and Low-Area Repeater Using Passive CTLE for On-Chip Interconnects	The Hong Kong Univ. of Sci. &Tech.	A Dithering-Less 54.79-to-63.16GHz DCO with 4-Hz Frequency Resolution Using an Exponentially-Scaling C-2C Switched-Capacitor Ladder	Texas A&M Univ.	A 32 Gb/s 0.55 mW/Gbps PAM4 1-FIR 2-IIR Tap DFE Receiver in 65-nm CMOS			
	C17-2	8:55-9:20	C16-2	8:55-9:20	C15-2	8:55-9:20			
	Univ. of Michigan	1.32GHz High-Throughput Charge-Recovery AES Core with Resistance to DPA Attacks	National Taiwan Univ.	A -194 dBc/Hz FOM Interactive Current-Reused QVCO (ICR-QVCO) with Capacitor-Coupling Self-Switching Sinusoidal Current Biasing (CSSCB) Phase Noise Reduction Technique	Univ. of California	A 40-Gb/s 9.2-mW CMOS Equalizer			
	C17-3	9:20-9:45	C16-3	9:20-9:45	C15-3	9:20-9:45			
	Univ. of Michigan	A Robust -40 to 120°C All-Digital True Random Number Generator in 40nm CMOS	Univ. of Michigan	A 99nW 70.4kHz Resistive Frequency Locking On-Chip Oscillator with 27.4ppm/ºC Temperature Stability	IBM Research	A 5.9mW/Gb/s 7Gb/s/pin 8-Lane Single-Ended RX with Crosstalk Cancellation Scheme Using a XCTLE and 56-Tap XDFE in 32nm SOI CMOS			
	C17-4	9:45-10:10	C16-4	9:45-10:10	C15-4	9:45-10:10			
	Columbia Univ.	A 3.07µm2/Bitcell Physically Unclonable Function with 3.5% and 1% Bit-Instability across 0 to 80°C and 0.6 to 1.2V in a 65nm CMOS	Massachusetts Institute of Tech.	4.2 pW Timer for Heavily Duty-Cycled Systems	Univ. of California	A 60Gb/s 173mW Receiver Frontend in 65nm CMOS Technology			
10:30-12:35	**C20: Power Management Circuits**		**C19: SRAM and CAM**		**C18: Wideband Over-Sampled ADCs**				
	C20-1	10:30-10:55	C19-1	10:30-10:55	C18-1	10:30-10:55			
	Univ. of California	A 0.78mW/cm2 Autonomous Thermoelectric Energy-Harvester for Biomedical Sensors	Intel	A 0.094um2 High Density and Aging Resilient 8T SRAM with 14nm FinFET Technology Featuring 560mV VMIN with Read and Write Assist	Texas A&M Univ.	A 75 MHz BW 68dB DR CT-ΣΔ Modulator with Single Amplifier Biquad Filter and a Broadband Low-Power Common-Gate Summing Technique			
	C20-2	10:55-11:20	C19-2	10:55-11:20	C18-2	10:55-11:20			
	Massachusetts Institute of Tech.	Solar Energy Harvesting System with Integrated Battery Management and Startup Using Single Inductor and 3.2nW Quiescent Power	IBM Research	14nm FinFET Based Supply Voltage Boosting Techniques for Extreme Low Vmin Operation	Oregon State Univ.	A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-Based CT ΔΣ ADC Using Dual Phase/Frequency Feedback in 65nm CMOS			
	C20-3	11:20-11:45	C19-3	11:20-11:45	C18-3	11:20-11:45			
	Seoul National Univ.	A 2.5-V, 160-µJ-Output Piezoelectric Energy Harvester and Power Management IC for Batteryless Wireless Switch (BWS) Applications	Univ. of Michigan	A Reconfigurable Sense Amplifier with 3X Offset Reduction in 28nm FDSOI CMOS	Univ. of Florida	A 7.2 mW 75.3 dB SNDR 10 MHz BW CT Delta-Sigma Modulator Using Gm-C-Based Noise-Shaped Quantizer and Digital Integrator			
	C20-4	11:45-12:10	C19-4	11:45-12:10	C18-4	11:45-12:10			
	Univ. of California	A 144MHz Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation	Univ. of Michigan	A Configurable TCAM / BCAM / SRAM Using 28nm Push-Rule 6T Bit Cell	MediaTek	A 16nm FinFet 19/39MHz 78/72dB DR Noise-Injected Aggregated CTSDM ADC for Configurable LTE Advanced CCA/NCCA Application			
	C20-5	12:10-12:35	C19-5	12:10-12:35	C18-5	12:10-12:35			
	The Hong Kong Univ. of Sci. &Tech.	A 5.5W AC Input Converter-Free LED Driver with 82% Low-Frequency-Flicker Reduction, 88.2% Efficiency and 0.92 Power Factor	Renesas Electronics	1.8 Mbit/mm2 Ternary-CAM Macro with 484 ps Search Access Time in 16 nm Fin-FET Bulk CMOS Technology	Broadcom	A 10/20/30/40 MHz Feed-Forward FIR DAC Continuous-Time ΔΣ ADC with Robust Blocker Performance for Radio Receivers			
13:55-16:00	**C23: Advanced Technologies for Processors**		**C22: High Speed and High Frequency TX/RX**		**C21: Delta-Sigma Modulators and Analog Techniques**				
	C23-1	13:55-14:20	C22-1	13:55-14:20	C21-1	13:55-14:20			
	Intel	Broadwell : A Family of IA 14nm Processors	Univ. of Texas at Dallas	410-GHz CMOS Imager Using a 4th Sub-Harmonic Mixer with Effective NEP of 0.3 fW/Hz0.5 at 1-kHz Noise Bandwidth	Universidade Nova de Lisboa	A 0.7 V 256 µW ΔΣ Modulator with Passive RC Integrators Achieving 76 dB DR in 2 MHz BW			
	C23-2	14:20-14:45	C22-2	14:20-14:45	C21-2	14:20-14:45			
	Univ. of California	A RISC-V Vector Processor with Tightly-Integrated Switched-Capacitor DC-DC Converters in 28nm FDSOI	Univ. of California	A CMOS 4-Channel MIMO Baseband Receiver with 65dB Harmonic Rejection over 48MHz and 50dB Spatial Signal Separation over 3MHz at 1.3mW	Broadcom	A 13-ENOB, 5 MHz BW, 3.16 mW Multi-Bit Continuous-Time ΔΣ ADC in 28 nm CMOS with Excess-Loop-Delay Compensation Embedded in SAR Quantizer			
	C23-3	14:45-15:10	C22-3	14:45-15:10	C21-3	14:45-15:10			
	Harvard Univ.	A 16-Core Voltage-Stacked System with an Integrated Switched-Capacitor DC-DC Converter	Panasonic	A 60GHz Wireless Transceiver Employing Hybrid Analog/Digital Beamforming with Interference Suppression for Multiuser Gigabit/s Radio Access	Kapik Integration Toronto	A Low-Power Gm-C-Based CT-ΔΣ Audio-Band ADC in 1.1V 65nm CMOS			
	C23-4	15:10-15:35	C22-4	15:10-15:35	C21-4	15:10-15:35			
	Aalto Univ.	Fully Integrated DC-DC Converter and a 0.4V 32-bit CPU with Timing-Error Prevention Supplied from a Prototype 1.55V Li-Ion Battery	Delft Univ. of Technology	A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS	Samsung Electronics	7.4µW Ultra-High Slew-Rate Pseudo Single-Stage Amplifier Driving 0.1-to-15nF Capacitive Load with >69° Phase Margin			
	C23-5	15:35-16:00	C22-5	15:35-16:00	C21-5	15:35-16:00			
	IBM Systems	Resonant Clock Mega-Mesh for the IBM z13TM	The Univ. of Texas at Dallas	0.65-0.73THz Quintupler with an On-Chip Antenna in 65-nm CMOS	Delft Univ. of Technology	A Fully Integrated ±5A Current-Sensing System with ±0.25% Gain Error and 12µA Offset from −40° C to +85°C			
16:15-17:55	**C26: Low-Power Wireline Transceivers**		**C25: DC-DC Converters**		**C24: Displays and Sensors**				
	C26-1	16:15-16:40	C25-1	16:15-16:40	C24-1	16:15-16:40			
	Intel	A 0.5-to-0.75V, 3-to-8 Gbps/lane, 385-to-790 fJ/b, Bi-Directional, Quad-Lane Forwarded-Clock Transceiver in 22nm CMOS	Univ. of Michigan	A Fully-Integrated 40-Phase Flying-Capacitance-Dithered Switched-Capacitor Voltage Regulator with 6mV Output Ripple	KAIST	Hybrid Driver IC for Real-Time TFT Non-Uniformity Compensation of Ultra High-Definition AMOLED Display			
	C26-2	16:40-17:05	C25-2	16:40-17:05	C24-2	16:40-17:05			
	Broadcom	A 3.8 mW/Gbps Quad-Channel 8.5-13 Gbps Serial Link with a 5-Tap DFE and a 4-Tap Transmit FFE in 28 nm CMOS	NXP Semiconductors	A 1W 8-ratio Switched-Capacitor Boost Power Converter in 140nm CMOS with 94.5% Efficiency, 0.5mm Thickness and 8.1mm2 PCB Area	The Hong Kong Univ. of Sci. &Tech.	An AMLED Microdisplay Driver SoC with Built-In 1.25-Mb/s VLC Transmitter			
	C26-3	17:05-17:30	C25-3	17:05-17:30	C24-3	17:05-17:30			
	Univ. of British Columbia	A 1.2-5Gb/s 1.4-2pJ/b Serial Link in 22nm CMOS with a Direct Data-Sequencing Blind Oversampling CDR	Univ. of California	A Battery-Connected 24-Ratio Switched Capacitor PMIC Achieving 95.5%-Efficiency	Univ. of Michigan	Wide Input Range 1.7µW 1.2kS/s Resistive Sensor Interface Circuit with 1 Cycle/Sample Logarithmic Sub-Ranging			
	C26-4	17:30-17:55	C25-4	17:30-17:55	C24-4	17:30-17:55			
	Univ. of Illinois	A 2.8mW/Gb/s 14Gb/s Serial Link Transceiver in 65nm CMOS	KAIST	86.55% Peak Efficiency Envelope Modulator for 1.5W 10MHz LTE PA without AC Coupling Capacitor	Univ. of California	A Near-Field Modulation Chopping Stabilized Injection-Locked Oscillator Sensor for Protein Conformation Detection at Microwave Frequency			