2017 Symposium on VLSI Circuits Short Course 1

Machine Learning for Circuit Designers [Suzaku I]

Monday, June 5, 8:30-16:20

Organizers / Chairs: M. Yamaoka, Hitachi, Ltd.
V. Sze, Massachusetts Institute of Technology

8:30 **Brief Outline,** Short Course Chair

8:35 **Machine Learning Basics and Its Applications to Internet-of-Things,** H. Maruyama, Preferred Networks

9:25 **Machine-Learning-Enabled Design Space for Energy-Efficient Mixed-Signal Inference Systems,**
N. Verma, Princeton Univ.

10:15 **Break**

10:35 **Designing Efficient Deep Learning Accelerators: Challenges and Opportunities,**
J. Emer, Massachusetts Institute of Technology / nVidia

11:25 **Advanced Techniques for High-Speed Deep Learning on Large-Scale Neural Network in the Cloud,**
Y. Tomita, Fujitsu Laboratories Ltd.

12:15 **Lunch**

13:30 **Deep Learning for Mobile and Embedded Devices,** M. Aleksic, Qualcomm Inc.

14:20 **Vision-Centric Devices at the Network Edge Using Deep-Networks and Computer Vision,**
D. Moloney, Intel Corp. / Movidius

15:10 **Break**

15:30 **Mobile/Embedded DNN and AI SoCs,** H.-J. Yoo, KAIST

2017 Symposium on VLSI Circuits Short Course 2

Integrated Circuits for Smart Connected Cars and Automated Driving [Suzaku II]

Monday, June 5, 8:30-16:20

Organizers / Chairs: K. Kanda, Fujitsu Laboratories Ltd.
J. Wuu, AMD

8:30 **Brief Outline,** Short Course Chair

8:35 **An Overview of Automotive Electronics,** C. Lang, Bosch USA

9:25 **Intra-Vehicle Wireline Networks,** A. Klaus, Marvell Semiconductor

10:15 **Break**

10:35 **Image Sensors for Automotive Applications,** S. Kawahito, Shizuoka Univ.

11:25 **LIDAR System Design for Automotive Applications,** E. Bartolome, Texas Instruments

12:15 **Lunch**

13:30 **Automotive Sensors and Interfaces,** B. Clark, Analog Devices, Inc.

14:20 **Key Technologies That Support EV Motor Control,** S. Otani, Renesas Electronics Corp.

15:10 **Break**

15:30 **Autonomous Vehicles Platform: Processor/Software Architecture, Machine Learning and Security,**
J. Weast, Intel Corp.

Demo Session & Reception [Suzaku I, II, III]

Monday, June 5, 17:30-19:30

Organizers / Chairs: Y. Oike, Sony Semiconductor Solutions Corp.
N. Sugii, Hitachi, Ltd.
R. Navid, Intel Corp.

Newly Established Venue for in-depth Discussion with Authors:
- Demonstration of chip operation highlighting key results
- Systems showcasing potential applications for circuit-level innovations
- Table-top real-time demonstration of new device characterization
- Visual illustration of technological concepts and analyses

C1-2
Innovative Solutions toward Future Society with AI, Robotics, and IoT, T. Yukitake, Panasonic Corp., Japan

C2-3
A Heterogeneous Microprocessor for Energy-Scalable Sensor Inference Using Genetic Programming, H. Jia, J. Lu, N. K. Jha and N. Verma, Princeton Univ., USA

C2-4
A 3.43TOPS/W 48.9pJ/Pixel 50.1nJ/Classification 512 Analog Neuron Sparse Coding Neural Network with On-Chip Learning and Classification in 40nm CMOS, F. N. Buhler*, P. Brown*, J. Li*.**, T. Chen*, Z. Zhang* and M. P. Flynn*, *Univ. of Michigan and **Intel Corp., USA

C4-1
A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-Directional Data Telemetry for Real-Time Human Epileptic Seizure Control, C.-H. Cheng, P.-Y. Tsai, T.-Y. Yang, W.-H. Cheng, T.-Y. Yen, Z. Luo, X.-H. Qian, Z.-X. Chen, T.-H. Lin, W.-H. Chen, W.-M. Chen, S.-F. Liang, F.-Z. Shaw, C.-S. Chang, F.-Y. Shih, Y.-L. Hsin, C.-Y. Lee, M.-D. Ker and C.-Y. Wu, National Chiao Tung Univ., Taiwan

C4-2
A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing, X.-H. Qian*, Y.-C. Wu**, T.-Y. Yang*, C.-H. Cheng*, H.-C. Chu*, W.-H. Cheng*, T.-Y. Yen*, T.-H. Lin*, Y.-J. Lin*, Y.-C. Lee*, J.-H. Chang*, S.-T. Lin*, S.-H. Li**, T.-C. Wu*, C.-C. Huang**, C.-F. Lee***, C.-H. Yang**, C.-C. Hung*, T.-S. Chi*, C.-H. Liu**, M.-D. Ker* and C.-Y. Wu*, *National Chiao Tung Univ., **National Taiwan Univ. and ***Hualien Tzu Chi Medical Center, Taiwan

JFS2-1
A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Solenoid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS, H. K. Krishnamurthy, S. Weng, G. E. Matthew, R. Saraswat, K. Ravichandran, J. Tschanz and V. De, Intel Corp., USA

JFS2-2
A 6Gb/s Rotatable Non-Contact Connector with High-Speed/I²C/CAN/SPI Interface Bridge IC, M. Haraguchi*, A. Kosuge*, T. Igarashi**, S. Masaki**, M. Sueda**, M. Hamada* and T. Kuroda*, *Keio Univ. and **Socionext Inc., Japan

JFS2-4
A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications, S. Park*, T. Cho*, M. Kim*, H. Park** and K. Lee*, *KAIST and **Seoul National Univ. of Science and Technology, Korea

C17-3
A Single-Chip 2048×1080 Resolution 32fps 380mW Trinocular Disparity Estimation Processor in 28nm CMOS Technology, J. Narinx, T. Demirci, A. Akin and Y. Leblebici, EPFL, Switzerland

C19-1
A 4.1Mpix 280fps Stacked CMOS Image Sensor with Array-Parallel ADC Architecture for Region Control, T. Takahashi*, Y. Kaji**, Y. Tsukuda*, S. Futami*, K. Hanzawa***, T. Yamauchi*, P. W. Wong***, F. Brady***, P. Holden***, T. Ayers***, K. Mizuta*, S. Ohki*, K. Tatani*, T. Nagano*, H. Wakabayashi*** and Y. Nitta*, *Sony Semiconductor Solutions Corp., **Sony LSI Design Inc., Japan and ***Sony Electronics Inc., USA

C22-1
320x240 Back-Illuminated 10μm CAPD Pixels for High Speed Modulation Time-of-Flight CMOS Image Sensor, Y. Kato*, T. Sano*, Y. Moriyama*, S. Maeda*, T. Yamazaki*, A. Nose*, K. Shina*, Y. Yasu*, W. van der Tempel**, A. Ercan** and Y. Ebiko*, *Sony Semiconductor Solutions Corp., Japan and **SoftKinetic, Belgium

C24-3
A 6×5×4mm³ General Purpose Audio Sensor Node with a 4.7μW Audio Processing IC, M. Cho*, S. Oh*, S. Jeong*, Y. Zhang*, I. Lee*, Y. Kim*, L.-X. Chuo*, D. Kim*, Q. Dong*, Y.-P. Chen*, M. Lim**, M. Daneman**, D. Blaauw*, D. Sylvester* and H.-S. Kim*, *Univ. of Michigan and **Invensense, USA

C26-4
A 130nm FeRAM-Based Parallel Recovery Nonvolatile SOC for Normally-OFF Operations with 3.9× Faster Running Speed and 11× Higher Energy Efficiency Using Fast Power-On Detection and Nonvolatile Radio Controller, Z. Wang*, F. Su*, Y. Wang*, Z. Li*, X. Li*, R. Yoshimura**, T. Naiki**, T. Tsuwa**, T. Saito**, Z. Wang**, K. Taniuchi**, M.-F. Chang***, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **Rohm Co., Ltd., Japan and ***National Tsing Hua Univ., Taiwan

T8-1
Towards A Fully Integrated, Wirelessly Powered, and Ordinarily Equipped On-Lens System for Successive Dry Eye Syndrome Diagnosis, J.-C. Chiou, S.-H. Hsu, Y.-C. Huang, G.-T. Yeh, K.-S. Dai and C.-K. Kuei, National Chiao Tung Univ., Taiwan

T10-4
Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal-Aware Lifetime Prediction Methodology, H. Jiang*,**, L. Shen*, S. H. Shin**, N. Xu***, G. Du*, B.-Y. Nguyen****, O. Faynot*****, M. A. Alam**, X. Zhang* and X. Y. Liu*, *Peking Univ., China, **Purdue Univ., ***Univ. of California, Berkeley, ****Soitec, USA and *****CEA-LETI, France

JFS3-3
Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application, S. H. Wu*, X. Y. Jia*, X. Li*, C. C. Shuai*, H. C. Lin*, M. C. Lu*, T. H. Wu*, M. Y. Liu*, J. Y. Wu*, D. Matsubayashi**, K. Kato** and S. Yamazaki**, *United Microelectronics Corporation, Singapore and **Semiconductor Energy Laboratory Co., Ltd., Japan

T14-1
First Experimental Observation of Channel Thickness Scaling (Down to 3 nm) Induced Mobility Enhancement in UTB GeOI _n_MOSFETs, W. H. Chang, T. Irisawa, H. Ishii, H. Hattori, H. Ota, H. Takagi, Y. Kurashima, N. Uchida and T. Maeda, AIST, Japan

T15-3
Flash Reliability Boost Huffman Coding (FRBH): Co-Optimization of Data Compression and V_{TH} Distribution Modulation to Enhance Data-Retention Time by Over 2900x, Y. Deguchi, A. Kobayashi, H. Watanabe and K. Takeuchi, Chuo Univ., Japan

Technology SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Tuesday, June 6, 8:00-10:10

Chairpersons: M. Masahara, AIST
                 C.-P. Chang, Applied Materials

T1-1 - 8:00
Welcome and Opening Remarks
S. Inaba, Toshiba Memory Corp.
M. Khare, IBM

T1-2 - 8:45 (Plenary)
5G and It's Surrounding Situations until 2020, T. Tsutsui, SoftBank Corp., Japan

Everybody getting excited with the 5G, mixing cats and dogs together. But the reality is, there is physical limitations and no magic, we should be cool. Whereas a lot would get to be possible and that should not be under estimated, and we should know what would be possible and what would not. Industry experts should be able to figure out better images before it actually comes, so as not to make big mistakes. Looking around 5G and it's surrounding technologies, in view of capabilities and physical limitations, I would like to briefly survey situations around forthcoming these years. So far with my experience, I believe I can figure out a little bit better images, and can help a little.

T1-3 - 9:25 (Plenary)
Privacy and Security: Key Requirements for Sustainable IoT Growth, F. Assaderaghi, G. Chindalore, B. Ibrahim, H. de Jong, M. Joye, S. Nassar, W. Steinbauer, M. Wagner and T. Wille, NXP Semiconductors, USA

As IoT moves beyond a catchphrase and starts to provide meaningful solutions in multiple fields, three of its critical pillars are now well understood:
- Transducers are needed as means of interacting with the environment and machines, and in converting stimuli to data and vice versa. These sensors and actuators form the basis of contextual awareness.
- Given that many end-node IoT devices are size and power constrained, local low-power computing is essential. The need for power-efficient end-node and edge computing becomes more apparent when latency, network bandwidth, and real time analytics are considered.
- Low power communication links to transmit the data between IoT devices and local aggregators or cloud resources form the third pillar.

Missing in this picture, and not fully appreciated yet, is the fourth pillar of IoT: privacy and security (P&S). If IoT is all about data, how P&S is treated will determine IoT's fate: a second phase of rapid proliferation or ultimate demise and collapse. Recent breaches in P&S are starting to change the industry's view on this issue. Even IoT end nodes that are low cost and have limited functionality pose significant risk to the entire system when their security is breached. This is due to the networking nature of the IoT that exposes a massive attack surface, making these devices ideal attack points for causing disruptions and stealing sensitive data. PC-era Internet security has been an expensive afterthought that has cost industry and consumers billions of dollars. Therefore, we should approach IoT differently, making P&S a key requirement at the design phase itself, and address all life-cycle aspects from initial deployment to in-field updates, to end-of-life decommissioning. This is a system level challenge that requires complete end-end HW/SW solutions, developed in partnership with the entire ecosystem.

SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Tuesday, June 6, 10:30-12:30

Chairpersons: M. Ikeda, The Univ. of Tokyo
                 K. Chang, Xilinx Inc.

C1-1 - 10:30
Welcome and Opening Remarks
M. Motomura, Hokkaido Univ.
G. Lehmann, Infineon Technologies AG

C1-2 - 10:50 (Plenary)
Innovative Solutions toward Future Society with AI, Robotics, and IoT, T. Yukitake, Panasonic Corp., Japan

AI, Robotics, and IoT have attracted enormous attention, expected to greatly change our society in the future. With these innovative technologies, our society would become (1) a borderless communication society, (2) a symbiotic society with robots, and (3) a safe, secure and comfortable network society. This plenary talk will show our specific initiatives, aiming at society heading for the futures, namely, (1) automatic translation, (2) underwater robot, and (3) large scale monitoring system. All of them work in collaboration with cloud, and will evolve into an advanced system. At the same time, higher performance and more intelligent processing is required on the edge side, thus we expect VLSI to play even more important roles.

C1-3 - 11:40 (Plenary)
Inside Waymo's Self-Driving Car: My Favorite Transistors, D. L. Rosenband, Waymo, USA

Waymo's self-driving Acbasrtsr acct ontain a broad set of technologies that enable our cars to sense the vehicle surroundings, perceive and understand what is happening in the vehicle vicinity, and determine the safe and efficient actions that the vehicle should take. Many of these technologies are rooted in advanced semiconductor technologies, e.g. faster transistors that enable more compute or low noise designs that enable the faintest sensor signals to be perceived. This paper summarizes a few areas where semiconductor technologies have proven to be fundamentally enabling to self-driving capabilities. The paper also lays out some of the challenges facing advanced semiconductors in the automotive context, as well as some of the opportunities for future innovation.

SESSION 2

Machine / Deep Learning [Suzaku III]

Tuesday, June 6, 14:00-15:40

Chairpersons: S. Nimmagadda, Intel Technology India Pvt Ltd.
                 V. Sze, Massachusetts Institute of Technology

C2-1 - 14:00
BRein Memory: A 13-Layer 4.2 K Neuron/0.8 M Synapse Binary/Ternary Reconfigurable In-Memory Deep Neural Network Accelerator in 65 nm CMOS, K. Ando*, K. Ueyoshi*, K. Orimo*, H. Yonekawa**, S. Sato**, H. Nakahara**, M. Ikebe*, T. Asai*, S. Takamaeda-Yamazaki*, T. Kuroda*** and M. Motomura*, *Hokkaido Univ., **Tokyo Institute of Technology and ***Keio Univ., Japan

A versatile reconfigurable accelerator for binary/ternary deep neural networks (DNNs) is presented. It features a massively parallel in-memory processing architecture and stores varieties of binary/ternary DNNs with a maximum of 13 layers, 4.2 K neurons, and 0.8 M synapses on chip. The 0.6 W, 1.4 TOPS chip achieves performance and energy efficiency that is 10-100 and 100-10,000 times better than a CPU/GPU/FPGA.

C2-2 - 14:25
A 1.06-To-5.09 TOPS/W Reconfigurable Hybrid-Neural-Network Processor for Deep Learning Applications, S. Yin, P. Ouyang, S. Tang, F. Tu, X. Li, L. Liu and S. Wei, Tsinghua Univ., China

An energy-efficient hybrid neural network (NN) processor is implemented in a 65nm technology. It has two 16x16 reconfigurable heterogeneous processing elements (PEs)arrays. To accelerate a hybrid-NN, the PE array is designed to support on demand partitioning and reconfiguration for parallel processing different NNs. To improve energy efficiency, each PE supports bit-width adaptive computing to meet variant bit-width of different neural layers. Measurement results show that this processor achieves a peak 409.6GOPS running at 200MHz and at most 5.09TOPS/W energy efficiency. This processor outperforms the state-of-the-art up to 5.2X in energy efficiency.

C2-3 - 14:50
A Heterogeneous Microprocessor for Energy-Scalable Sensor Inference Using Genetic Programming, H. Jia, J. Lu, N. K. Jha and N. Verma, Princeton Univ., USA

We present a heterogeneous microprocessor for IoE sensor-inference applications, which achieves programmability required for feature extraction strictly using application data. Acceleration, though key for energy efficiency, poses substantial programmability challenges. These are overcome by exploiting genetic programming (GP) for automatic program synthesis. GP yields highly structured models of computation, enabling: (1) high degree of specialization; (2) systematic mapping of programs to the accelerator; and (3) energy scalability via user-controllable approximation. The microprocessor (130nm) achieves $325\times/156\times$ energy reduction, and further $20\times/9\times$ energy scalability, for programmable feature extraction in two medical-sensor applications (seizure/arrhythmia-detection) vs. GP-model execution on CPU. The energy efficiency is 220 GOPS/W, near that of fixed-function accelerators, exceeding typical programmable accelerators.

C2-4 - 15:15
A 3.43TOPS/W 48.9pJ/Pixel 50.1nJ/Classification 512 Analog Neuron Sparse Coding Neural Network with On-Chip Learning and Classification in 40nm CMOS, F. N. Buhler*, P. Brown*, J. Li*.**, T. Chen*, Z. Zhang* and M. P. Flynn*, *Univ. of Michigan and **Intel Corp., USA

A digital-analog hybrid neural network exploits efficient analog computation and digital intra-network communication for feature extraction and classification. Taking advantage of the inherently low SNR requirements of the Locally Competitive Algorithm (LCA), the internally-analog neuron is 3x smaller and 7.5x more energy efficient than an equivalent digital design. This work demonstrates large-scale integration of 512 analog neurons using a traditional scalable digital workflow to achieve a best-of-class power efficiency of 3.43TOPS/W for object classification. At 48.9pJ/pixel and 50.1nJ/classification, the prototype 512-neuron IC achieves 2x efficiency over the digital design while maintaining reliable classification results over PVT.

SESSION 3

Delta-Sigma Modulators [Suzaku II]

Tuesday, June 6, 14:00-15:40

Chairpersons: Y.-S. Shu, MediaTek Inc.
               Y. Chiu, The Univ. of Texas at Dallas

C3-1 - 14:00
A 4.2mW 10MHz BW 74.4dB SNDR Fourth-Order CT DSM with Second-Order Digital Noise Coupling Utilizing an 8b SAR ADC, I.-H. Jang*, M.-J. Seo*, M.-Y. Kim*, J.-K. Lee**, S.-Y. Baek**, S.-W. Kwon**, M. Choi**, H.-J. Ko** and S.-T. Ryu*, *KAIST and **Samsung Electronics Co., Ltd., Korea

A compact and low-power digital-domain noise coupling technique is proposed for higher-order CT DSM implementation, exploiting the architectural advantage of a SAR ADC and a simple digital filter. With an 8b SAR ADC and a second-order digital noise coupling filter, a prototype fourth-order DSM achieves 74.4dB SNDR for 10MHz BW with an OSR of 16 in a 28nm CMOS, showing an FoM_{S_DR} of 174.5dB.

C3-2 - 14:25
A 0.028mm^2 19.8fJ/step 2nd-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback in 40nm CMOS, S. Li and N. Sun, The Univ. of Texas at Austin, USA

This paper presents an OTA-less 2nd-order VCO-based CT ΔΣ modulator featuring a passive integrator that makes use of the VCO's inherent parasitic effect. A low-power capacitive feedback technique is also presented for robust loop compensation. Fabricated in 40nm CMOS, the prototype occupies 0.028mm^2 of active area and consumes 524μW when sampling at 330MHz. The ΔΣM achieved peak Walden FoM of 19.8fJ/step with 68.6dB SNDR over 6MHz BW.

C3-3 - 14:50
A 5GS/s 156MHz BW 70dB DR Continuous-Time Sigma-Delta Modulator with Time-Interleaved Reference Data-Weighted Averaging, M. B. Dayanik, D. Weyer and M. P. Flynn, Univ. of Michigan, USA

The continuous time ΣΔ ADC architecture is very attractive for high dynamic range applications, however conventional dynamic element matching methods to improve DAC accuracy introduce too much loop delay and limit ADC speed.This work introduces a Time-Interleaved Reference Data-Weighted-Averaging (TI-RDWA) architecture that breaks the speed limitation of the traditional DEM decoder. Time interleaving eliminates the reference voltage settling bottleneck, enabling DWA operation at 5GHz, while still achieving the benefits of first order shaping of feedback DAC mismatch. The prototype 5GS/s ADC with TI-RDWA improves SFDR by 17dB resulting in a measured 70dB dynamic range and 84dB SFDR from a 156MHz bandwidth. The prototype, fabricated in 40nm CMOS, consumes 233mW.

C3-4 - 15:15
A 55μW 93.1dB-DR 20kHz-BW Single-Bit CT ΔΣ Modulator with Negative R-Assisted Integrator Achieving 178.7dB FoM in 65nm CMOS, M. Jang, S. Lee and Y. Chae, Yonsei Univ., Korea

This paper presents a power-efficient 3rd order single-bit Continuous Time ΔΣ modulator with active-RC integrators using negative-*R* assistant at virtual ground. The virtual ground of an active-RC integrator is assisted with negative R to relax opamp's specifications, such as open-loop gain, unity-gain bandwidth, thermal noise and linearity leading to a drastic power-saving. Fabricated in a 65nm CMOS process, the modulator occupies area of $0.27mm^2$. It achieves 100.5dB SFDR and 93.1dB DR in 20kHz BW, while consuming only 55μW from a 1.2V supply. This results in Schreier FoM of 178.7dB and Walden FoM of 63.1fJ/step which achieves the highest energy efficiency among audio CTDSMs implemented in 65nm CMOS.

SESSION 4

Biomedical Circuits and Systems [Suzaku I]

Tuesday, June 6, 14:00-15:40

Chairpersons: J. Ohta, Nara Institute of Science and Technology
            D. Sylvester, Univ. of Michigan

C4-1 - 14:00
A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-Directional Data Telemetry for Real-Time Human Epileptic Seizure Control, C.-H. Cheng, P.-Y. Tsai, T.-Y. Yang, W.-H. Cheng, T.-Y. Yen, Z. Luo, X.-H. Qian, Z.-X. Chen, T.-H. Lin, W.-H. Chen, W.-M. Chen, S.-F. Liang, F.-Z. Shaw, C.-S. Chang, F.-Y. Shih, Y.-L. Hsin, C.-Y. Lee, M.-D. Ker and C.-Y. Wu, National Chiao Tung Univ., Taiwan

This paper presents a 16-channel closed-loop neuromodulation SoC for human seizure control. The SoC includes a 16-ch signal acquisition unit, a bio-signal processor, a 16-ch adaptive stimulator, and wireless telemetry. The signal acquisition unit achieves 3.78 NEF and shares electrodes with stimulator. The seizure detection latency is 0.76s and delivered 0.5-3mA biphasic current stimulation. The SoC is powered wirelessly and bidirectional data telemetry is realized through the same pair of coils in 13.56MHz.

C4-2 - 14:25
A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing, X.-H. Qian*, Y.-C. Wu**, T.-Y. Yang*, C.-H. Cheng*, H.-C. Chu*, W.-H. Cheng*, T.-Y. Yen*, T.-H. Lin*, Y.-J. Lin*, Y.-C. Lee*, J.-H. Chang*, S.-T. Lin*, S.-H. Li**, T.-C. Wu*, C.-C. Huang**, C.-F. Lee***, C.-H. Yang**, C.-C. Hung*, T.-S. Chi*, C.-H. Liu**, M.-D. Ker* and C.-Y. Wu*, *National Chiao Tung Univ., **National Taiwan Univ. and ***Hualien Tzu Chi Medical Center, Taiwan

In this paper, a bone-guided cochlear implant (BGCI) SOC microsystem is proposed and designed. The BGCI microsystem uses four or more electrodes placed on the bone surface of the cochlea and one on the round window to preserve partially the acoustic hearing. The external SOC of the BGCI processes the acoustic signals and generates stimulation patterns and command that are transmitted to the implanted chip through the 13.56MHz wireless power and bidirectional data telemetry. The implanted chip with 4-channel high-voltage-tolerant stimulator generates biphasic stimulation currents up to 800μA and sends back the power indication and electrode impedance error signals to the external SOC. Electrical tests on the fabricated BGCI has been performed. The in-vivo animal tests on guinea pigs has shown the evoked Wave III of EABR waveforms. The proposed BGCI can be applied to patients with high-frequency hearing loss, tinnitus, and dizziness.

C4-3 - 14:50
An Implantable 700μW 64-Channel Neuromodulation IC for Simultaneous Recording and Stimulation with Rapid Artifact Recovery, B. C. Johnson*,**, S. Gambini, I. Izyumin*, A. Moin**, A. Zhou**, G. Alexandrov**, S. R. Santacruz**, J. M. Rabaey**, J. M. Carmena** and R. Muller*,**, *Cortera Neurotechnologies, Inc. and **Univ. of California, Berkeley, USA

We present an 180nm HV CMOS IC for concurrent neural stimulation and recording that combines 64 low-noise recording front-ends and 4 independent stimulators multiplexed to any of the 64 channels. The stimulators have 5mA peak current, 12V compliance and dynamic power management to maximize efficiency. Co-design of the stimulation and recording subsystems resulted in 100mV of recording linear range, 70nV/rtHz noise, and a rapid 1ms (single-sample) artifact recovery during stimulation.

C4-4 - 15:15
Intraneural Active Probe for Bidirectional Peripheral Nerve Interface, M. Ballini*, J. Bae*, N. Marrocco*, R. Verplancke**, D. Schaubroeck**, D. Cuypers**, M. Cauwe**, J. O'Callaghan*, A. Fahmy***, N. Maghari***, R. Bashirullah***, C. V. Hoof*,****, N. V. Helleputte*, M. O. de Beeck*,**, D. Braeken* and S. Mitra*, *imec, **CMST (imec/Univ. of Ghent), Belgium, ***Univ. of Florida, USA and ****KU Leuven, Belgium

Advanced bionic prosthetics that can restore both the motor functionality and sensory perception of an amputee, require high-resolution recording and stimulation interfaces targeting the peripheral nervous system (PNS). To provide high nerve fiber selectivity, we propose a low-noise (3.67μVrms), low-power (2.24mW) and high-density CMOS microelectrode probe for intra-neural implantation. The probe is composed of two ICs, encapsulated in a biocompatible and hermetic package, each featuring 64 recording and 16 stimulation electrodes. A backend IC digitizes the recorded signals at 31.25kS/s and provides spike detection.

SESSION 5

Application Specific I/Os [Suzaku III]

Tuesday, June 6, 16:00-18:05

Chairpersons: Y. Tomita, Fujitsu Laboratories Ltd.
                 A. Momtaz, Broadcom Corp.

C5-1 - 16:00
A 5Gb/s 7.1fJ/b/mm 8× Multi-Drop On-Chip 10mm Data Link in 14nm FinFET CMOS SOI at 0.5V, E. Sacco*,**, P. A. Francese*, M. Brändli*, C. Menolfi*, T. Morf*, A. Cevrero*, I. Ozkaya*, M. Kossel*, L. Kull*, D. Luu*, H. Yueksel*, G. Gielen** and T. Toifl*, *IBM Research, Switzerland and **KU Leuven, Belgium

We report a 5Gb/s data link implemented in 14nm FinFET CMOS SOI technology in which a single transmitter (TX) broadcasts NRZ data to eight receivers (RXs) distributed along an on-chip RC-dominated 10mm-long channel. The TX comprises a full-rate AC-coupled 2-tap FIR driver with a quarter-rate pre-driver. Each RX is equipped with a novel decision-gated 1-tap speculative DFE optimized for low-power. Correct operation was verified with PRBS31 data transmitted at 5Gb/s and concurrently received error free at each drop with >40% horizontal margin (BER<10^{-12}). At this data rate the efficiency is 7.1fJ/b/mm, resulting in the best performance among multi-drop on-chip data links so far published. The TX and eight RXs are running on a 0.5V power supply and consume 0.62 and 0.98mW, respectively.

C5-2 - 16:25
A 10Gb/s 10mm On-Chip Serial Link in 65nm CMOS Featuring a Half-Rate Time-Based Decision Feedback Equalizer, P.-W. Chiu, S. Kundu, Q. Tang and C. H. Kim, Univ. of Minnesota, USA

An all-digital 2-tap half-rate time-based decision feedback equalizer (TB-DFE) was demonstrated on a 10mm on-chip serial link. Implemented in a 65nm GP technology, the transmitter and receiver achieve an energy-efficiency of 31.9 and 45.3 fJ/b/mm, respectively, at a data rate of 10Gb/s. A Bit Error Rate (BER) less than 10^{-12} was verified for an eye width of 0.43 Unit Interval (UI) using an in-situ BER monitor.

C5-3 - 16:50
An FFE TX with 3.8x Eye Improvement by Automatic Impedance Adaptation for Universal Compatibility with Arbitrary Channel and RX Impedances, M. Choi, S. Lee, M. Lee, J. Lee, J.-Y. Sim, H.-J. Park and B. Kim, POSTECH, Korea

An FFE TX which automatically adapts impedance to arbitrary channel and RX impedances is proposed. Based on on-chip TDR monitoring, the TX impedance matching is adaptively relaxed without increasing reflection. In experiment, the proposed TX adapted to any combination of 35-75Ω channels and 30-200Ω RX impedances, achieving 3.8x eye improvement and the maximum data rate of 12Gb/s.

C5-4 - 17:15
A Distance-Immune Low-Power 4-Mbps Inductively-Coupled Bidirectional Data Link, A. Yousefi, D. Yang, A. A. Abidi and D. Marković, Univ. of California, Los Angeles, USA

A distance-immune inductively coupled link is based on a free-running oscillator tuned by coupled resonators. It can transfer data at up to 4 Mbps and 2 Mbps in half-duplex with an LSK uplink and ASK downlink, respectively (at BER< 5×10^{-8}). In uplink direction, the implanted unit consumes less than 0.1 pJ/bit while transmitting.

C5-5 - 17:40
A 16.6-pJ/b 150-Mb/s Body Channel Communication Transceiver with Decision Feedback Equalization Improving >200% Area Efficiency, J.-H. Lee, K. Kim, M. Choi, J.-Y. Sim, H.-J. Park and B. Kim, POSTECH, Korea

This paper presents the fastest and most energy efficient body channel communication transceiver integrated into the smallest chip area. To enhance data rate with limited human body channel bandwidth, decision feedback equalization technique is adopted to body channel communication for the first time. The transceiver, fabricated in 65 nm CMOS technology, reliably (BER < 10^{-6}) achieves the maximum data rates of 150 Mb/s and 100 Mb/s over 20-cm and 1.0 m human body channels at costs of 16.6 pJ/b and 23.5 pJ/b. Even with the drastic performance improvements, the transceiver only occupies an area of 5580 μm^2, which is of less than 1% compared to any previously presented works. This remarkable area efficiency verifies the superiority of the proposed design's simplicity of and efficiency.

SESSION 6

Circuits Focus Session - Ultra-Low Power Wireless Transceivers for IoT Systems [Suzaku II]

Tuesday, June 6, 16:00-18:05

Chairpersons: H. Ishikuro, Keio Univ.
                 M. Chen, Univ. of Southern California

C6-1 - 16:00 (Invited)
Reaching 10-Years of Battery Life for Industrial IoT Wireless Sensor Networks, X. Lu, I. H. Kim, A. Xhafa, J. Zhou and K. Tsai, Texas Instruments, USA

In this paper we present methods to reach 10-years of battery life for Industrial Internet of Things (IIoT) wireless sensor network (WSN) using a platform called the I3Mote. I3Mote provides connected sensor nodes for tough industrial environment and a number of I3Motes can form a large-scale coverage of data collectors or actuators. The goal is to achieve 10-years network life time for all the connected battery powered nodes with a duty cycle of data collection (uplink traffic) in 10 seconds. Due to the ubiquitous optimization of hardware (sensors, connectivity, MCU, HMI and PM), protocol, localized data process, etc. we see a light through the tunnel. This paper will go through techniques of power optimization at device and network level to extend the battery life to industry standard of 10 years.

C6-2 - 16:25
A 1.7nW PLL-Assisted Current Injected 32KHz Crystal Oscillator for IoT, Y. Zeng, T. Jang, Q. Dong, M. Saligane, D. Sylvester and D. Blaauw, Univ. of Michigan, USA

This paper presents a PLL-assisted crystal oscillator using a current switching phase detector (PD) with intrinsic 90° phase offset for IoT applications. The PLL provides accurate pulse injection timing into the XO, sustaining its oscillation at only 100mV amplitude and ensuring robustness operation across PVT. This technique achieves high energy injection efficiency and avoids the use of power hungry amplifiers. Measured power is 1.7nW at room temperature and operation is demonstrated from -20 – 80°C and across 3 corner wafers.

C6-3 - 16:50
A 2.4GHz, -102dBm-Sensitivity, 25kb/s, 0.466mW Interference Resistant BFSK Multi-Channel Sliding-IF ULP Receiver, H.-G. Seok, O.-Y. Jung, A. Dissanayake and S.-G. Lee, KAIST, Korea

This paper presents an ultra-low power, high-sensitivity, and interference-resistant receiver suitable for IoT applications. By the combination of sliding-IF based low-power down-conversion and relative-power-detection based FSK demodulation, the proposed receiver achieves multi-channel operation and minimizes power consumption. Cascaded N-path filter and 4th-order hybrid-PPF are adopted to improve the sensitivity and carrier-to-interference ratio. Implemented in a 65nm CMOS, the receiver achieves -102dBm sensitivity at 0.1% BER and 25kb/s data rate while consuming 466µW from a 0.6V supply.

C6-4 - 17:15
A 16 nm FinFET 0.4 V Inductor-Less Cellular Receiver Front-End with 10 mW Ultra-Low Power and 0.31 mm² Ultra-Small Area for 5G System in Sub-6 GHz Band, E.-H. V. Yeh, A.-H. Lo, W.-S. Chen, T.-J. Yeh and M. Chen, TSMC, Taiwan

This work presents an inductor-less 0.4 V cellular receiver (RX) front-end with an ultra-low power of 10 mW and an ultra-small area 0.31 mm² in 16 nm FinFET technology, which enables massive receivers in a single chip for 10 Gb/s high throughput 5G system in sub-6 GHz band. The proposed inductor-less low-Vdd RX front-end consists of an LNA, passive mixers, LO generator and 20MHz bandwidth channel filters. By using the proposed current stabilization circuit in 0.4 V channel filter, the current variation with process corners is greatly reduced. This RX front-end can achieve a noise figure of 2.5dB, an in-band IIP3 of -6 dBm, a voltage gain of 35 dB at 2.1 GHz Band-I frequency. To the best of authors' knowledge, this work demonstrates the lowest power consumption with minimum chip area and a competitive performance under the lowest supply voltage of 0.4 V, compared with the prior arts.

C6-5 - 17:40 (Invited)
A Multi-Mode WPAN (Bluetooth, BLE, IEEE 802.15.4) SoC for Low-Power and IoT Applications, A. Zolfaghari, M. E. Said, M. Youssef, G. Zhang, T. Liu, F. Cattivelli, Y. Syllaios, F. Khan, F. Fang, J. Wang, K.-Y. Li, F. Liao, D. Jin, V. Roussel, D.-U. Lee and F. Hameed, Broadcom Corp., USA

A multi-mode WPAN transceiver implemented in an SoC is presented. Fabricated in 40-nm CMOS, the chip supports IEEE 802.15.4 and all modes of Bluetooth. Consuming 7.8 mW from a 1.2-V supply, the receiver has a sensitivity of -104, -98, -95/-94/-88 dBm in 802.15.4, BLE and Bluetooth BDR/EDR2/EDR3, respectively. The transmitter has a power consumption of 10 mW to deliver 0 dBm output in the constant envelope mode and 14.5 mW in BT EDR.

SESSION 7

Sensor Readout Circuits [Suzaku I]

Tuesday, June 6, 16:00-17:40

Chairpersons: T. Okumoto, Socionext Inc.
                C. Sandner, Infineon Technologies AG

C7-1 - 16:00
A Compact Sensor Readout Circuit with Combined Temperature, Capacitance and Voltage Sensing Functionality, B. Yousefzadeh*, W. Wu*, B. Buter**, K. A. A. Makinwa* and M. Pertijs*, *Delft Univ. of Technology and **NXP Semiconductors, The Netherlands

This paper presents an area- and energy-efficient sensor readout circuit, which can precisely digitize temperature, capacitance and voltage. The three modes use only on-chip references and employ a shared zoom ADC based on SAR and ΔΣ conversion to save die area. Measurements on 24 samples from a single wafer show a temperature inaccuracy of ±0.2 °C (3σ) over the military temperature range (-55°C to 125°C). The voltage sensing shows an inaccuracy of ±0.5%. The sensor also offers 18.7-ENOB capacitance-to-digital conversion, which handles up to 3.8 pF capacitance with a 0.76 pJ/conv.-step energy-efficiency FoM. It occupies 0.33 mm² in a 0.16 µm CMOS process and draws 4.6 µA current from a 1.8 V supply.

C7-2 - 16:25
A 9.1 mW Inductive Displacement-to-Digital Converter with 1.85 nm Resolution, V. Chaturvedi, J. G. Vogel, K. A. A. Makinwa and S. Nihtianov, Delft Univ. of Technology, The Netherlands

A displacement-to-digital converter (DDC) based on inductive (eddy-current) sensor is presented. The sensor is embedded in a self-oscillating front-end, whose 145MHz output is then digitized by a ratiometric ΔΣ ADC. Over a 10µm range, the DDC achieves 1.85nm resolution (1.02 pH), in a 2kHz bandwidth. It draws 9.1mW from a 1.8V supply making it the most energy-efficient ECS interface ever reported.

C7-3 - 16:50
A CMOS Temperature Sensor with a 49fJ·K² Resolution FoM, S. Pan, H. Jiang and K. A. A. Makinwa, Delft Univ. of Technology, The Netherlands

This paper presents the most energy-efficient CMOS temperature sensor ever reported, with a resolution FoM of 49fJ·K², 2.7× better than the state-of-the-art. It consists of a Wheatstone bridge made from poly-silicon resistors, which is readout by a 2nd-order Continuous-Time Delta-Sigma modulator (CTDSM). This approach leads to a high resolution (160µK in 10ms) and a low supply-voltage sensitivity (< 20mK/V at room temperature).

C7-4 - 17:15
A 0.06mm² ± 50mV Range -82dB THD Chopper VCO-Based Sensor Readout Circuit in 40nm CMOS, C.-C. Tu, Y.-K. Wang and T.-H. Lin, National Taiwan Univ., Taiwan

A VCO-based sensor readout circuit is presented. It comprises a VCO-based integrator with counters, and a capacitively-coupled feedback DAC, to form a 1st-order DSM with high input impedance and wide dynamic range for voltage sensors. Chopping is applied to suppress the flicker noise. The time-domain approach relaxes the voltage swing requirement compared to that of a Gm-C integrator, and thus area efficiency is achieved. The prototype is implemented in 40nm CMOS. It consumes 21µA under 1.2V supply. With a 100mV$_{pp}$ sinusoidal input, it achieves 74.9dB SNDR over 2 kHz BW and the THD is -82dB. This readout circuit is also measured with a Hall sensor to demonstrate its operation. The FoM and distortion achieves the state-of-the-art performance of VCO-based sensor readout circuits.

IEEE SSCS Young Professional Mentoring Event [Suzaku I]

Tuesday, June 6, 18:15-19:30

Symposium on VLSI Circuits

30th Anniversary Celebration [Suzaku II, III]

Tuesday, June 6, 19:30-20:00

Alcoholic and Non-Alcoholic beverages will be served.

Both Technology/Circuits Symposia attendees are cordially invited.

Technology / Circuits Joint Evening Panel Discussion

How will We Survive the Post-Scaling Era? [Shunju II, III]

Tuesday, June 6, 20:00-21:30

Organizers: S. Nimmagadda, Intel Technology India Pvt Ltd.
             T. Tsunomura, Tokyo Electron Ltd.
             C. Mazure, Soitec Group

Moderator: T. Letavic, GLOBALFOUNDRIES

Panelists: R. Moore, ARM Ltd.
             J. Burns, IBM
             Y. Jeon, Samsung Electronics Co., Ltd.
             F. Boeuf, The Univ. of Tokyo
             J. Ryckaert, imec

For many decades the semiconductor industry has enjoyed the benefits of scaling. Every 2 years or so a new process node would arrive, bringing with it reduced area, along with improved performance and power. In recent years, we have seen and overcome many challenges to the scaling model, necessitating considerable efforts in VLSI circuits and technology. While we have largely maintained area scaling, obtaining even modest node-to-node improvements in performance and power has been difficult.
New applications require much higher level compute than ever before which we are aiming to do via accelerators, programmable fabrics etc. These implementations respond very well with technology scaling.
However, we are now approaching the biggest challenge yet. What happens when scaling slows to the point that it has, for practical purposes, stopped? How will we survive the post-scaling era? Our panel of experts, spanning VLSI technology, circuits, and business, looks at the difficulties ahead and potential ways forward.

Circuits Evening Panel Discussion

The Most Important Circuits of 2037 [Suzaku I]

Tuesday, June 6, 20:00 - 21:30

Organizers: H. Ishikuro, Keio Univ.
B. K. Casper, Intel Corp.

Moderator: K. Makinwa, Delft Univ.

Panelists: J. Myers, ARM Ltd.
P. Harpe, Eindhoven Univ. of Technology
H. Tamura, Fujitsu Laboratories Ltd.
C. Thakkar, Intel Corp.
J. Yoo, National Univ. of Singapore
K. Nose, Renesas Electronics Corp.
K. Zhang, TSMC

This year, the Symposium on VLSI Circuits celebrates its 30th anniversary. Many innovative circuit design techniques have been presented over the history of symposium, but what does the future hold? What kinds of VLSI circuits will be presented, and for what kind of applications, at the 2037 Symposium on VLSI Circuits? In short, what will be the most important circuits of 2037? In response to this question, the panelists, who are a mix of young and senior specialists from across the circuits spectrum, give us their version of the future 20 years from now, with an entertaining mix of fantasy, science fiction and humor in their contributed VLSI circuits.

SESSION 8

Pipelined ADCs [Suzaku II]

Wednesday, June 7, 8:30-10:10

Chairpersons: C. P. Yue, Hong Kong Univ. of Science and Technology
S. Ho, MediaTek Inc.

C8-1 - 8:30
A 16nm 69dB SNDR 300MSps ADC with Capacitive Reference Stabilization, E. Martens, B. Hershberg and J. Craninckx, imec, Belgium

We present a 300 MSps 2 times interleaved pipelined SAR ADC in 16nm digital CMOS. It implements a new scheme to cancel reference voltage ripple due to DAC switching, greatly reducing requirements for decoupling capacitance and/or reference buffering, and achieves better than 76dB harmonic distortion. At 300 MSps, the peak ENOB is 11.2 bit with a power consumption of 3.6mW.

C8-2 - 8:55
A 9.1 ENOB 21.7fJ/conversion-step 10b 500MS/s Single-Channel Pipelined SAR ADC with a Current-Mode Fine ADC in 28nm CMOS, K.-J. Moon*,**, H.-W. Kang*, D.-S. Jo*, M.-Y. Kim*, S.-Y. Baek**, M. Choi**, H.-J. Ko** and S.-T. Ryu*, *KAIST and **Samsung Electronics Co., Ltd., Korea

A single-channel 10b pipelined SAR ADC with a gm-cell residue amplifier and a current-mode fine SAR ADC achieves a 500MS/s conversion rate in a 28nm CMOS process under a 1.0V supply. With background offset and gain calibration, the prototype ADC achieves an SNDR of 56.6dB at Nyquist. With power consumption of 6mW, it obtains a FoM of 21.7fJ/conversion-step.

C8-3 - 9:20
A Single-Channel, 600Msps, 12bit, Ringamp-Based Pipelined ADC in 28nm CMOS, J. Lagos*,**, B. Hershberg*, E. Martens*, P. Wambacq*,** and J. Craninckx*, *imec and **Vrije Universiteit Brussel (VUB), Belgium

A pipelined ADC is presented that exploits the low but very constant (over output swing) open-loop gain characteristic of the ring amplifier to achieve high SFDR in low-voltage nanoscale CMOS designs. A dynamic ring amplifier (ringamp) biasing scheme using CMOS resistors and an active ringamp-based common-mode feedback are also introduced. The implemented prototype achieves 56.3dB SNDR and 69.2dB SFDR at 600Msps, consuming 14.2mW from a 0.9V supply, resulting in a Figure-of-Merit of 44.3fJ/conv.-step.

C8-4 - 9:45
A Calibration-Free 2.3 mW 73.2 dB SNDR 15b 100 MS/s Four-Stage Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC, Y. Lim*,** and M. P. Flynn*, *Univ. of Michigan, USA and **Samsung Electronics Co., Ltd., Korea

A four-stage fully differential ring amplifier in 40 nm CMOS improves gain to over 90 dB without compromising speed. It is applied in a 15b, 100 MS/s calibration-free SAR-assisted pipeline ADC. In addition, a new auto-zero noise filtering method reduces noise without consuming additional power. The ADC achieves 73.2 dB SNDR (11.9b) and 90.4 dB SFDR with a 1.1 V supply. It consumes 2.3 mW resulting in a SNDR based Schreier FoM of 176.6 dB.

SESSION 9

Sensors for Biomedical Applications [Suzaku I]

Wednesday, June 7, 8:30-10:10

Chairpersons: M.-D. Ker, National Chiao Tung Univ.
                N. Verma, Princeton Univ.

C9-1 - 8:30
A 1.06 µW Smart ECG Processor in 65 nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring, S. Yin*, M. Kim*, D. Kadetotad*, Y. Liu**, C. Bae***, S. J. Kim***, Y. Cao* and J.-S. Seo*, *Arizona State Univ., USA, **Samsung Research Center, China and ***Samsung Advanced Institute of Technology, Korea

A smart wearable electrocardiographic (ECG) processor is presented for secure ECG-based biometric authentication and cardiac monitoring, including arrhythmia and anomaly detection. Data-driven Lasso regression and low-precision techniques are developed to compress the neural networks by 24.4X. The prototype chip fabricated in 65 nm LP CMOS consumes 1.06 µW at 0.55 V for real-time ECG authentication. Equal error rates of 0.74% and 1.7% are achieved on ECG-ID database and in-house 645-subject database, respectively.

C9-2 - 8:55
A High-Precision 36 mm^3 Programmable Implantable Pressure Sensor with Fully Ultrasonic Power-Up and Data Link, M. J. Weber*, Y. Yoshihara*.**, A. Sawaby*, J. Charthad*, T. C. Chang*, R. Garland* and A. Arbabian*, *Stanford Univ., USA and **Toshiba Corp., Japan

This paper presents the first fully ultrasonic (US) high-precision implantable sensor with active US links for power-up, data downlink, and data uplink. The packaged implant measures just 1.7×2.6×8.1mm^3 and includes a custom IC, piezoelectric devices (piezos) designed for data/power links, and a pressure transducer (PT). Characterization is performed at a large depth of 12 cm, in a phantom material, giving a >10× improvement over state-of-the-art in both the *depth/volume* and *energy per sample* figures of merit. The IC has a front-end and 10-bit ADC which achieves a pressure LSB of 0.78 mmHg and full-scale range of 800 mmHg, exceeding specifications required for various pressure monitoring applications. The sample rate is externally controlled, up to 1 kHz, through the downlink, allowing power optimization for various applications.

C9-3 - 9:20
Chip-Scale Fluorescence Imager for *In Vivo* Microscopic Cancer Detection, E. P. Papageorgiou*, B. E. Boser* and M. Anwar**, *Univ. of California, Berkeley and **Univ. of California, San Francisco, USA

Modern cancer treatment faces the pervasive challenge of identifying microscopic cancer foci *in vivo*, but no imaging device exists with the ability to identify these cells intraoperatively, where they can be removed. We introduce a novel CMOS sensor that identifies foci of less than 200 cancer cells labeled with fluorescent biomarkers in 50ms. The sensor's miniature size enables manipulation within a small, morphologically complex, tumor cavity. Recognizing that focusing optics traditionally used in fluorescence imagers present a barrier to miniaturization, we integrate stacked CMOS metal layers above each photodiode to form angle-selective gratings, rejecting background light and deblurring the image. A high-gain capacitive transimpedance amplifier based pixel with 8.2V/s per pW sensitivity and a dark current minimization circuit enables rapid detection of microscopic clusters of 100s of tumor cells with minimal error.

C9-4 - 9:45
A 4µW, ADPLL-Based Implantable Amperometric Biosensor in 65nm CMOS, A. Agarwal, A. Gural, M. Monge, D. Adalian, S. Chen, A. Scherer and A. Emami, California Institute of Technology, USA

This paper presents a fully implantable, wirelessly powered subcutaneous amperometric biosensor. We propose a novel ultra-low power all-digital phase-locked loop (ADPLL) based potentiostat architecture for electrochemical sensing. The system is wirelessly powered by near-field RF coupling of an on-chip antenna to an external coil at 915 MHz. Bi-directional wireless telemetry supports data transmission from the sensor to the external reader (uplink) via backscattering, and reconfiguration of the sensor chip over the RF downlink. The 1.2×1.2 mm^2 prototype is fabricated in TSMC 65nm CMOS process. The potentiostat achieves a 100pA sensitivity over a full scale current range of 0-350nA. The total power consumption of the system is 4µW.

Technology / Circuits Joint Focus Session 1

Emerging Reliability Solutions [Suzaku III]

Wednesday, June 7, 10:30-12:35

Chairpersons: M. Yamaoka, Hitachi, Ltd.
                E. Wang, Intel Corp.

JFS1-1 - 10:30
An Adaptive Clocking Control Circuit with 7.5% Frequency Gain for SPARC Processors, T. Hashimoto*, Y. Kawabe*, M. Hara**, Y. Kakimura**, K. Tajiri**, S. Shirota**, R. Nishiyama**, H. Sakurai**, H. Okano**, Y. Tomita*, S. Satoh** and H. Yamashita**, *Fujitsu Laboratories Ltd. and **Fujitsu Ltd., Japan

This paper presents an adaptive clocking control circuit to mitigate the processor performance degradation due to on-die supply voltage droops. The circuit utilizes multi-path TDC to reduce quantization errors and thermometer code-based data processing to eliminate latches, which shortens frequency modulation latency. This results in faster frequency/supply tracking. A test chip including the adaptive clocking control circuit with SPARC processor cores was fabricated in a 20-nm CMOS process. Experimental measurements demonstrated that the adaptive clocking control circuit achieved the state-of-the-art frequency gain of 7.5%, resulting in the operating frequency as high as 5 GHz.

JFS1-2 - 10:55
Statistical Characterization of Radiation-Induced Pulse Waveforms and Flip-Flop Soft Errors in 14nm Tri-Gate CMOS Using a Back-Sampling Chain (BSC) Technique, S. Kumar*, M. Cho**, L. Everson*, H. Kim*, Q. Tang*, P. Mazanec*, P. Meinerzhagen**, A. Malavasi**, D. Lake**, C. Tokunaga**, H. Quinn***, M. Khellah**, J. Tschanz**, S. Borkar**, V. De** and C. H. Kim*, *Univ. of Minnesota, **Intel Corp. and ***Los Alamos National Laboratory, USA

A novel BSC circuit with tunable current starved buffers demonstrates higher sensitivity, scalability & accurate statistical characterization of radiation-induced SET pulse waveforms & flip-flop SER in 14nm tri-gate CMOS, thus enabling improved SER estimation & analysis for a range of supply voltages including NTV. Neutron beam tests confirm that the proposed BSC chain can characterize Single Event Transients (SETs), Single Event Upsets (SEUs), and Multi Bit Upsets (MBUs) with high precision, thereby, offering insight into logic and memory SER, and its dependence on various circuit parameters.

JFS1-3 - 11:20
F_{MAX} / V_{MIN} and Noise Margin Impacts of Aging on Domino Read, Static Write, and Retention of 8T 1R1W SRAM Arrays in 22nm High-k/Metal-Gate Tri-Gate CMOS, J. P. Kulkarni, C. Tokunaga, M. Cho, M. M. Khellah, J. W. Tschanz and V. K. De, Intel Corp., USA

In this paper, we demonstrate by direct measurements and statistical analysis, progressive aging impacts on F_{MAX} and noise margin of the precharge-evaluate domino read, V_{MIN} for differential static write (with write assist), and retention over the operational lifetime of a 14KB 1R1W 8T SRAM array implemented in 22nm high-k/metal-gate tri-gate CMOS.

JFS1-4 - 11:45
Excellent Reliability of Ferroelectric HfZrO$_x$ Free from Wake-Up and Fatigue Effects by NH$_3$ Plasma Treatment, K.-Y. Chen, P.-H. Chen and Y.-H. Wu, National Tsing Hua Univ., Taiwan

With TiN/ferroelectric-HfZrO$_x$ (HZO)/TiN capacitors as the platform, NH$_3$ plasma treatment was employed at different HZO/TiN interfaces to investigate the impact on reliability. HZO free from wake-up and fatigue effects up to 10^6 cycles (± 2.5 MV/cm, long pulses width of 1 ms) with high κ value of 29~30, low leakage current and 2P$_r$ of 20.2 μC/cm^2 can be achieved by treatments at both top and bottom interfaces. It is a great advance for HfO$_2$-based FE and can be mainly attributed to significant reduction of oxygen vacancies (Vo) in HZO, especially treatment at bottom interface so that the interfacial TiO$_x$N$_y$ which causes oxygen-deficient HZO is effectively suppressed. NH$_3$-treated HZO has been physically confirmed with fewer Vo (lower non-lattice oxygen by 7 %) that is beneficial to suppress pinned domain walls and generation of new Vo during cycling, eliminating wake-up and fatigue effects. Conspicuously mitigated fatigue is also maintained at 85 °C.

JFS1-5 - 12:10
A 10MHz 5-to-40V EMI-Regulated GaN Power Driver with Closed-Loop Adaptive Miller Plateau Sensing, Y. Chen, X. Ke and D. B. Ma, The Univ. of Texas at Dallas, USA

To optimize the classic design trade-off between EMI noise and power efficiency in GaN power drivers at 10MHz and beyond, a closed-loop adaptive Miller Plateau sensing (AMPS) technique is proposed. In order to mitigate long delays and low accuracy issues in conventional Miller Plateau (MP) sensing approaches, an emulated MP tracking (EMPT) technique is adopted to achieve instant MP start point sensing. An isolated negative voltage sensor is designed for the EMPT to avoid considerable leakage current and enhance reliability without increasing circuit complexity. A noise-isolated feedback link ensures the closed-loop regulation accuracy by blocking the switching noise between HV and LV operation domains. Fabricated in a 0.35μm BCD process, the design achieves EMI reduction of 19.23dBμV in Band B (<30MHz) and over 9dBμV in Band C/D (>30MHz).

SESSION 10

Frequency Generation [Suzaku II]

Wednesday, June 7, 10:30-12:35

Chairpersons: J.-Y. Sim, POSTECH
                B. Nikolic, Univ. of California, Berkeley

C10-1 - 10:30
A Pulse-Tail-Feedback VCO Achieving FoM of 195dBc/Hz with Flicker Noise Corner of 700Hz, A. T. Narayanan, N. Li, K. Okada and A. Matsuzawa, Tokyo Institute of Technology, Japan

This paper proposes a pulse-tail-feedback technique for improving both $1/f^2$ and $1/f^3$ noises. The proposed VCO has separated tail transistors driven by inverters with rail-to-rail voltage swing. The tail transistor has an impulse shaped current waveform to improve FoM, and the flicker noise up-conversion is reduced by the switching operation. A prototype of the proposed VCO is implemented in 180nm CMOS, and the VCO achieves an FoM of 195dBc/Hz from 10kHz-10MHz offset with a flicker noise corner of 700Hz at 4.55GHz oscillation.

C10-2 - 10:55
A 3.2ppm/°C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting Technique, G. Zhang*, K. Yayama*, A. Katsushima* and T. Miki**, *Renesas System Design Co., Ltd. and **Renesas Electronics Corp., Japan

A CMOS on-chip oscillator (OCO) for local interconnection network (LIN) bus is presented. The temperature dependence of the output frequency is compensated by the voltage ratio adjusting (VRA) technique. The frequency variation with supply voltage is reduced by a voltage regulator with a wide input range of 1.8V to 5.0V. The frequency shift caused by package stress is minimized by resistor placement. Over a temperature range of -40°C to 150°C, the measured temperature coefficients of the output frequency are 3.2ppm/°C without the effect of the package stress and 14.2ppm/°C with that, respectively. The measured frequency variation with supply voltage is within ±0.015%.

C10-3 - 11:20
An 8GHz, 0.005mm² All Digital Clock Generator Having 0.1% Frequency Accuracy by New ZTC Algorithm, W. Kim, T. Kim, J. Kim and H. Ko, Samsung Electronics Co., Ltd., Korea

This work proposes an all digital clock generator (ADCG) with a new PVT compensation technique to generate a stable and accurate frequency over wide frequency ranges up to 8GHz. To compensate frequency variations by temperature changes, a novel Zero Temperature Coefficient (ZTC) algorithm using mutual compensation between the mobility and the threshold voltage of devices has been implemented. The proposed scheme achieves frequency accuracy of 0.1% or less over wide temperature ranges without any external reference clock. The experimental results of an ADCG having automatic ZTC algorithm in 28nm CMOS technology show 104 dB FOM, low power (0.49mW per GHz) and tiny size (0.005mm²).

C10-4 - 11:45
A 4GHz Clock Distribution Architecture Using Subharmonically Injection-Locked Coupled Oscillators with Clock Skew Calibration in 16nm CMOS, L.-C. Cho*, F.-W. Kuo*, R. Chen*, J. Liu*, C.-P. Jou*, F.-L. Hsueh* and R. B. Staszewski**, *TSMC, Taiwan and **Univ. College Dublin, Ireland

We propose a new approach to an on-chip clock distribution scheme. It is based on distributed multi-GHz LC-tank oscillators generating local clocks. The oscillators are mutually coupled to align their frequencies and are further subharmonically injection-locked to a much lower frequency reference to align their phases. The final phase calibration is via adjusting their self-resonant frequencies. We demonstrate the scheme with two 4GHz digitally controlled oscillators (DCO) separated by 650um on a 16nm CMOS die, mutually coupled via a differential transmission line and injection-locked to a 125MHz reference. The proposed architecture achieves a sub-ps calibrated skew with 87fs rms jitter while consuming 4.3mW, resulting in -258dB clock FOM (jitter²×power).

C10-5 - 12:10
A 5.12-GHz Fractional-*N* Frequency Synthesizer with an LC-VCO-Based MDLL, D.-E. Jhou, W.-S. Chang and T.-C. Lee, National Taiwan Univ., Taiwan

An LC-VCO-based MDLL is presented in a fractional-*N* frequency synthesizer to extend its frequency multiplication factor and performance. By employing the proposed MUXs in the LC-VCO, it increases the loop bandwidth (BW) from 3MHz to 15MHz (nearly $0.4f_{REF}$) as well as flicker noise suppression. Moreover, the re-quantized delta-sigma modulator (DSM) is combined with the prototype in order to reduce spurious tones and in-band noise, which come from the gain error of the digital-to-time converter (DTC). Fabricated in a 40 nm CMOS technology, the proposed MDLL with a large frequency multiplication factor of 128 exhibits an integrated jitter of 177fs (integer-*N)* and 326fs (fractional-*N))* with power consumption of 1.81mW and 2.38mW from a 0.9V supply at 5.12GHz respectively. The FoM_J of the proposed MDLL can be as good as -252.5dB (integer-*N))* and -246dB (fractional-*N))* with a reference frequency of 40MHz.

SESSION 11

Analog Techniques [Suzaku I]

Wednesday, June 7, 10:30-12:35

Chairpersons: K. Agawa, Toshiba Corp.
         R. Kapusta, Analog Devices, Inc.

C11-1 - 10:30
A Capacitively-Degenerated 100dB Linear 20-150MS/s Dynamic Amplifier, M. S. Akter*, K. A. A. Makinwa** and K. Bult**, *Broadcom Corp. and **Delft Univ. of Technology, The Netherlands

This paper presents a new dynamic residue amplifier for pipelined ADCs. With an input of $100mV_{pp,diff}$ and 4× gain, it achieves -100dB THD, the lowest ever reported in dynamic amplifiers. Compared to the state-of-the-art, it exhibits >25dB better linearity with >2× larger output swing and similar noise performance. The key to this is a new linearization technique based on capacitive-degeneration. Fabricated in a 28nm CMOS, the prototype amplifier dissipates 87μW at a clock speed of 43MS/s and maintains -100dB THD up to 150MS/s.

C11-2 - 10:55
A Hybrid Power Amplifier Using 3-Phase 3-Level Class-D with 200nH Inductors and Current Balancing Technique, J.-H. Choi*,** and G.-H. Cho*, *KAIST and **Samsung Electronics Co., Ltd., Korea

A hybrid power amplifier (PA_{HYBRID}), combining class-D and class-AB amplifier is demonstrated. As a specific structure for class-D, 3-level and 3-phase (3P3L) techniques are applied to reduce the current ripple to 1/12th of that of standard 2-level class-D amplifier. At the same time, the effective switching frequency increases by 6 times. Compared to the previous works which use several u*H* inductors, this paper only uses 200n*H* inductors with comparable efficiency, showing 30% increase in the proposed figure-of-merit (FOM).

C11-3 - 11:20
A 1V 0.25uW Inverter-Stacking Amplifier with 1.07 Noise Efficiency Factor, L. Shen, N. Lu and N. Sun, The Univ. of Texas at Austin, USA

This paper presents a highly power efficient amplifier. By stacking inverters and splitting the capacitor feedback network, the proposed amplifier achieves 6-time current reuse, thereby significantly boosting g_m and lowering noise but without increasing power. A novel biasing scheme is devised to ensure robust operation under 1V supply. A prototype in 180nm CMOS has 5.5uV rms noise within 10kHz BW while consuming only 0.25uW, leading to a noise efficiency factor (NEF) of 1.07, which is the best among reported amplifiers.

C11-4 - 11:45
A 150-μW 3rd-Order Butterworth Passive-Switched-Capacitor Filter with 92 dB SFDR, S. Z. Lulec, D. A. Johns and A. Liscidini, Univ. of Toronto, Canada

For the first time, complex conjugate poles are integrated on silicon by using only switches and capacitors. A general design methodology is proposed to implement low-pass transfer functions with sharper frequency profile compared to the passive-switched-capacitor topologies present in the literature. Theory and simulation results are validated through the measurements of a 0.13μm prototype filter. The 3rd-order filter has a cut-off frequency of 540 kHz, an integrated input referred noise of 17μV and out-of-band IIP3 of 55dBm, while consuming 150μW in the waveform generator.

C11-5 - 12:10
A 0.8V, 37nW, 42ppm/°C Sub-Bandgap Voltage Reference with PSRR of -81dB and Line Sensitivity of 51ppm/V in 0.18um CMOS, M. Kim and S. Cho, KAIST, Korea

This paper presents a low-power, high-PSRR sub-bandgap voltage reference that operates under 1V supply. In order to achieve low temperature coefficient (TC), a CTAT circuit with internal feedback and a two-transistor PTAT circuit are proposed. For improved line sensitivity (LS) and PSRR, a self supply-regulated feedback is employed. Implemented in 0.18μm CMOS, the proposed voltage reference achieves an average TC of 42ppm/°C, PSRR of -81dB and LS of 51ppm/V while consuming 37nW at 0.8V supply.

Technology / Circuits Joint Focus Session 2

Advanced Assembly [Suzaku III]

Wednesday, June 7, 14:00-15:40

Chairpersons: N. Miura, Kobe Univ.
B. Calhoun, Univ. of Virginia

JFS2-1 - 14:00
A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Solenoid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS, H. K. Krishnamurthy, S. Weng, G. E. Matthew, R. Saraswat, K. Ravichandran, J. Tschanz and V. De, Intel Corp., USA

A fully integrated digitally controlled buck VR, featuring hysteretic and PFM control for maximum light load efficiency, with 3D-TSV based on-die solenoid inductor with backside planar magnetic core in 14nm tri-gate CMOS demonstrates 111 nH/mm² inductance density & 80% conversion efficiency.

JFS2-2 - 14:25
A 6Gb/s Rotatable Non-Contact Connector with High-Speed/I²C/CAN/SPI Interface Bridge IC, M. Haraguchi*, A. Kosuge*, T. Igarashi**, S. Masaki**, M. Sueda**, M. Hamada* and T. Kuroda*, *Keio Univ. and **Socionext Inc., Japan

A 6Gb/s 9.8pJ/b rotatable non-contact connector applicable to robot arms is developed. The proposed rotatable transmission line coupler (RTLC) has a wide bandwidth at all rotation angles. An interface bridge IC is also developed to transfer a wide range of interface signals from slow legacy ones to high-speed ones. The proposed system improves power efficiency by a factor of 3.7, space efficiency by a factor of 1.8, and satisfies EMC regulations.

JFS2-3 - 14:50
High Density 3D Fanout Package for Heterogeneous Integration, S.-P. Jeng, S. M. Chen, F. C. Hsu, P. Y. Lin, J. H. Wang, T. J. Fang, P. Kavle and Y. J. Lin, TSMC, Taiwan

Three-dimensional (3D) fanout package stacking offers new levels of performance, high-density integration, and form factor advantages. Known-good fanout packages are stacked, and the vertical connection is built through Cu pillars in the molding area and solder bumps. Compared to existing TSV-based 3D integrated circuits (3DIC) technology, this solution reduces thermal crosstalk when integrating devices of different die sizes. Fanout package stacking potentially provides a cost-effective platform for highly flexible heterogeneous integration of digital, memory, analog, radio-frequency (RF) and optical devices.

JFS2-4 - 15:15
A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications, S. Park*, T. Cho*, M. Kim*, H. Park** and K. Lee*, *KAIST and **Seoul National Univ. of Science and Technology, Korea

A micro-bolometer focal plane array (MBFPA)-based long wavelength Infra-red thermal imaging sensor is presented. The proposed multiple digital correlated double sampling (MD-CDS) readout method employing newly designed reference-cell greatly reduces PVT variation-induced fixed pattern noise (FPN) and as a result features much relaxed calibration process, easier TEC-less operation and Shutter-less operation. The readout IC and MBFPA was fabricated in 0.35um CMOS and amorphous silicon MEMS process respectively. The fabricated MBFPA thermal imaging sensor has NETD performance of 0.1 kelvin even though the mechanical shutter is not used.

SESSION 12

SRAM & Emerging Memory [Suzaku II]

Wednesday, June 7, 14:00-15:40

Chairpersons: H. Noda, Micron Memory Japan, Inc.
V. Agrawal, Cypress Semiconductor Corp.

C12-1 - 14:00
A 31.2pJ/disparity·pixel Stereo Matching Processor with Stereo SRAM for Mobile UI Application, J. Lee, D. Shin, K. Lee and H.-J. Yoo, KAIST, Korea

An energy-efficient and high-speed stereo matching processor is proposed for smart mobile devices with proposed stereo SRAM (S-SRAM) and independent regional integral cost (IRIC). Cost generation unit (CGU) with the proposed S-SRAM reduces 63.2% of CGU power consumption. The proposed IRIC enables cost aggregation unit (CAU) to obtain 6.4× of speed and 12.3% of the power reduction of CAU with pipelined integral cost generator (PICG). The proposed stereo matching processor, implemented in 65nm CMOS process, achieves 82fps and 31.2pJ/disparity·pixel energy efficiency at 30fps. Its energy efficiency is improved by 77.6% compared to the state-of-the-art.

C12-2 - 14:25
A 0.3V VDDmin 4+2T SRAM for Searching and In-Memory Computing Using 55nm DDC Technology, Q. Dong*, S. Jeloka*, M. Saligane*, Y. Kim*, M. Kawaminami**, A. Harada**, S. Miyoshi**, D. Blaauw* and D. Sylvester*, *Univ. of Michigan and **Fujitsu Semiconductor America, Inc., USA

A 4+2T SRAM is proposed that offers searching and logic functions. The cell uses the N-well as the write wordline and eliminates the access transistors. Decoupled read paths enable reliable multi-word activation for in-memory Boolean logic functions. The SRAM can reconfigure to BCAM/TCAM for searching operations, with 0.13fJ/search/bit at 0.35V. Forty test chips in 55nm deeply depleted channel technology achieve worst-case 0.3V VDDmin.

C12-3 - 14:50
A 140 MHz 1 Mbit 2T1C Gain-Cell Memory with 60-nm Indium–Gallium–Zinc Oxide Transistor Embedded Into 65-nm CMOS Logic Process Technology, T. Ishizu*, S. Nagatsuka*, M. Yamaguchi*, A. Isobe*, Y. Ando*, D. Matsubayashi*, K. Kato*, H. B. Yao**, C. C. Shuai**, H. C. Lin**, J. Y. Wu**, M. Fujita*** and S. Yamazaki*, *Semiconductor Energy Laboratory Co., Ltd., Japan, **United Microelectronics Corp., Taiwan and ***The Univ. of Tokyo, Japan

An embedded 1 Mbit 2T1C gain-cell memory macro using indium-gallium-zinc oxide semiconductor FETs (OSFETs) with an extremely low off-state current of less than 1 zA (10^{-21} A) was fabricated. In the 2T1C gain cell, an OSFET for the write operation was stacked over a SiFET for the read operation. The 1 Mbit macro was fabricated using a combination of 60-nm OSFET and 65-nm CMOS processes. It achieves a 140 MHz operation and data retention of more than 1 h. Its static power in the standby state and active power are 31 µW and 64 µW/MHz, respectively. The macro with long-term data retention can reduce the static power by power gating. 2T1C OSFET-based embedded memory is applicable to devices requiring high performance as well as low power.

C12-4 - 15:15
Embedded 2Mb ReRAM Macro with 2.6ns Read Access Time Using Dynamic-Trip-Point-Mismatch Sampling Current-Mode Sense Amplifier for IoE Applications, C.-P. Lo*·**, W.-Z. Lin*·**, W.-Y. Lin*, H.-T. Lin*, T.-H. Yang**, Y.-N. Chiang*, Y.-C. King*, C.-J. Lin*, Y.-D. Chih**, T.-Y. J. Chang**, M.-S. Ho*** and M.-F. Chang*, *National Tsing Hua Univ., **TSMC and ***National Chung Hsing Univ., Taiwan

Recent embedded ReRAM has a small resistance-ratio (R-ratio), which results in a small read sensing margin (I_{SM}). A larger BL current (I_{BL}) increases the input offset (I_{OS}) of current-mode sense amplifiers (CSA), resulting in low-yield read operations and long read access times (T_{CD}). This work proposes an I_{BL}-aware small-I_{OS} CSA, using a dynamic trip-point-mismatch sampling (DTPMS) scheme to increase tolerance for small I_{SM} and residual BL precharge current (I_{PRE}) in order to improve memory yield and speed up T_{CD} in cases of small R-ratio. A fabricated 65nm 2Mb ReRAM macro achieved T_{CD}=2.6ns at VDD=1V. For the first-time, a ReRAM macro with sub-3ns T_{CD} is presented.

SESSION 13

Biosignal Recording / Monitoring Circuits [Suzaku I]

Wednesday, June 7, 14:00-15:40

Chairpersons: Y. P. Xu, National Univ. of Singapore
D. Markovic, Univ. of California, Los Angeles

C13-1 - 14:00
3.37 µW/Ch Modular Scalable Neural Recording System with Embedded Lossless Compression for Dynamic Power Reduction, S.-Y. Park, J. Cho and E. Yoon, Univ. of Michigan, USA

We report a neural recording system with embedded lossless compression using spatiotemporal correlation and sparsity of neural signals to reduce dynamic power (P_D) dissipation for data transmission in high-density neural recording systems. We could successfully compress the data rate of neural signals by a factor of 5.35 (local field potential, LFP) and 10.54 (action potential, AP), respectively. Consequently we reduced P_D consumption by 89% while achieving the state-of-the-art recording performance of 3.37 µW/Ch, 5.18 µV$_{rms}$ input-referred noise, and 3.41NEF^{2}V$_{DD}$.

C13-2 - 14:25
A 36μW Reconfigurable Analog Front-End IC for Multimodal Vital Signs Monitoring, J. Xu*, M. Konijnenburg*, H. Ha*, R. van Wegberg*, B. Lukita*, S. Z. Asl*, C. V. Hoof*,**,*** and N. V. Helleputte**, *imec/Holst Centre, The Netherlands, **imec and ***KU Leuven, Belgium

This paper presents a highly reconfigurable analog front-end (AFE) IC supporting multimodal (bio)signal monitoring. By efficiently reusing core components, the reconfigurable AFE channel occupies an area of 1.1mm^2 while supporting four acquisition modes, i.e. biopotential (ExG), bio-impedance (BioZ), galvanic skin response (GSR) and general purpose analog (GPA). State-of-the-art sensitivity has been achieved at low power by employing both chopping and dynamic element matching (DEM). The reconfigurable AFE channel consumes 36μW maximum from a 1.2V supply.

C13-3 - 14:50
A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression, W. A. Smith, J. P. Uehlin, S. I. Perlmutter, J. C. Rudell and V. S. Sathe, Univ. of Washington, USA

We present a scalable, highly multiplexed CMOS electro-cortocography (ECoG) recording front-end capable of differential-mode and common-mode artifact suppression. The front-end digitally delta-encodes 8-bit data converters to achieve 14-bit resolution. A single, shared mixed-signal front-end is time-division multiplexed to 64 differential input channels; this reduces channel area by 10x compared to the state-of-the-art. A return-to-zero scheme effectively eliminates channel crosstalk. We present performance and in-vivo measurement results of a 65nm CMOS test-chip implementation of the proposed architecture.

C13-4 - 15:15
A Bio-Impedance Readout IC with Frequency Sweeping from 1k-to-1MHz for Electrical Impedance Tomography, H. Ha*, M. Konijnenburg*, B. Lukita*, R. van Wegberg*, J. Xu*, R. van den Hoven*, M. Lemmens**, R. Thoelen**,***, C. V. Hoof***,**** and N. V. Helleputte***, *imec/Holst Centre, The Netherlands, **Hasselt Univ., ***imec and ****KU Leuven, Belgium

This paper presents a bio-impedance (BIOZ) readout IC for electrical impedance tomography (EIT). The IC includes a complete readout channel for impedance characterization at various frequencies ranging from 1k-to-1MHz, an input multiplexer and a programmable digital controller enabling multi-frequency impedance scanning from multiple locations. To relax the bandwidth requirements of the readout channel, pre-demodulation before the IA is employed. A fast channel settling mechanism (<1ms) allows quick switching between frequencies enabling a fast imaging speed. Dynamic element matching (DEM) in the current generation and chopping in the readout front-end are adopted to mitigate 1/f noise resulting in a noise floor of 38.4mΩ$_{RMS}$. This IC, fabricated in 0.18μm, consumes 18.7μW and 63μW in the readout front-end and the current generator (CG), respectively. By means of *in-vitro* and *in-vivo* testing its effectivity for EIT is demonstrated.

SESSION 14

Phase-Locked Loops [Suzaku III]

Wednesday, June 7, 16:00-18:05

Chairpersons: H. Shin, Kwangwoon Univ.
                E. Janssen, NXP Semiconductors

C14-1 - 16:00
A 0.5V 1.6mW 2.4GHz Fractional-N All-Digital PLL for Bluetooth LE with PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28nm CMOS, F.-W. Kuo*, S. Pourmousavian**, T. Siriburanon**, R. Chen*, L.-C. Cho*, C.-P. Jou*, F.-L. Hsueh* and R. B. Staszewski**, *TSMC, Taiwan and **Univ. College Dublin, Ireland

This paper proposes an ultra-low-voltage (ULV) fractional-N all- digital PLL (ADPLL) powered from a single 0.5 V supply. While its DCO runs directly at 0.5 V, a switched-capacitor DC-DC converter doubles the supply voltage to all the digital circuitry and regulates the TDC supply to stabilize its resolution thus maintaining fixed in- band phase noise (PN) across PVT. The ADPLL supports a 2-point modulation and forms a Bluetooth LE (BLE) transmitter realized in 28 nm CMOS. It achieves in-band PN of –106 dBc/Hz (FoM of –239.2 dB) and RMS jitter of 0.86 ps while dissipating only 1.6 mW at 40MHz reference. The power consumption reduces to 0.8mW during BLE transmission when the DCO switches to open-loop.

C14-2 - 16:25
A Supply Noise Insensitive PLL with a Rail-To-Rail Swing Ring Oscillator and a Wideband Noise Suppression Loop, D. Kim and S. Cho, KAIST, Korea

This paper presents a supply noise insensitive digital phase-locked loop (PLL) using a wide bandwidth noise suppression loop (NSL). Unlike previous techniques using regulation or calibration on the voltage-controlled oscillator (VCO) that lead to voltage headroom reduction, the proposed approach employs a wide bandwidth feedback loop around the oscillator, which suppresses supply noise without any headroom loss. The proposed dual loop PLL is implemented in 65nm CMOS, achieving spur suppression of about 30dB near PLL loop bandwidth, while consuming 2.73mW at 3.2GHz output.

C14-3 - 16:50
A 164fs$_{rms}$ 9-to-18GHz Sampling Phase Detector Based PLL with In-Band Noise Suppression and Robust Frequency Acquisition in 16nm FinFET, M. Raj, A. Bekele, D. Turker, P. Upadhyaya, Y. Frans and K. Chang, Xilinx Inc., USA

A sampling phase detector (SPD) based PLL is presented. The high gain of this programmable SPD suppresses PLL's in-band noise and controls its bandwidth. Instead of sampling the VCO output directly like sub-sampling PLLs, the output of the frequency divider is sampled. This improves capture range and eases high frequency design while maintaining in-band noise reduction. The design uses a single charge pump based frequency acquisition technique with programmability for robust operation. The PLL is realized in a 16nm FinFET process. The SPD improves the measured in-band phase noise from -90.6dBc/Hz to -104.1dBc/Hz at 18GHz with RMS jitter of 164fs when integrated over 10KHz-100MHz, while consuming 29.2mW. 2X frequency range of 9-to-18GHz is demonstrated using two LC VCOs.

C14-4 - 17:15
Computational Locking: Accelerating Lock-Times in All-Digital PLLs, F. U. Rahman*, G. F. Taylor** and V. S. Sathe*, *Univ. of Washington and **Intel Corp., USA

We propose computational-lock (C-Lock), a technique for achieving rapid phase-acquisition in ADPLLs during cold-start and re-lock. A wide-dynamic range, high resolution TDC is also proposed to further support C-Lock. Lock-time (Tlock) performance is evaluated through 50,000 measure-ments of C-Lock enabled ADPLL test-chips in 65nm CMOS. Mean Tlock values of 16 T_{refclk} and 12 T_{refclk} for cold-start and re-lock respectively are reported. Used only during cold-start or re-lock, C-Lock does not impact steady-state PLL power and performance.

C14-5 - 17:40
A −242-dB FOM and −71-dBc Reference Spur Ring-VCO-Based Ultra-Low-Jitter Switched-Loop-Filter PLL Using a Fast Phase-Error Correction Technique, T. Seong, Y. Lee, S. Yoo and J. Choi, UNIST, Korea

This work presents an ultra-low jitter, low-reference spur switched-loop-filter (SLF) PLL that uses a fast phase-error correction (FPEC) technique that emulates the phase-realignment mechanism of an injection-locked clock multiplier (ILCM). Despite a high multiplication factor (i.e., 64), the proposed SLFPLL concurrently achieved ultra-low jitter and low reference spur. From the prototype that was fabricated using a 65-nm CMOS process, the RMS-jitter, the FOM, and the reference spur were measured as 378 fs, –242 dB, and –71 dBc, respectively.

SESSION 15

Memory Interface and Flash Memory [Suzaku II]

Wednesday, June 7, 16:00-18:05

Chairpersons: K. Sohn, Samsung Electronics Co., Ltd.
                J. T. Pawlowski, Micron Technology, Inc.

C15-1 - 16:00
A Floating Tap Termination Scheme with Inverted DBI AC and Floating Tap Forcing Technique for High-Speed Low-Power Signaling, H.-K. Jung, H.-J. Song, H.-W. Song, D.-W. Jang, K. Song, W. Kim, K.-H. Kim, D.-H. Kwon, J. Cho and J.-H. Oh, SK hynix, Inc., Korea

This paper presents a novel floating tap termination (FTT) scheme with inverted data bus inversion (iDBI_AC) and floating tap forcing (FTF) to remove the DC current path, leading to reduction of static current. The iDBI_AC and FTF are proposed to resolve common-mode stabilization issues for the floating tap termination scheme during transmitting unbalanced data patterns. Power efficiency with the proposed scheme using 0.6V I/O supply and a 0.13-um technology is measured as 0.127mW/Gbps/pin, which is 61% lower than that of a low tap termination (LTT) scheme used in LPDDR4X. In addition to the power benefit, measurement results present that the proposed scheme leads to achieve 7Gbps data-rate without penalty of signal integrity issues and the iDBI_AC minimizes inter-symbol interference (ISI).

C15-2 - 16:25
A Resistor-Free 4.266 Gbps LPDDR4 I/O in 10 nm FinFET CMOS Technology, T.-C. Lu, M.-H. Hsieh, T.-C. Huang, C.-M. Fu, C.-H. Chang and K. Hsieh, TSMC, Taiwan

This paper presents a 4.266 Gbps LPDDR4 I/O with resistor-free on-die termination (ODT). The resistor-free ODT utilizes resistor-free driving unit (RFDU) with adaptive bias unit (ABU). The ABU adopts source-follower based structure which provides an adaptive bias voltage to compensate the saturated ID current caused non-linearity. The proposed LPDDR4 I/O is fabricated in 10 nm FinFET technology with the post-driver area of $0.0025mm^2$. The measurement result shows that the calibrated ODT resistances among 63 dies all meet LPDDR4 specifications. Furthermore, the eye opening of 0.73 UI is achieved with 4.266 Gbps PRBS pattern.

C15-3 - 16:50
A 1.2V 1.33Gb/s/pin 8Tb NAND Flash Memory Multi-Chip Package Employing F-Chip for Low Power and High Performance Storage Applications, H.-J. Kim, Y. Choi, J. Lee, J. Byun, S. Yu, D. Na, J. Park, K. Kim, A. Kavala, Y. Jo, C. Kim, S. Kim, N. Kim, J. Kim, B. Jung, Y. Lee, C. Park, H. Joo, K. Kim, Y. Choi, P. Kwak, H. Kim, J.-D. Ihm, D.-S. Byeon, J.-Y. Lee, K.-T. Park and K.-H. Kyung, Samsung Electronics Co., Ltd., Korea

A 1.2V 1.33Gb/s/pin 8Tb NAND flash memory multi-chip package incorporating 16-die stacked 512-Gb NAND flash memory and F-Chip is presented. To meet the performance requirements of storage devices for higher capacity and faster data throughput, the 2nd generation F-Chip is developed. The F-Chip presents a dual bi-directional transceiver architecture including data retiming and training techniques to adaptively improve signal integrity. Besides, the F-Chip supports 1.2V I/O for low power storage applications. This work, as a result, shows 33% improvement of eye-opening performances and 41% reduction of I/O power consumption compared to the previous generation.

C15-4 - 17:15
An Ultra-Wide Program, 122pJ/Bit Flash Memory Using Charge Recycling, S. Jeloka, J. Lee, Z. Li, J. Shah, Q. Dong, K. Yang, D. Sylvester and D. Blaauw, Univ. of Michigan, USA

Embedded flash for low power sensing systems require very low write energy and peak power. This work proposes a 130nm, 1024x260 SONOS flash with an ultra-wide 1Kb program cycle, using efficient FN tunneling based programing and a dedicated, multi-output transition pump with charge sharing and charge recycling. Combined with energy efficient charge pumps, the proposed flash program energy is 122pJ/bit with a 1Mbps throughput.

C15-5 - 17:40
A 40nm Split Gate Embedded Flash Macro with Flexible 2-in-1 Architecture, Code Memory with 140MHz Read Speed and Data Memory with 1M Cycles Endurance, H.-C. Yu, K.-F. Lin, Y.-D. Chih and J. Chang, TSMC, Taiwan

This paper presents a 40nm 9.5Mb embedded flash (eflash) macro which can be partitioned as code storage and data storage in a single macro with enhanced read margin by using two design schemes: temperature adaptive reference scheme and flexible array partitioned scheme. By way of these design features, code storage memory achieves 140MHz read speed at the junction temperature of 160°C and data storage memory achieves 1M cycles endurance.

SESSION 16

Power Management Circuit [Suzaku I]

Wednesday, June 7, 16:00-18:05

Chairpersons: M. Takamiya, The Univ. of Tokyo
Y. Ramadass, Texas Instruments

C16-1 - 16:00
A 1452-% Power Extraction Improvement Energy Harvesting Circuit with Simultaneous Energy Extraction from a Piezoelectric Transducer and A Thermoelectric Generator, K.-S. Yoon*, S.-W. Hong**, J.-S. Bang*, S.-H. Lee*, S.-W. Choi* and G.-H. Cho*, *KAIST and **Samsung Electronics Co., Ltd., Korea

This paper presents a dual-source energy harvesting circuit that efficiently and simultaneously extracts the energy from a piezoelectric transducer (PZT) and a thermoelectric generator (TEG). The harvester operates in a dual-source pile-up mode (DPM) to efficiently extract the energy from both sources with an increment of the damping force, resulting in a 1452% improvement of power extraction even without a TEG, which is the best among the-state-of-the-art works. Also, the harvester operates in a boost converter mode (BCM) without an additional power switch, achieving 75 % conversion efficiency at 450 µW output power. With a single-shared inductor, a simple control scheme enables the harvester to operate in both DPM and BCM by a time-multiplexing method, consuming low quiescent current of 240 nA.

C16-2 - 16:25
A 20nW-to-140mW Input Power Range, 94% Peak Efficiency Energy-Harvesting Battery Charger with Frequency-Sweeping Input Voltage Monitor and Optimal On-Time Generator, S.-Y. Jung, M. Lee, J. Yang and J. Kim, Seoul National Univ., Korea

This paper presents a boost-type energy-harvesting battery charger IC that can maintain high efficiencies over a wide range of input power. In other words, the IC has a fast response to achieve 94% peak efficiency at high input power conditions, yet dissipates only 14.7nW quiescent power to achieve a net positive charging at low input power conditions. The key to this fast, low-power operation is the use of frequency-sweeping input voltage monitor, i.e., a clocked comparator of which sampling clock frequency is exponentially swept from 800-kHz to 100-Hz. In addition, an optimal on-time pulse generator improves the power efficiency by scaling the switching pulse-width proportional to the battery-to-input voltage ratio. The prototype IC fabricated in 0.25-µm CMOS can charge a 3.0V battery from the input source ranging 0.3-2V and 20nW-140mW, which is the widest input power range reported to date.

C16-3 - 16:50
A 42nJ/Conversion On-Demand State-of-Charge Indicator for Miniature IoT Li-Ion Batteries, J. Jeong*,**, S. Jeong**, C. Kim*, D. Sylvester** and D. Blaauw**, *Korea Univ., Korea and **Univ. of Michigan, USA

An energy efficient State-of-Charge (SOC) indication algorithm and integrated system for small IoT batteries are introduced in this paper. The system is implemented in a 180-nm CMOS technology. Based on a key finding that small Li-ion batteries exhibit a linear dependence between battery voltage and load current, we propose an instantaneous linear extrapolation (ILE) algorithm and circuit allowing on-demand estimation of SOC. Power consumption is 42nW and maximum SOC indication error is 1.7%.

C16-4 - 17:15
A 0.3-0.86V Fully Integrated Buck Regulator with 2GHz Resonant Switching for Ultra-Low Power Applications, T. Jia and J. Gu, Northwestern Univ., USA

A fully integrated buck regulator for ultra-low voltage application is presented featuring (1) an ultra-high switching frequency at 2GHz with small inductor size at low load current and (2) a resonant switching technique rendering significant efficiency improvement. With small on-chip inductors, the test chip shows a wide voltage tuning range of 0.3-0.86V, at 10-40mA low current, up to 73% efficiency and only occupies 0.073mm^2 in a 65nm CMOS process.

C16-5 - 17:40
A True Two-Quadrant Fully Integrated Switched Capacitor DC-DC Converter Supporting Vertically Stacked DVS-Loads with up to 99.6% Efficiency, A. Sarafianos and M. Steyaert, KU Leuven, Belgium

This paper presents a Switched Capacitor DC-DC converter capable of powering two vertically stacked loads, unlocking efficiencies of up to 99.6% when loads consume identical current. Furthermore, this converter is the first to provide up to 100% current imbalance thanks to its true two-quadrant operation, allowing loads to completely turn off. The system has been fabricated in a 65nm GP process followed by validation through measurements of its high efficiencies (>90% when δI<0.4) and control loop operation.

Technology / Circuits Joint Banquet [Shunju I, II, III]

Wednesday, June 7, 19:00-21:00

Technology / Circuits Joint Focus Session 3

Ultra Low Power for IoT [Shunju II, III]

Thursday, June 8, 8:30-10:10

Chairpersons:　M. Tada, NEC Corp.
　　　　　　　　L. Bair, AMD

JFS3-1 - 8:30 (Invited)
Computing Platform for Automotive Electronics of Automated Driving Generation, H. Sugimoto, DENSO Corp., Japan

This paper addresses requirements from future automotive electronics system concept/design to computing technology or platform filling processing characteristics which will be used in applications of automated driving generation. We cannot completely predict future trends of functionality or application, so it is important to have flexible and scalable computing platform for that generation. The platform should also have a reasonable coverage of processing characteristics especially for parallelism point of view, because it will strongly affect to automotive electronics system efficiency and quality. Here, we'll mainly point to automotive unique processing characteristics which should be improved in near future.

JFS3-2 - 8:55 (Invited)
Semiconductor Platforms for Ultra Low Power IoT Solutions, T. Dry and T. Letavic, GLOBALFOUNDRIES, USA

Intelligent connected sensor and actuator endpoint nodes enable the Internet-of-Things (IoT).   A brief overview of endpoint node functional blocks and requirements for low-power consumption are discussed. VLSI technology enablers for IoT include Ultra low Power (ULP) and Ultra Low Leakage (ULL) semiconductor process platform extensions. ULP and ULL implementations for bulk silicon technologies are presented and compared to fully-depleted silicon-on-insulator (FDSOI) technology. FDSOI utilizes Back Bias (BB) to improve performance and achieve the lowest dynamic and static power, enabling cost-effective low-power IoT applications.

JFS3-3 - 9:20
Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application, S. H. Wu*, X. Y. Jia*, X. Li*, C. C. Shuai*, H. C. Lin*, M. C. Lu*, T. H. Wu*, M. Y. Liu*, J. Y. Wu*, D. Matsubayashi**, K. Kato** and S. Yamazaki**, *United Microelectronics Corporation, Singapore and **Semiconductor Energy Laboratory Co., Ltd., Japan

The worldwide first 100MHz dynamic oxide semiconductor RAM (DOSRAM) is successfully demonstrated using a new high-mobility crystalline In-Ga-Zn-O (IGZO) material. The new IGZO exhibits around two times carrier mobility of conventional IGZO, while still achieving an extremely low off-state leakage (I_{off}) at ~10^{-21}A (zA) level. Attributed to DOSRAM performance improvement, 100MHz normally-off (Noff) CPU is successfully demonstrated with drastically reduced power consumption (~94% power reduction for ARM Cortex-M0 and ~70% power reduction for memory), making it a promising candidate for IoT application. In addition, an OS-FPGA is successfully fabricated by integration of 65nm SiFET and 60nm oxide semiconductor FET (OSFET) with an operation frequency of 360MHz. The application of the OSFET in analog circuits will also be discussed in this paper.

JFS3-4 - 9:45
A 65 nm 1.0 V 1.84 ns Silicon-On-Thin-Box (SOTB) Embedded SRAM with 13.72 nW/Mbit Standby Power for Smart IoT, M. Yabuuchi*, K. Nii*, S. Tanaka*, Y. Shinozaki**, Y. Yamamoto*, T. Hasegawa*, H. Shinkawata* and S. Kamohara*, *Renesas Electronics Corp. and **Nippon Systemware Co. Ltd., Japan

A 65-nm Silicon-on-Thin-Box (SOTB) embedded SRAM is demonstrated. By using back-bias (BB) control in the sleep mode, 13.72 nW/Mbit ultra-low standby power is observed, which is reduced to 1/1000 compared to the normal standby mode. The measured read access time with forward BB is 1.84 ns at 1.0 V overdrive and 25°C, which is improved by 60% and thus we achieved over 380 MHz operation. Up to 20% active read power reduction is also achieved by using proposed localized adoptive wordline width control.

SESSION 17

Video Processing [Suzaku III]

Thursday, June 8, 8:30-10:10

Chairpersons:　J. Chang, TSMC
　　　　　　　　S. Dillen, Qualcomm Technologies, Inc.

C17-1 - 8:30 (Invited)
System Architecture with Single Chip 8K HEVC Decoder for 8K Advanced BS Receiver System, M. Nakajima, D. Murakami, H. Kubo, T. Baba and Y. Miki, Socionext Inc., Japan

To implement 8K Advanced BS receiver system, 8K HEVC decoder SoC is developed as key component. To solve the exceeded required memory bandwidth over physical memory bandwidth limitation issue for realizing 8K decoder, two types of multi-cast write back scheme, including reference data multi-cast write back and output data multi-cast write back, are introduced. 8K HEVC decoder chip is fabricated in 28nm CMOS technology and SIP packaged with eight DDR3 memories.

C17-2 - 8:55
A 127mW 1.63TOPS Sparse Spatio-Temporal Cognitive SoC for Action Classification and Motion Tracking in Videos,
C.-E. Lee, T. Chen and Z. Zhang, Univ. of Michigan, USA

A sparse spatio-temporal (ST) cognitive SoC is designed to extract ST features from videos for action classification and motion tracking. The SoC core is a sparse ST convolutional auto-encoder that implements recurrence using a 3-layer network. High sparsity is enforced in each layer of processing, reducing the complexity of ST convolution by two orders of magnitude and allowing all multiply-accumulates (MAC) to be replaced by select-adds (SA). The design is demonstrated in a 3.98mm^2 40nm CMOS SoC with an OpenRISC processor providing software-defined control and classification. ST kernel compression is applied to reduce memory by 43%. At 0.9V and 240MHz, the SoC achieves 1.63TOPS to meet the 60fps 1920×1080 HD video data rate, dissipating 127mW.

C17-3 - 9:20
A Single-Chip 2048×1080 Resolution 32fps 380mW Trinocular Disparity Estimation Processor in 28nm CMOS Technology, J. Narinx, T. Demirci, A. Akin and Y. Leblebici, EPFL, Switzerland

This paper presents a single-chip trinocular disparity estimation processor, capable of computing in real-time up to 2048×1080 resolution depth maps at 32fps with up to 256-pixel disparity range using two/three CMOS camera sensors. The most important feature of the presented design is that the chip is based on a trinocular adaptive window matching process that requires very limited on-chip memory, and completely avoids the usage of any external memory. Moreover, it provides the highest reported disparity range capability at the lowest power consumption and highest frame rate, while computing high-quality disparity results. It features a stream-in/out interface to be easily integrated in existing vision systems, without additional overhead, and offers a dynamically scalable tradeoff between throughput, resolution and disparity range. The single-chip is fabricated in 28nm CMOS technology, has a die area of 5.96mm^2 and a power consumption of 380mW at 300MHz clock frequency.

C17-4 - 9:45
A Fully-Integrated Energy-Efficient H.265/HEVC Decoder with eDRAM for Wearable Devices, M. Tikekar, V. Sze and A. Chandrakasan, Massachusetts Institute of Technology, USA

Data movement to and from off-chip memory dominates energy consumption in most video decoders, with DRAM accesses consuming 2.8x-6x more energy than the processing itself. We present a H.265/HEVC video decoder with embedded DRAM (eDRAM) as main memory. We propose the following techniques to optimize data movement and reduce the power consumption of eDRAM: 1) lossless compression is used to store reference frames in 2x fewer eDRAM banks, reducing refresh power by 33%; 2) eDRAM banks are powered up on-demand to further reduce refresh power by 33%; 3) syntax elements are distributed to four decoder cores in a partially compressed form to reduce decoupling buffer power by 4x. These approaches reduce eDRAM power by 2x in a fully-integrated H.265/HEVC decoder with the lowest reported system power. The decoder chip requires no external components and consumes 24.9 – 30.6mW for 1920x1080 video at 24 – 50 fps.

SESSION 18

SAR ADCs [Suzaku II]

Thursday, June 8, 8:30-10:10

Chairpersons: K. Okada, Tokyo Institute of Technology
E. Naviasky, Cadence Design Systems, Inc.

C18-1 - 8:30
A 2.4-mW 25-MHz BW 300-MS/s Passive Noise Shaping SAR ADC with Noise Quantizer Technique in 14-nm CMOS, Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, R.-X. Chu and C.-H. Lu, MediaTek Inc., Taiwan

This paper presents a SAR ADC using passive noise shaping and a noise quantizer technique. A ping-pong residue switching enables noise shaping at high sampling rate. The prototype in 14 nm achieves 69-dB SNDR at 25-MHz BW and 300 MS/s. The Schreier FOM and Walden FOM are 169 dB and 20.5 fJ/conversion-step, respectively. With noise shaping only, the SNDR is 66.2 dB at 33-MHz BW and 400 MS/s.

C18-2 - 8:55
A 13b-ENOB 173dB-FoM 2nd -Order NS SAR ADC with Passive Integrators, W. Guo, H. Zhuang and N. Sun, The Univ. of Texas at Austin, USA

This paper presents a low-power 2nd-order noise-shaping (NS) SAR ADC. Instead of using power-hungry op-amps, it uses switches and capacitors to make passive integrators for noise shaping. The overall architecture is simple and the NS order can be easily reconfigured from 0 to 2. A prototype chip is fabricated in a 40nm CMOS process. With 2nd-order NS, the chip consumes 143μW power at 1.1V and 8.4MS/s. At an OSR of 16, SNDR is 80dB and the Schreier FoM is 173dB.

C18-3 - 9:20
A 510nW 12-bit 200kS/s SAR-Assisted SAR ADC Using a Re-Switching Technique, Y.-S. Hu, K.-Y. Lin and H.-S. Chen, National Taiwan Univ., Taiwan

This paper presents a 510nW 12-bit 200kS/s SAR-assisted SAR ADC in 40nm CMOS at 0.7V supply. A re-switching technique is proposed to suppress DNL spikes so that the size of DAC capacitor array can be minimized to reduce switching energy. A set of 2-way charge pump is used to decrease settling time constant and to increase sampling linearity. The prototype ADC achieves the DNL/INL performance of 0.5/0.79 LSB. Its SNDR and SFDR at Nyquist rate are 69.1dB and 81.72dB, respectively. It results in an FoM$_s$ of 182dB and an FoM$_w$ of 1.1fJ/c.-s.

C18-4 - 9:45
A 107 dB SFDR, 80 kS/s Nyquist-Rate SAR ADC Using a Hybrid Capacitive and Incremental ΣΔ DAC, A. AlMarashli, J. Anders, J. Becker and M. Ortmanns, Univ. of Ulm, Germany

This paper introduces an architecture and design for high resolution, high linearity Nyquist rate SAR ADCs requiring only a single simple calibration at startup. The proposed architecture benefits from an intrinsically linear 1.5bit DAC to resolve the fine bits of the SAR ADC after a coarse conversion phase with a monotonically switched capacitive DAC. The SD-DAC is also used for a single shot calibration of the coarse CDAC which therefore does not require good matching and can be sized solely upon noise requirement. A prototype was fabricated in 40nm CMOS. It occupies an active area of only 0.074mm^2. The prototype achieves a measured peak SFDR of 107dB and a noise limited SNDR of 84.8dB at 80kS/s Nyquist rate operation. The core power consumption is 101µW at 80kS/s. In oversampling mode, the ADC achieves an SNDR above 90dB over a 5kHz bandwidth.

SESSION 19

Image Sensors [Suzaku I]

Thursday, June 8, 8:30-10:10

Chairpersons: H. Wakabayashi, Sony Electronics Inc.
                N. Dutton, STMicroelectronics

C19-1 - 8:30
A 4.1Mpix 280fps Stacked CMOS Image Sensor with Array-Parallel ADC Architecture for Region Control, T. Takahashi*, Y. Kaji**, Y. Tsukuda*, S. Futami*, K. Hanzawa***, T. Yamauchi*, P. W. Wong***, F. Brady***, P. Holden***, T. Ayers***, K. Mizuta*, S. Ohki*, K. Tatani*, T. Nagano*, H. Wakabayashi*** and Y. Nitta*, *Sony Semiconductor Solutions Corp., **Sony LSI Design Inc., Japan and ***Sony Electronics Inc., USA

A 4.1Mpix 280fps stacked CMOS image sensor with array-parallel ADC architecture is developed for region control applications. The combination of an active reset scheme and frame correlated double sampling (CDS) operation cancels Vth variation of pixel amplifier transistors and kTC noise. The sensor utilizes a floating diffusion (FD) based back-illuminated (BI) global shutter (GS) pixel with 4.2e-rms readout noise. An intelligent sensor system with face detection and high resolution region-of-interest (ROI) output is demonstrated with significantly low data bandwidth and low ADC power dissipation by utilizing a flexible area access function.

C19-2 - 8:55
A 256 Energy Bin Spectrum X-Ray Photon-Counting Image Sensor Providing 8Mcounts/s/pixel and On-Chip Charge Sharing, Charge Induction and Pile-Up Corrections, A. Peizerat*, J.-P. Rostaing*, P. Ouvrier-Buffet*, S. Stanchina*, P. Radisson** and E. Marché**, *CEA-LETI and ** Multix, France

To achieve better and faster material discrimination in applications like security inspection, X-Ray image sensors giving a highly resolved energy spectrum per pixel are required. In this paper, a new pixel architecture for spectral imaging is presented, exhibiting a 256 bin spectrum per pixel in a single image duration, up to two orders of magnitude higher than previous works. A prototype circuit, composed of 4x8 pixels of 756µmx800µm and hybridized to a CdTe crystal, was fabricated in a 0.13µm process. Our pixel architecture has been measured at 8 Mcounts/s/pixel while embedding on-chip charge sharing, charge induction and pile-up corrections.

C19-3 - 9:20
A 0.61 E- Noise Global Shutter CMOS Image Sensor with Two-Stage Charge Transfer Pixels, K. Yasutomi, M. W. Seo, M. Kamoto, N. Teranishi and S. Kawahito, Shizuoka Univ., Japan

A low-noise global shutter (GS) CMOS image sensor (CIS) with two-stage charge transfer (2-CT) structure is presented. The low-noise wide dynamic range performance of the proposed pixel has been demonstrated by using column-parallel folding integration (FI)/cyclic ADCs. The GS image sensor with 5.6µm-pitch 1200 x 900 pixels is implemented with a 0.11µm CIS technology. The noise and dynamic range are measured to be 0.61 e$^-_{rms}$ and 81 dB, respectively.

C19-4 - 9:45
224-ke Saturation Signal Global Shutter CMOS Image Sensor with In-Pixel Pinned Storage and Lateral Overflow Integration Capacitor, Y. Sakano*, S. Sakai*, Y. Tashiro*, Y. Kato*, K. Akiyama*, K. Honda*, M. Sato*, M. Sakakibara*, T. Taura*, K. Azami*, T. Hirano*, Y. Oike*, Y. Sogo*, T. Ezaki*, T. Narabu*, T. Hirayama* and S. Sugawa**, *Sony Semiconductor Solutions Corp. and **Tohoku Univ., Japan

The required incorporation of an additional in-pixel retention node for global shutter complementary metal-oxide semiconductor (CMOS) image sensors means that achieving a large saturation signal presents a challenge. This paper reports a 3.875-µm pixel single exposure global shutter CMOS image sensor with an in-pixel pinned storage (PST) and a lateral-overflow integration capacitor (LOFIC), which extends the saturation signal to 224 ke, thereby enabling the saturation signal per unit area to reach 14.9 ke/µm^2. This pixel can assure a large saturation signal by using a LOFIC for accumulation without degrading the image quality under dark and low illuminance conditions owing to the PST.

Technology / Circuits Joint Focus Session 4

Computing Beyond Von Neumann [Shunju II, III]

Thursday, June 8, 10:30-12:10

Chairpersons: M. Kobayashi, The Univ. of Tokyo
M. Vinet, CEA-LETI, MINATEC

JFS4-1 - 10:30 (Invited)
Implementation Challenges for Scalable Neuromorphic Computing, S. Yamamichi, A. Horibe, T. Aoki, K. Hosokawa, T. Hisada and H. Mori, IBM Research, Japan

In the big data era, a new computing system, called Cognitive Computing, that can handle unstructured data, learn and extract the insights is required. A neuromorphic device is a key component for this, and several architectures are reported. Compared to the neuromorphic device with SRAM-based spiking neural network, a cross-bar structure device realizes on-chip leaning, but requires high-density off-chip interconnect, much higher than those for conventional high-end logic devices. Recent progress of solder bumping and 3-dimentional integration technologies are described.

JFS4-2 - 10:55 (Invited)
Distributed Quantum Computing Systems: Technology to Quantum Circuits, R. Van Meter, Keio Univ., Japan

Quantum computers, both solid-state and other, are developing rapidly in the laboratory and commercialization has begun. We discuss their potential applications and the challenges of manufacturing, managing errors, and creating full-scale systems.

JFS4-3 - 11:20
Ultra-Low Power Probabilistic IMT Neurons for Stochastic Sampling Machines, M. Jerry*, A. Parihar**, B. Grisafe*, A. Raychowdhury** and S. Datta*, *Univ. of Notre Dame and **Georgia Institute of Technology, USA

Stochastic sampling machines (SSM) utilize neural sampling from probabilistic spiking neurons to escape local minima and prevent overfitting of training datasets. This enables improved error rates compared to deterministic implementations, and, in turn, enables lower bit precision, decreased chip area, and reduced energy consumption. In this work, we experimentally demonstrate: (i) Insulator-to-Metal Phase Transition (IMT) neurons with record low peak operating power of 11.9µW at V_{DD}=0.7V; (ii) the IMT in vanadium dioxide (VO_2) provides a natural probabilistic hardware substrate for realizing a compact stochastic IMT neuron for SSMs; (iii) implementation of SSM for pattern recognition on MNIST database using experimentally calibrated device modeling. These results are compared to a 22nm CMOS ASIC which shows stochastic IMT neuron based SSMs result in a 4.5x reduction in system power consumption.

JFS4-4 - 11:45
A 462GOPs/J RRAM-Based Nonvolatile Intelligent Processor for Energy Harvesting IoE System Featuring Nonvolatile Logics and Processing-In-Memory, F. Su*, W.-H. Chen**, L. Xia*, C.-P. Lo**, T. Tang*, Z. Wang*, K.-H. Hsu**, M. Cheng*, J.-Y. Li**, Y. Xie***, Y. Wang*, M.-F. Chang**, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **National Tsing Hua Univ., Taiwan and ***Univ. of California, Santa Barbara, USA

An energy-efficient nonvolatile intelligent processor (NIP) is proposed for battery-less energy harvesting system. This NIP employs RRAM-based nonvolatile logics (NVL) with self-write-termination (SWT) scheme and low-power processing-in-memory (PIM) to achieve energy-efficient computing against frequent power-off situations. An NIP test chip was fabricated in 150nm CMOS process using HfO RRAM. This NIP chip achieves 462GOPs/J energy efficiency at 20MHz clock frequency, showing 13× performance improvement over state-of-the-arts. This work presents the first nonvolatile processor capable of general as well as neural network computing in addition to the first integrated chip using RRAM-based PIM.

SESSION 20

Circuits for Security and Low Power [Suzaku III]

Thursday, June 8, 10:30-12:35

Chairpersons: M. Natsui, Tohoku Univ.
E. Beigne, CEA-LETI

C20-1 - 10:30
Recryptor: A Reconfigurable In-Memory Cryptographic Cortex-M0 Processor for IoT, Y. Zhang, L. Xu, K. Yang, Q. Dong, S. Jeloka, D. Blaauw and D. Sylvester, Univ. of Michigan, USA

This paper proposes Recryptor, an energy efficient and compact ARM Cortex-M0 based reconfigurable cryptographic processor using in-memory computing. Recryptor is capable of accelerating a wide range of cryptography algorithms and standards, including public/private key cryptography and hash functions, by augmenting the memory of a commercial general purpose IoT processor resulting in a highly compact implementation. The wide bit-width of memory is ideally suited for high bitwidth (64 - 512b) arithmetic operations common in cryptographic functions. Recryptor (28.8 MHz at 0.7 V) achieves 6.8× average speedup and 12.8× average energy improvements over state-of-the-art software and hardware-accelerated implementations with only 0.128 mm^2 area overhead in 40nm CMOS.

C20-2 - 10:55
A 2.5ns-Latency 0.39pJ/b 289μm²/Gb/s Ultra-Light-Weight PRINCE Cryptographic Processor, N. Miura*, K. Matsuda*, M. Nagata*, S. Bhasin**, V. Yli-Mayry***, N. Homma***, Y. Mathieu****, T. Graba**** and J.-L. Danger****, *Kobe Univ., Japan, **Nanyang Technological Univ., Singapore, ***Tohoku Univ., Japan and ****Telecom ParisTech, France

An ultra-light-weight PRINCE cryptographic processor is developed. A fully-unrolled differential-logic architecture saves delay, energy, and area (i.e. hardware weight) of XOR as a dominant cipher component. An S-box is composed only by four kinds of compact composite gates and a replica-delay-based transition-edge aligner prevents glitches accumulated in the long unrolled combinational-logic data path to further suppress the weight. A 28nm CMOS prototype successfully demonstrates 2.5ns-latency with 0.39pJ/b and 289μm²/Gb/s of ultra-light-weight cryptographic performance.

C20-3 - 11:20
Strong Subthreshold Current Array PUF with 2^{65} Challenge-Response Pairs Resilient to Machine Learning Attacks in 130nm CMOS, X. Xi, H. Zhuang, N. Sun and M. Orshansky, The Univ. of Texas at Austin, USA

This paper presents a strong silicon physically unclonable function (PUF) immune to machine learning (ML) attacks. The PUF, termed the subthreshold current array (SCA) PUF, is composed of a pair of two-dimensional transistor arrays and a low-offset comparator. The fabricated PUF chip allows 2^{65} challenge-response pairs (CRPs) and achieves high reliability with average bit error rate (BER) of 5.8% for temperatures -20 to 80°C and $V_{DD} \pm 10\%$. The calibration-based CRPs filtering method effectively improves BER to 2.6% with a 10% loss of CRPs. When subjected to ML attacks, the PUF shows resilience that is 100X higher than known alternatives, with negligible loss in PUF unpredictability.

C20-4 - 11:45
A Sequence Dependent Challenge-Response PUF Using 28nm SRAM 6T Bit Cell, S. Jeloka*, K. Yang*, M. Orshansky**, D. Sylvester* and D. Blaauw*, *Univ. of Michigan and **The Univ. of Texas at Austin, USA

Conventionally, SRAM PUFs are only used for chip ID. The proposed sequence dependent PUF expands the challenge-response space of an SRAM PUF by an order of rows[(sequence length-1)], making it suitable for authentication. In addition, it has a sequence dependent non-linear behavior making it more immune to machine learning attacks. In 28nm, the 64x64 SRAM-based PUF has a bit area of $388F^2$ with energy ranging from 30fJ/bit - 88fJ/bit at 0.6V. It also provides high throughput, from 2.2Gbps to 6.8Gbps at 0.9V.

C20-5 - 12:10
A Continuous-Time Digital IIR Filter with Signal-Derived Timing, Agile Power Dissipation and Synchronous Output, Y. Chen*, X. Zhang**, Y. Lian***, R. Manohar**** and Y. Tsividis*, *Columbia Univ., USA, **National Univ. of Singapore, Singapore, ***York Univ., Canada and ****Yale Univ., USA

We present the first continuous-time digital IIR filter with power consumption tracking the input activity and varying by over 50X, resulting in a FoM varying from 2.5fJ to 0.05fJ. Only two tapped delays are used for a sixth-order filter. The 1.2V 65nm CMOS prototype achieves very high stopband rejection and includes an output converter to synchronous mode, allowing integration with discrete-time systems.

SESSION 21

High Speed ADCs [Suzaku II]

Thursday, June 8, 10:30-12:35

Chairpersons: M. Ito, Renesas System Design Co., Ltd.
                 E. Martens, imec

C21-1 - 10:30
A 12b 61dB SNDR 300MS/s SAR ADC with Inverter-Based Preamplifier and Common-Mode-Regulation DAC in 14nm CMOS FinFET, D. Luu*·**, L. Kull**, T. Toifl**, C. Menolfi**, M. Braendli**, P. A. Francese**, T. Morf**, M. Kossel**, H. Yueksel**, A. Cevrero**, I. Ozkaya** and Q. Huang*, *ETH Zurich and **IBM Research, Switzerland

A 300MS/s 12b SAR ADC achieving 61.6dB peak SNDR is presented. It reaches 60.5dB SNDR and 78.7dB SFDR with $0.8V_{pp,diff}$ input amplitude at Nyquist. The key elements are a comparator with inverter-based preamplifier and a SAR-based common-mode regulation. The regulation adjusts the common mode on a sample-by-sample basis to improve common-mode rejection. The ADC consumes 7.0mW from a single 0.85V supply, where 3.7mW is contributed by the reference buffer.

C21-2 - 10:55
A 0.014mm² 10-Bit 2GS/s Time-Interleaved SAR ADC with Low-Complexity Background Timing Skew Calibration, L. Luo, S. Chen, M. Zhou and T. Ye, Marvell - Shanghai, China

A 10-bit 2GS/s time-interleaved SAR ADC with low-complexity background timing skew calibration is presented. 10% of the area is utilized for the interleaving mismatch estimation and correction. The ADC achieves -64dB mismatch spur and 50.1dB SNDR at Nyquist rate, with 10.4mW power consumption and 0.014mm² area in 16nm.

C21-3 - 11:20
An 18-Bit 2MS/s Pipelined SAR ADC Utilizing a Sampling Distortion Cancellation Circuit with -107dB THD at 100kHz, D. Hummerston and P. Hurrell, Analog Devices, UK

This paper presents an 18-bit SAR ADC capable of -107dB THD for a 10V pk to pk 100kHz input. Distortion originating from the input switch's nonlinear on-resistance is cancelled by sampling the input onto two separate capacitor arrays, whose components are scaled to give the same nonlinear charge error, and then subtracting this charge during conversion. The new sampling scheme can support event-driven sampling, requires no active circuits and draws zero quiescent power.

C21-4 - 11:45
A 16-Bit 16MS/s SAR ADC with On-Chip Calibration in 55nm CMOS, J. Shen, A. Shikata, L. Fernando, N. Guthrie, B. Chen, M. Maddox, N. Mascarenhas, R. Kapusta and M. Coln, Analog Devices, Inc., USA

This paper presents a SAR ADC that is much smaller and faster than the recently reported precision (16-bit and beyond) SAR ADCs [1, 2, 3]. In addition, it features low input capacitance and an efficient on-chip foreground calibration algorithm to fix bit weight errors. Several other enabling techniques are also used, including signal independent reference switching using reservoir capacitors to improve speed and reduce area, LSB repeats and ADC residue measurement to improve efficiency. The prototype achieves 97.5dB SFDR while operating at 16MS/s and consumes 16.3mW. It was fabricated in 55nm CMOS and occupies 0.55mm^2.

C21-5 - 12:10
A 2GS/s 8b Flash ADC Based on Remainder Number System in 65nm CMOS, S. Zhu, B. Wu, Y. Cai and Y. Chiu, The Univ. of Texas at Dallas, USA

A non-interleaved 2GS/s, 8b flash ADC achieves an effec-tive resolution bandwidth (ERBW) of 1.74 GHz using a re-mainder number system (RNS) architecture, which results in reduced number of comparators while preserving the flash speed of the converter. The prototype ADC, fabricated in a 65nm CMOS process with an area of 0.08 mm^2, achieves an SNDR of 40.7 dB for a Nyquist input. The measured DNL and INL are ±0.14 and ±0.61 LSBs, respectively.

Luncheon Talk [Suzaku I]

Thursday, June 8, 12:40-14:00

Organizers: M. Ikeda, The Univ. of Tokyo
             M. Masahara, AIST

Approach to Develop Prosthetic Technology as a Part of Body, K. Endo, Xiborg

Once a part of human body is disabled physically or functionally, he would lose a huge amount of his quality of life, and the current available technology is not functional enough to compensate lost function in comprehensive way. On the other hand, several fields such as paralympic long jump show possibility of technology which could exceed human normal function. We are currently focusing on developing prosthetic technology to optimize sprint gait which is eventually useful to develop device supporting human life.

SESSION 22

Circuits Focus Session - Advanced Sensing Systems [Suzaku III]

Thursday, June 8, 14:00-15:40

Chairpersons: Y. Oike, Sony Semiconductor Solutions Corp.
               H. Lee, Google

C22-1 - 14:00 (Invited)
320x240 Back-Illuminated 10µm CAPD Pixels for High Speed Modulation Time-of-Flight CMOS Image Sensor, Y. Kato*, T. Sano*, Y. Moriyama*, S. Maeda*, T. Yamazaki*, A. Nose*, K. Shina*, Y. Yasu*, W. van der Tempel**, A. Ercan** and Y. Ebiko*, *Sony Semiconductor Solutions Corp., Japan and **SoftKinetic, Belgium

A 320x240 back-illuminated Time-of-Flight CMOS image sensor with 10µm CAPD pixels has been developed. The back-illuminated (BI) pixel structure maximizes the fill factor, allows for flexible transistor position and makes the light path independent of the metal layer. In addition, the CAPD pixel, which is optimized for high speed modulation, results in 80% modulation contrast at 100MHz modulation frequency.

C22-2 - 14:25 (Invited)
An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-µm CMOS for Automotive LIDAR Application, H. Akita*, I. Takai**, K. Azuma*, T. Hata* and N. Ozaki*, *DENSO Corp. and **Toyota Central R&D Labs., Inc., Japan

A feasibility imager chip of a 32 x 4-pixel array was developed in a 0.18-µm CMOS process for a small size automotive laser imaging detection and ranging. Each pixel consists of 8 single-photon avalanche diodes as a world-first 2-D pixel array with digital output macro pixel architecture which enables laser signal sensing under sunlight noise. Distance measurement results show less than 2.1%nonlinearity and 0.11-m standard deviation up to 20-m distance with 10%-reflective target under the ambient light of 75 klux.

C22-3 - 14:50
A 16.5 Giga Events/s 1024 × 8 SPAD Line Sensor with Per-Pixel Zoomable 50ps-6.4ns/bin Histogramming TDC, A. T. Erdogan, R. Walker, N. Finlayson, N. Krstajić, G. O. S. Williams and R. K. Henderson, Univ. of Edinburgh, UK

A 1024 × 8 single photon avalanche diode (SPAD) based line sensor for time resolved spectroscopy is implemented in 0.13 µm imaging CMOS with 23.78 µm pixel pitch at 49.31% fill factor. The line sensor can operate in single photon counting (SPC) mode (65 giga-events/s), time-correlated single photon counting (TCSPC) mode (194 million events/s) or histogramming mode (16.5 giga-events/s), increasing the count rate up to 85 times compared to TCSPC operation. This performance is enabled by a 512 channel histogramming TDC with 50ps-6.4ns/bin zoomable time resolution.

C22-4 - 15:15
A 272.49 pJ/pixel CMOS Image Sensor with Embedded Object Detection and Bio-Inspired 2D Optic Flow Generation for Nano-Air-Vehicle Navigation, K. Lee, S. Park, S.-Y. Park, J. Cho and E. Yoon, Univ. of Michigan, USA

We report a CMOS imager embedded with energy-efficient object detection and bio-inspired 2D optic flow generation cores for navigation of nano-air-vehicles (NAVs). The proposed vision-based navigation system employs spatial difference imaging and gradient orientation using mixed-signal circuits to achieve both energy-efficient and area-efficient implementation. The system achieved 272.49 pJ/pixel with 75% reduction in memory size for integrated operation of object detection and 2D optic flow generation.

SESSION 23

High-Speed and Power Efficient Wireless Transceivers [Suzaku II]

Thursday, June 8, 14:00-15:40

Chairpersons: J. Lee, National Taiwan Univ.
               A. Molnar, Cornell Univ.

C23-1 - 14:00
A 100mW 3.0 Gb/s Spectrum Efficient 60 GHz Bi-Phase OOK CMOS Transceiver, Y. Wang*, B. Liu*, H. Liu*, A. T. Narayanan*, J. Pang*, N. Li*, T. Yoshioka*, Y. Terashima*, H. Zhang*, D. Tang*, M. Katsuragi*, D. Lee**, S. Choi**, R. Wu*, K. Okada* and A. Matsuzawa*, *Tokyo Institute of Technology, Japan and **Samsung Electronics Co., Ltd., Korea

A novel high-data-rate low-power spectrum-efficient 60GHz Bi-Phase-On-Off-Keying (BPOOK) transceiver is presented for indoor short-range IoT application targeting IEEE 802.11ad/WiGig standard. By employing bi-phase encoder and double-balanced mixer, the BPOOK transmitter spectrum is efficient to be compliant with 2-channel bonding spectrum mask. The proposed 60GHz OOK transceiver is fabricated in 65nm CMOS, achieves 3.0 Gb/s data-rate and -46 dBm sensitivity, while consuming a power of 100mW including the on-chip 60GHz synthesizer.

C23-2 - 14:25
A 230-260GHz Wideband Amplifier in 65nm CMOS Based on Dual-Peak G_{max}-Core, D.-W. Park*, D. R. Utomo*, J.-P. Hong** and S.-G. Lee*, *KAIST and **CBNU, Korea

A dual-peak maximum achievable gain core design technique is proposed. It has been adopted into a 4-stage wideband amplifier. Implemented in a 65nm CMOS, the amplifier achieves 3dB bandwidth of 30GHz (230~260GHz), gain of 12.4±1.5dB, and peak PAE of 1.6% while dissipating 23.8mW, which corresponds to the widest bandwidth and highest gain per stage among other reported CMOS amplifiers operating above 200GHz.

C23-3 - 14:50
A 65nm CMOS I/Q RF Power DAC with 24 - 42dB 3rd Harmonic Cancellation and up to 18dB Mixed-Signal Filtering, B. Yang, E. Y. Chang, A. Niknejad, B. Nikolić and E. Alon, Univ. of California, Berkeley, USA

This paper presents an RF DAC transmitter (TX) with integrated, programmable harmonic cancellation as well as mixed-signal filtering at a peak power of 25.6dBm. The 65nm CMOS prototype uses device stacking and transformer combining and demonstrates 24dB to 42dB HD3 reduction across a frequency range of 0.7GHz to 2GHz, and up to 18dB of notching at a 40MHz offset.

C23-4 - 15:15
A 43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle, M. Mizokami*, T. Uozumi*, Y. Yamashita**, K. Shibata* and H. Sato*, *Renesas Electronics Corp. and **Renesas System Design Co., Ltd., Japan

A high efficiency class-E power amplifier (PA) is proposed with only 3 external components. The PA is driven by a 33.3% duty cycle with a rise-edge-synchronized harmonic calibration. The 33.3% duty cycle operation lowers the drain voltage swing as well as the 3rd harmonics, and the calibration optimizes the duty imbalance and the phase difference between the differential signals, improving the PA efficiency and eliminating the external harmonic filters. The PA fabricated in 40nm CMOS has achieved the output power of 20dBm and the TX efficiency of 43% with "only 3 external components" in the impedance matching network.

SESSION 24

Physical Sensors [Suzaku III]

Thursday, June 8, 16:00-17:40

Chairpersons: Y. Hirose, Panasonic Corp.
B. Ginsburg, Texas Instruments

C24-1 - 16:00
A 10.1" 56-Channel, 183 uW/electrode, 0.73 mm^2/sensor High SNR 3D Hover Sensor Based on Enhanced Signal Refining and Fine Error Calibrating Techniques, Y. Huh*, S.-W. Hong**, S.-H. Park*, J.-S. Bang*, C. Park**, S. Park**, H.-D. Gwon*, S.-U. Shin*, H. Shin*, S.-W. Choi*, Y.-M. Ju*, J.-H. Lee* and G.-H. Cho*, *KAIST and **Samsung Electronics Co., Ltd., Korea

This paper presents a high SNR self-capacitance sensing 3D hover sensor that does not use panel offset cancelation blocks. Not only reducing noise components, but increasing the signal components together, this paper achieved a high SNR performance while consuming very low power and die-area. Thanks to the proposed separated structure between driving and sensing circuits of the self-capacitance sensing scheme (SCSS), the signal components are increased without using high-voltage MOS sensing amplifiers which consume big die-area and power and badly degrade SNR. In addition, since a huge panel offset problem in SCSS is solved exploiting the panel's natural characteristics, other costly resources are not required. Furthermore, display noise and parasitic capacitance mismatch errors are compressed. We demonstrate a 39dB SNR at a 1cm hover point under 240Hz scan-rate condition with noise experiments, while consuming 183uW/electrode and 0.73mm^2/sensor, which are the power per electrode and the die-area per sensor, respectively.

C24-2 - 16:25
A Robust and Versatile, -40°C to +180°C, 8Sps to 1kSps, Multi Power Source Wireless Sensor System for Aeronautic Applications, R. Grezaud*, L. Sibeud*, F. Lepin*, J. Willemin*, J.-C. Riou** and B. Gomez*, *CEA-LETI and **SAFRAN Electronics & Defense, France

To meet severe aeronautic environment constraints, we propose in this paper a versatile 794µW autonomous multi-power-source wireless sensor node interfacing with aeronautic-grade resistive bridge transducers and operating over a wide range of -40°C to +180°C in 180nm HT SOI technology. Compared to previously reported works, it provides robust and versatile 8Sps-1kSps sensor interface and RFID/micro wind turbine power supply scheme.

C24-3 - 16:50
A 6×5×4mm^3 General Purpose Audio Sensor Node with a 4.7µW Audio Processing IC, M. Cho*, S. Oh*, S. Jeong*, Y. Zhang*, I. Lee*, Y. Kim*, L.-X. Chuo*, D. Kim*, Q. Dong*, Y.-P. Chen*, M. Lim**, M. Daneman**, D. Blaauw*, D. Sylvester* and H.-S. Kim*, *Univ. of Michigan and **Invensense, USA

We present a complete, fully functional energy-autonomous audio sensor node with 6x5x4mm^3 form factor. The system uses a new audio processing IC integrated with a MEMS microphone, general purpose 32-bit processor, 8Mb Flash, RF transceiver with custom 3D antenna, PV cells for energy harvesting and battery. The 4.7µW audio processing IC performs audio acquisition with 4-32x compression. The complete stand-alone system achieves 38mins of speech recording and energy autonomous operation in room light.

C24-4 - 17:15
A 4.7µW Switched-Bias MEMS Microphone Preamplifier for Ultra-Low-Power Voice Interfaces, S. Oh, T. Jang, K. D. Choo, D. Blaauw and D. Sylvester, Univ. of Michigan, USA

This paper presents a switched-bias MEMS microphone preamplifier for an ultra-low-power voice interface. A switched-MOSFET periodically changes the MOSFET between strong inversion and accumulation to inherently reduce 1/f noise. In addition, a proposed coupling capacitor allows the microphone to benefit from a high bias voltage while the preamp can use a low VDD. The preamp achieves 7.3µVrms input referred noise (A-weighted) with 3.4µA, improving NEF by 4.5x. Acoustic testing with the preamp and MEMS microphone shows 61.3dBA SNR at 94dB SPL.

SESSION 25

High-Speed Wireline Circuits [Suzaku II]

Thursday, June 8, 16:00-18:05

Chairpersons: K. Sunaga, NEC Corp.
B. Casper, Intel Corp.

C25-1 - 16:00
A 32Gb/s, 4.7pJ/bit Optical Link with −11.7dBm Sensitivity in 14nm FinFET CMOS, J. Proesel*, Z. Deniz*, A. Cevrero**, I. Ozkaya**, S. Kim*, D. Kuchta*, S. Lee***, S. Rylov*, H. Ainspan*, T. Dickson*, J. Bulzacchelli* and M. Meghelli*, *IBM T. J. Watson Research Center, USA, **IBM Research, Switzerland and ***IBM Systems, USA

This work presents an 850nm VCSEL-based multi-mode 32Gb/s NRZ optical link with circuits in 14nm bulk FinFET CMOS. The TX uses a 3-tap, 1/2-UI-spaced FFE to improve eye opening. The RX uses a low-BW, low-noise TIA and a speculative 1-tap DFE for high sensitivity. The TX and RX power efficiencies are 3.3 and 1.4pJ/bit, respectively. The link sensitivity is -11.7dBm OMA at BER=10^{-12} with PRBS31 data.

C25-2 - 16:25
A 60 Gb/s 1.9 Pj/bit NRZ Optical-Receiver with Low Latency Digital CDR in 14nm CMOS FinFET, A. Cevrero*, I. Ozkaya*,***, P. A. Francese*, C. Menolfi*, M. Braendli*, T. Morf*, D. Kuchta**, M. Kossel*, L. Kull*, D. Luu*, J. Proesel**, Y. Leblebici*** and T. Toifl*, *IBM Research, Switzerland, **IBM Research, USA and ***EPFL, Switzerland

This work reports a low power implementation of a 60Gb/s NRZ optical receiver (RX) in 14nm bulk CMOS finFET featuring a first-order digital CDR with high jitter tolerance (JTOL). The design includes a single phase-rotator (PR) with low complexity control logic suitable for high-speed applications. Multi-phase clock signals that drive data/edge slicers are created by an open loop quadrature clock generator. The circuit, characterized in an 850nm VCSEL based optical link, recovers PRBS7 data (BER<10^{-12}) at 60Gb/s with a frequency tracking range of ±600ppm. The measured sinusoidal JTOL indicates a corner frequency of 80MHz, with high frequency JTOL of 0.16UI$_{pp}$ at -5dBm optical modulation amplitude (OMA). The RX energy efficiency is 1.9pJ/bit.

C25-3 - 16:50
A 2.25-mW/Gb/s 80-Gb/s-PAM4 Linear Driver with a Single Supply Using Stacked Current-Mode Architecture in 65-nm CMOS, S. Nakano, M. Nagatani, M. Nogawa, Y. Kawamura, K. Kikuchi, K. Tsuzuki and H. Nosaka, NTT Corp., Japan

This paper presents a low-power linear driver for a coherent optical transmitter. We propose a driver using stacked current-mode architecture to achieve low-power consumption with a single supply. The driver can drive from 25 to 50 Ω impedances with almost the same output waveforms by using a variable equalizer and adjusting the current of the post-amplifier. The proposed driver was fabricated in 65-nm CMOS technology and achieved the power efficiency of 3.6 mW/Gbps with a differential output swing of 2.9 Vpp for a 50-Gbps NRZ signal and 2.25 mW/Gbps with a differential output swing of 2.0 Vpp for an 80-Gbps PAM4 signal.

C25-4 - 17:15
A 26-Gb/s 8.1-mW Receiver with Linear Sampling Phase Detector for Data and Edge Equalization, Y. Wang*,**, Z. Li*, J. Zhuang***, C. Zhi*** and C. P. Yue*, *The Hong Kong Univ. of Science and Technology, China, **Xilinx Inc., Singapore and ***Brite Semiconductor, China

This paper presents a source-synchronous receiver with a quarter-rate linear sampling phase detector (LSPD) with embedded FFE and DFE. The 1-tap FFE and 1-tap DFE are realized by reusing the data samples generated in the LSPD to minimize power and area overhead. The equalization is applied to both that data and edge samples to suppress ISI for improving BER and bit efficiency. The 28-nm CMOS receiver IC achieves error-free operation up to 26 Gb/s with a superior bit efficiency of 0.31 pJ/b while compensating for 14-dB channel loss at 13 GHz.

C25-5 - 17:40
A 28.05Gb/s Transceiver Using Quarter-Rate Triple-Speculation Hybrid-DFE Receiver with Calibrated Sampling Phases in 32nm CMOS, G. Gangasani*, J. F. Bulzacchelli**, M. Wielgos*, W. Kelly*, V. Sharma***, A. Prati***, G. Cervelli***, D. Gardellini***, M. Baecher*, M. Shannon*, T. Beukema**, J. Garlett*, H. H. Xu*, T. Toifl****, M. Meghelli**, J. Ewen* and D. Storaska*, *GLOBALFOUNDRIES, **IBM Research, USA, ***Miromico and ****IBM Research, Switzerland

This paper presents a 28.05Gb/s transceiver in 32nm SOI CMOS technology. The receiver employs a quarter-rate triple-speculation architecture. Techniques are introduced to adapt for mismatches in tap weights, gains and sampling phases. Error-free signaling at 28.05Gb/s is demonstrated with the transceiver over a 48dB loss backplane channel. In a four-port configuration, the power consumption at 28.05Gb/s is 484mW/lane, giving a FOM of 0.36mW/Gb/s/dB.

SESSION 26

Processors and SoC [Suzaku I]

Thursday, June 8, 16:00-18:05

Chairpersons: M. Hashimoto, Osaka Univ.
                J. Wuu, AMD

C26-1 - 16:00
A 501mW 7.61Gb/s Integrated Message-Passing Detector and Decoder for Polar-Coded Massive MIMO Systems, Y.-T. Chen*, C.-C. Cheng**, T.-L. Tsai**, W.-C. Sun**, Y.-L. Ueng** and C.-H. Yang***, *National Chiao Tung Univ., **National Tsing Hua Univ. and ***National Taiwan Univ., Taiwan

This work presents the first integration of a message-passing detector (MPD) and a polar decoder. A soft-output MPD, which is essential to approach the channel capacity, is first proposed. Compared to the state-of-the-art design, the proposed MPD achieves a 6.9x higher throughput with 49% lower energy, despite the soft outputs. The proposed polar decoder achieves a 1.35x higher throughput with comparable energy. The chip delivers a throughput of 7.61Gb/s for mas-sive MIMO systems with up to 128 antennas and 32 users.

C26-2 - 16:25
A 12.4pJ/cycle Sub-Threshold, 16pJ/cycle Near-Threshold ARM Cortex-M0+ MCU with Autonomous SRPG/DVFS and Temperature Tracking Clocks, J. Myers, A. Savanth, P. Prabhat, S. Yang, R. Gaddh, S. O. Toh and D. Flynn, ARM Ltd., UK

IoT requirements are almost as varied as the Things to which they are applied, but common demands are maximum battery life with minimum system cost and physical volume. Sub-threshold operation is promising, but even a single un-optimized or always-on component can eliminate low-voltage gains elsewhere. This work presents a highly integrated sub-threshold capable ARM based MCU with fully integrated multi-mode IVR, always-on power control, and on-chip clock sources, achieving 12.44pJ/cycle active energy (6.3pJ/cycle ideal), 139.4nW standby power (46nW ideal) and 1μW ULPBench power. Simple adaptive circuits are demonstrated to be efficient and correct for standby IVR and active system clocks across 0-70°C.

C26-3 - 16:50

A 2.267 Gbps, 93.7pJ/b Non-Binary LDPC Decoder for Storage Applications, Y. Toriyama and D. Marković, Univ. of California, Los Angeles, USA

This paper presents a Non-Binary LDPC decoder with information throughput of 2.267Gbps and power consumption of 212.4mW, yielding an energy efficiency of 93.7pJ/b, implemented in a 40nm CMOS technology. The employed code is long and high-rate without degree-2 variable nodes, resulting in a low error floor. A dual decoding algorithm scheme alleviates the computational complexity of decoding, realized in an efficient architecture with high parallelism and avoidance of idle clock cycles.

C26-4 - 17:15

A 130nm FeRAM-Based Parallel Recovery Nonvolatile SOC for Normally-OFF Operations with 3.9× Faster Running Speed and 11× Higher Energy Efficiency Using Fast Power-On Detection and Nonvolatile Radio Controller, Z. Wang*, F. Su*, Y. Wang*, Z. Li*, X. Li*, R. Yoshimura**, T. Naiki**, T. Tsuwa**, T. Saito**, Z. Wang**, K. Taniuchi**, M.-F. Chang***, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **Rohm Co., Ltd., Japan and ***National Tsing Hua Univ., Taiwan

This paper proposes a FeRAM-based Nonvolatile SOC (NVSOC) to obtain system-level startup acceleration and energy efficiency enhancement for normally-off applications. The NVSOC supports adaptive parallel recovery and two fast startup schemes. The quick power-on detection is enabled by hysteresis-comparator based voltage detector and leakage cut-off controller. A nonvolatile radio frequency controller (NVRF) is first proposed to further boost the recovery of transceivers. Compared with the fastest switching nonvolatile processor based platform, measurement results show NVSOC achieves 3.9× faster running speed and 11× higher energy efficiency to execute periodical normally-off sensing and transmitting tasks. This is the first parallel recovery enabled NVSOC with fast power-on detection and RF initialization capability.

C26-5 - 17:40

A Battery-Less 507nW SoC with Integrated Platform Power Manager and SiP Interfaces, F. Yahya*, C. J. Lukas*, J. Breiholz*, A. Roy*, H. N. Patel*, N. Liu*, X. Chen**, A. Kosari**, S. Li*, D. Akella*, O. Ayorinde*, D. Wentzloff** and B. H. Calhoun*, *Univ. of Virginia and **Univ. of Michigan, USA

A 507nW self-powered SoC is demonstrated for ultra-low power (ULP) internet-of-things (IoT) applications. The SoC includes ULP system-in-package (SiP) interfaces that enable its harmonious integration with a radio transmitter (TX) and a non-volatile memory (NVM). The energy harvesting platform power manager (EH-PPM) powers the SoC as well as off-chip components and is optimized for low quiescent power. It supplies the SoC with 0.5V, 1.0V, and 1.8V and can also power ULP sensors and the SiP components while running an example shipping-integrity tracking algorithm. A power monitor (PM) cold-boots the SoC from NVM and adapts the system's power consumption. The tight integration between the SoC's blocks enables sub-µW operation.

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2017 Symposium on VLSI Techonlogy / Circuits

International Forum on Singularity: Exponential X (Friday Forum)

Friday, June 9, 9:00-16:30

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General Chair: T. Hiramoto, Univ. of Tokyo
Program Committee Chair K. Yano, Hitachi

    8:30   **Welcome to Exponential X,** K. Yano, Hitachi

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Session 1. Exponential Technology

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    9:15   **Exponential Neuromorphic Systems for Singularity,** V. De, Intel

    9:45   **Exponential Computing for Singularity,** M. Saito, PEZY

    10:15   **Exponential Connectivity for Singularity,** A. Amerasekera, UCB/BWRC

    10:45   **Exponential Commerce for Singularity,** T. Kitagawa, Rakuten

    11:15   Panel **"Where will the Next Exponential Technology Arise?"**

    12:00   **Lunch Time**

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Session 2. Exponential Humans

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    13:30   **Exponential Intelligence for Singularity,** K. Ataka, Yahoo

    14:00   **Exponential Healthcare for Singularity,** Y. Ishikawa

    14:30   **Exponential Mind for Singularity,** J. Tani, KAIST

    15:00   **Exponential Robotics for Singularity,** K. Kanaoka, Ritsumeikan Univ.

    15:30   **Break**

    15:45   Panel **"How will Human Beings Change in the Future?"**