2017 Symposium on VLSI Technology Short Course

Technology Enablers for 5nm and Next Wave of Integration [Shunju II, III]

Monday, June 5, 8:30-17:10

Organizers / Chairs: S. Yamakawa, Sony Semiconductor Solutions Corp.
W. Rachmady, Intel Corp.

8:30 **Introduction**

8:35 **CMOS Device Technology Enablers and Challenges for 5nm Node,** P. Hashemi and T. B. Hook, IBM Research

9:25 **Heterogeneous Integration of Ge, III-V, and 2D on Si – from More Moore to Beyond CMOS –,** M. Takenaka, The Univ. of Tokyo

10:15 **Break**

10:35 **Design & Technology Co-Optimization for High Performance SoC,** T.-B. Chan, Qualcomm Technologies, Inc.

11:25 **The Duality of Interconnect Scaling in Sub-10nm Technology Nodes: Increasingly Complex, Increasingly Important,** R. Fox, GLOBALFOUNDRIES

12:15 **Lunch**

13:30 **Heterogeneous 3D/2.5D Integration toward IoT and AI Era,** M. Koyanagi, Tohoku Univ.

14:20 **Device Challenges for Scaled Analog-RF,** F.-L. Hsueh, Y.-C. Peng, J.-J. Horng, W.-C. Chen, S. Yang, H. Liu, B. Yang, V. Chou, A. Kundu, C.-T. Lu, M.-C. Chuang, C.-H. Chen, H.-H. Hsieh, C.-H. Chang, Y.-W. Chen, L.-C. Cho, J. Fu and J. Tsai, TSMC

15:10 **Break**

15:30 **Embedded Memory Design – Memories Differentiate Microcontoller Solutions –,** T. Jew, NXP Semiconductors

16:20 **On DIE Processor in Memory – PIM on DRAM –,** F. Devaux, uPmem

Demo Session & Reception [Suzaku I, II, III]

Monday, June 5, 17:30-19:30

Organizers / Chairs: Y. Oike, Sony Semiconductor Solutions Corp.
N. Sugii, Hitachi, Ltd.
R. Navid, Intel Corp.

Newly Established Venue for in-depth Discussion with Authors:

- Demonstration of chip operation highlighting key results
- Systems showcasing potential applications for circuit-level innovations
- Table-top real-time demonstration of new device characterization
- Visual illustration of technological concepts and analyses

T8-1
Towards A Fully Integrated, Wirelessly Powered, and Ordinarily Equipped On-Lens System for Successive Dry Eye Syndrome Diagnosis, J.-C. Chiou, S.-H. Hsu, Y.-C. Huang, G.-T. Yeh, K.-S. Dai and C.-K. Kuei, National Chiao Tung Univ., Taiwan

T10-4
Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal-Aware Lifetime Prediction Methodology, H. Jiang*,**, L. Shen*, S. H. Shin**, N. Xu***, G. Du*, B.-Y. Nguyen****, O. Faynot*****, M. A. Alam**, X. Zhang* and X. Y. Liu*, *Peking Univ., China, **Purdue Univ., ***Univ. of California, Berkeley, ****Soitec, USA and *****CEA-LETI, France

JFS3-3
Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application, S. H. Wu*, X. Y. Jia*, X. Li*, C. C. Shuai*, H. C. Lin*, M. C. Lu*, T. H. Wu*, M. Y. Liu*, J. Y. Wu*, D. Matsubayashi**, K. Kato** and S. Yamazaki**, *United Microelectronics Corporation, Singapore and **Semiconductor Energy Laboratory Co., Ltd., Japan

T14-1
First Experimental Observation of Channel Thickness Scaling (Down to 3 nm) Induced Mobility Enhancement in UTB GeOI *n*MOSFETs, W. H. Chang, T. Irisawa, H. Ishii, H. Hattori, H. Ota, H. Takagi, Y. Kurashima, N. Uchida and T. Maeda, AIST, Japan

T15-3
Flash Reliability Boost Huffman Coding (FRBH): Co-Optimization of Data Compression and V_{TH} Distribution Modulation to Enhance Data-Retention Time by Over 2900x, Y. Deguchi, A. Kobayashi, H. Watanabe and K. Takeuchi, Chuo Univ., Japan

C1-2
Innovative Solutions toward Future Society with AI, Robotics, and IoT, T. Yukitake, Panasonic Corp., Japan

C2-3
A Heterogeneous Microprocessor for Energy-Scalable Sensor Inference Using Genetic Programming, H. Jia, J. Lu, N. K. Jha and N. Verma, Princeton Univ., USA

C2-4
A 3.43TOPS/W 48.9pJ/Pixel 50.1nJ/Classification 512 Analog Neuron Sparse Coding Neural Network with On-Chip Learning and Classification in 40nm CMOS, F. N. Buhler*, P. Brown*, J. Li*.**, T. Chen*, Z. Zhang* and M. P. Flynn*, *Univ. of Michigan and **Intel Corp., USA

C4-1
A Fully Integrated Closed-Loop Neuromodulation SoC with Wireless Power and Bi-Directional Data Telemetry for Real-Time Human Epileptic Seizure Control, C.-H. Cheng, P.-Y. Tsai, T.-Y. Yang, W.-H. Cheng, T.-Y. Yen, Z. Luo, X.-H. Qian, Z.-X. Chen, T.-H. Lin, W.-H. Chen, W.-M. Chen, S.-F. Liang, F.-Z. Shaw, C.-S. Chang, F.-Y. Shih, Y.-L. Hsin, C.-Y. Lee, M.-D. Ker and C.-Y. Wu, National Chiao Tung Univ., Taiwan

C4-2
A Bone-Guided Cochlear Implant CMOS Microsystem Preserving Acoustic Hearing, X.-H. Qian*, Y.-C. Wu**, T.-Y. Yang*, C.-H. Cheng*, H.-C. Chu*, W.-H. Cheng*, T.-Y. Yen*, T.-H. Lin*, Y.-J. Lin*, Y.-C. Lee*, J.-H. Chang*, S.-T. Lin*, S.-H. Li**, T.-C. Wu*, C.-C. Huang**, C.-F. Lee***, C.-H. Yang**, C.-C. Hung*, T.-S. Chi*, C.-H. Liu**, M.-D. Ker* and C.-Y. Wu*, *National Chiao Tung Univ., **National Taiwan Univ. and ***Hualien Tzu Chi Medical Center, Taiwan

JFS2-1
A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Solenoid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS, H. K. Krishnamurthy, S. Weng, G. E. Matthew, R. Saraswat, K. Ravichandran, J. Tschanz and V. De, Intel Corp., USA

JFS2-2
A 6Gb/s Rotatable Non-Contact Connector with High-Speed/I²C/CAN/SPI Interface Bridge IC, M. Haraguchi*, A. Kosuge*, T. Igarashi**, S. Masaki**, M. Sueda**, M. Hamada* and T. Kuroda*, *Keio Univ. and **Socionext Inc., Japan

JFS2-4
A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications, S. Park*, T. Cho*, M. Kim*, H. Park** and K. Lee*, *KAIST and **Seoul National Univ. of Science and Technology, Korea

C17-3
A Single-Chip 2048×1080 Resolution 32fps 380mW Trinocular Disparity Estimation Processor in 28nm CMOS Technology, J. Narinx, T. Demirci, A. Akin and Y. Leblebici, EPFL, Switzerland

C19-1
A 4.1Mpix 280fps Stacked CMOS Image Sensor with Array-Parallel ADC Architecture for Region Control, T. Takahashi*, Y. Kaji**, Y. Tsukuda*, S. Futami*, K. Hanzawa***, T. Yamauchi*, P. W. Wong***, F. Brady***, P. Holden***, T. Ayers***, K. Mizuta*, S. Ohki*, K. Tatani*, T. Nagano*, H. Wakabayashi*** and Y. Nitta*, *Sony Semiconductor Solutions Corp., **Sony LSI Design Inc., Japan and ***Sony Electronics Inc., USA

C22-1
320x240 Back-Illuminated 10μm CAPD Pixels for High Speed Modulation Time-of-Flight CMOS Image Sensor, Y. Kato*, T. Sano*, Y. Moriyama*, S. Maeda*, T. Yamazaki*, A. Nose*, K. Shina*, Y. Yasu*, W. van der Tempel**, A. Ercan** and Y. Ebiko*, *Sony Semiconductor Solutions Corp., Japan and **SoftKinetic, Belgium

C24-3
A 6×5×4mm³ General Purpose Audio Sensor Node with a 4.7μW Audio Processing IC, M. Cho*, S. Oh*, S. Jeong*, Y. Zhang*, I. Lee*, Y. Kim*, L.-X. Chuo*, D. Kim*, Q. Dong*, Y.-P. Chen*, M. Lim**, M. Daneman**, D. Blaauw*, D. Sylvester* and H.-S. Kim*, *Univ. of Michigan and **Invensense, USA

C26-4
A 130nm FeRAM-Based Parallel Recovery Nonvolatile SOC for Normally-OFF Operations with 3.9× Faster Running Speed and 11× Higher Energy Efficiency Using Fast Power-On Detection and Nonvolatile Radio Controller, Z. Wang*, F. Su*, Y. Wang*, Z. Li*, X. Li*, R. Yoshimura**, T. Naiki**, T. Tsuwa**, T. Saito**, Z. Wang**, K. Taniuchi**, M.-F. Chang***, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **Rohm Co., Ltd., Japan and ***National Tsing Hua Univ., Taiwan

SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Tuesday, June 6, 8:00-10:10

Chairpersons: M. Masahara, AIST
C.-P. Chang, Applied Materials

T1-1 - 8:00
Welcome and Opening Remarks
S. Inaba, Toshiba Memory Corp.
M. Khare, IBM

T1-2 - 8:45 (Plenary)
5G and It's Surrounding Situations until 2020, T. Tsutsui, SoftBank Corp., Japan

Everybody getting excited with the 5G, mixing cats and dogs together. But the reality is, there is physical limitations and no magic, we should be cool. Whereas a lot would get to be possible and that should not be under estimated, and we should know what would be possible and what would not. Industry experts should be able to figure out better images before it actually comes, so as not to make big mistakes. Looking around 5G and it's surrounding technologies, in view of capabilities and physical limitations, I would like to briefly survey situations around forthcoming these years. So far with my experience, I believe I can figure out a little bit better images, and can help a little.

T1-3 - 9:25 (Plenary)
Privacy and Security: Key Requirements for Sustainable IoT Growth, F. Assaderaghi, G. Chindalore, B. Ibrahim, H. de Jong, M. Joye, S. Nassar, W. Steinbauer, M. Wagner and T. Wille, NXP Semiconductors, USA

As IoT moves beyond a catchphrase and starts to provide meaningful solutions in multiple fields, three of its critical pillars are now well understood:

- Transducers are needed as means of interacting with the environment and machines, and in converting stimuli to data and vice versa. These sensors and actuators form the basis of contextual awareness.
- Given that many end-node IoT devices are size and power constrained, local low-power computing is essential. The need for power-efficient end-node and edge computing becomes more apparent when latency, network bandwidth, and real time analytics are considered.
- Low power communication links to transmit the data between IoT devices and local aggregators or cloud resources form the third pillar.

Missing in this picture, and not fully appreciated yet, is the fourth pillar of IoT: privacy and security (P&S). If IoT is all about data, how P&S is treated will determine IoT's fate: a second phase of rapid proliferation or ultimate demise and collapse. Recent breaches in P&S are starting to change the industry's view on this issue. Even IoT end nodes that are low cost and have limited functionality pose significant risk to the entire system when their security is breached. This is due to the networking nature of the IoT that exposes a massive attack surface, making these devices ideal attack points for causing disruptions and stealing sensitive data. PC-era Internet security has been an expensive afterthought that has cost industry and consumers billions of dollars. Therefore, we should approach IoT differently, making P&S a key requirement at the design phase itself, and address all life-cycle aspects from initial deployment to in-field updates, to end-of-life decommissioning. This is a system level challenge that requires complete end-end HW/SW solutions, developed in partnership with the entire ecosystem.

Circuits SESSION 1

Welcome and Plenary Session [Shunju I, II, III]

Tuesday, June 6, 10:30-12:30

Chairpersons: M. Ikeda, The Univ. of Tokyo
K. Chang, Xilinx Inc.

C1-1 - 10:30
Welcome and Opening Remarks
M. Motomura, Hokkaido Univ.
G. Lehmann, Infineon Technologies AG

C1-2 - 10:50 (Plenary)
Innovative Solutions toward Future Society with AI, Robotics, and IoT, T. Yukitake, Panasonic Corp., Japan

AI, Robotics, and IoT have attracted enormous attention, expected to greatly change our society in the future. With these innovative technologies, our society would become (1) a borderless communication society, (2) a symbiotic society with robots, and (3) a safe, secure and comfortable network society. This plenary talk will show our specific initiatives, aiming at society heading for the futures, namely, (1) automatic translation, (2) underwater robot, and (3) large scale monitoring system. All of them work in collaboration with cloud, and will evolve into an advanced system. At the same time, higher performance and more intelligent processing is required on the edge side, thus we expect VLSI to play even more important roles.

C1-3 - 11:40 (Plenary)
Inside Waymo's Self-Driving Car: My Favorite Transistors, D. L. Rosenband, Waymo, USA

Waymo's self-driving Acbasrtsr acct ontain a broad set of technologies that enable our cars to sense the vehicle surroundings, perceive and understand what is happening in the vehicle vicinity, and determine the safe and efficient actions that the vehicle should take. Many of these technologies are rooted in advanced semiconductor technologies, e.g. faster transistors that enable more compute or low noise designs that enable the faintest sensor signals to be perceived. This paper summarizes a few areas where semiconductor technologies have proven to be fundamentally enabling to self-driving capabilities. The paper also lays out some of the challenges facing advanced semiconductors in the automotive context, as well as some of the opportunities for future innovation.

SESSION 2

Technology Focus Session - Nonvolatile & Embedded Memory [Shunju II, III]

Tuesday, June 6, 14:00-15:40

Chairpersons: S. S. Chung, National Chiao Tung Univ.
K. Baker, Freescale Semiconductor, Inc. / NXP Semiconductors N.V.

T2-1 - 14:00 (Invited)
Memory Technology for the Terabit Era: from 2D to 3D, J. Van Houdt, KU Leuven and imec, Belgium

Current stand-alone memory technologies for high density data storage are still based on electron-based principles that were established in the 1960s. While high bandwidth memories close to the CPU are still based on the 1T1C DRAM cell [1], also the nonvolatile space is still dominated by floating gate and charge trap concepts [2,3]. Meanwhile we have seen a major shift in the latter type, since Flash has made the jump to 3D monolithic integration, while, however, keeping with the same operating mechanisms. This transition has enabled a new roadmap by stacking ever more layers on the same chip. Although initially the technology was supposed to strongly lower the cost per bit [4], it turned out to be more expensive at first and several generations were needed to fully displace the planar floating gate concept, which essentially stopped scaling at the 15nm node [5]. In this paper this transition is discussed as well as its main limitations, and some suggestions are given for further scaling of 3D memories.

T2-2 - 14:25 (Invited)
Embedded Memories for Mobile, IoT, Automotive and High Performance Computing, J. Chang, H.-J. Liao, Y.-D. Chih, M. Sinangil, Y.-H. Chen, M. Clinton and S.-L. L. Lu, TSMC, Taiwan

Embedded memories play an important role to enable applications for mobile, IoT, security and high performance computing. In this paper, we presented the SRAM and non-volatile memories for different applications.

T2-3 - 14:50
A Low-Power Cu Atom Switch Programmable Logic Fabricated in a 40nm-Node CMOS Technology, X. Bai, T. Sakamoto, M. Tada, M. Miyamura, Y. Tsuji, A. Morioka, R. Nebashi, N. Banno, K. Okamoto, N. Iguchi, H. Hada and T. Sugibayashi, NEC Corp., Japan

For the first time, a 40nm-node, 2x logic density, 3.8x operation speed, and 3x power efficient, nonvolatile programmable logic (NPL) is demonstrated by using Cu atom switch for configuration switches. The switching characteristics of the atom switch are kept in scaling down to 64/32nm device area, and an improved PSE reduces set voltage while keeping low leakage current, enabling core transistors to select the atom switches. The developed 40nm NPL is a strong candidate for the next wave of energy-efficient computing.

T2-4 - 15:15
A Cross Point Cu-ReRAM with a Novel OTS Selector for Storage Class Memory Applications, S. Yasuda, K. Ohba, T. Mizuguchi, H. Sei, M. Shimuta, K. Aratani, T. Shiimoto, T. Yamamoto, T. Sone, S. Nonoguchi, J. Okuno, A. Kouchiyama, W. Otsuka and K. Tsutsui, Sony Semiconductor Solutions Corp., Japan

This paper demonstrates a cross point Cu based Resistive Random Access Memory (Cu-ReRAM) technology suitable for Storage Class Memory (SCM) applications. Two key technologies have been developed for large capacity of 100Gb-class SCM with 100 ns program speed and 10M cycles of program endurance. One is tight resistance distributions of Cu-ReRAM by inserting a barrier layer to prevent excess intermixing. The other is a novel Boron and Carbon (BC) based Ovonic Threshold Switch (OTS) selector which meets requirements for large cross point arrays with low leakage current, low threshold voltage variability, and high endurance.

SESSION 3

III-V [Shunju I]

Tuesday, June 6, 14:00-15:40

Chairpersons: T. Tsunomura, Tokyo Electron Ltd.
P. Ye, Purdue Univ.

T3-1 - 14:00
Record Performance for Junctionless Transistors in InGaAs MOSFETs, C. B. Zota, M. Borg, L.-E. Wernersson and E. Lind, Lund Univ., Sweden

We demonstrate junctionless tri-gate MOSFETs utilizing a single layer 7 nm thick $In_{0.80}Ga_{0.20}As$ (N_D = 1×10^{19} cm^{-3}) as both channel and contacts. Devices with source and drain metal separation of 32 nm and L_G of 25 nm exhibit SS = 76 mV/dec., both the highest reported *gm* = 1.6 mS/μA and I_{ON} = 160 μA/μm (V_{DD} = 0.5 V, I_{OFF} = 100 nA/μm) for a junctionless transistor. We also examine the influence of the contact thickness, comparing double-layer junctionless devices with 37 nm thick contacts with single-layer 7 nm contact devices.

T3-2 - 14:25
Vertical Heterojunction InAs/InGaAs Nanowire MOSFETs on Si with I_{on} = 330 μA/μm at I_{off} = 100 nA/μm and V_D = 0.5V, O.-P. Kilpi, J. Wu, J. Svensson, E. Lind and L.-E. Wernersson, Lund Univ., Sweden

We present vertical InAs nanowire MOSFETs on Si with an $In_{0.7}Ga_{0.3}As$ drain. The devices show I_{on} and g_m/SS record performance for vertical MOSFETs and I_{off} below 1 nA/μm at V_D 0.5 V. We show a device with g_m=1.4 mS/μm and *SS*=85 mV/dec, therefore having Q-value (*gm/SS*) of 16. The device has I_{on}=330 μA/μm and 46 μA/μm at I_{off} 100 nA/μm and 1 nA/μm, respectively. Furthermore, we show a device with *SS*=68 mV/dec and I_{on}=88 μA/μm at I_{off} 1 nA/μm and V_D 0.5 V.

T3-3 - 14:50
First Demonstration of ~3500 cm^2/V-s Electron Mobility *and* Sufficient BTI Reliability (Max V_{ov} Up to 0.6V) $In_{0.53}Ga_{0.47}As$ nFET Using an IL/$LaSiO_x$/HfO_2 Gate Stack, S. Sioncke*, J. Franco*, A. Vais*, V. Putcha**, L. Nyns*, A. Sibaja-Hernandez*, R. Rooyackers*, S. C. Ardila*, V. Spampinato*, A. Franquet*, J. W. Maes***, Q. Xie***, M. Givens****, F. Tang****, X. Jiang****, M. Heyns**, D. Linten*, J. Mitard*, A. Thean*****, D. Mocuta* and N. Collaert*, *imec, **also at KU Leuven, ***ASM Belgium, Belgium, ****ASM America, USA and *****currently at National Univ. of Singapore, Singapore

In this paper, we demonstrate for the first time an implant free $In_{0.53}Ga_{0.47}As$ n-MOSFET that meets the reliability target for advanced technology nodes with a max operating V_{ov} of 0.6V. In addition, an excellent electron mobility ($\mu_{eff,peak}$=3531 cm^2/V-s), low SS_{lin}=71mV/dec and an EOT of 1.15 nm were obtained. We also report the scaling potential of this stack to 1nm EOT without loss of performance, reliability and further reduction of the sub-threshold swing (SS_{lin}=68mV/dec). On top of the novel IL we presented last year, in this paper we insert a $LaSiO_x$ layer between the IL and HfO_2 offering an increased chemical stability of the gate stack. This combination is key and offers both an improved interface quality as well as a reduction of the oxide trap density.

T3-4 - 15:15
High Performance and Low Leakage Current InGaAs-on-Silicon FinFETs with 20 nm Gate Length, X. Sun*, C. D'Emic*, C.-W. Cheng*, A. Majumdar*, Y. Sun*, E. Cartier*, R. L. Bruce*, M. Frank*, H. Miyazoe*, K.-T. Shiu*, S. Lee**, J. Rozen*, J. Patel*, T. Ando*, W.-B. Song**, M. Lofaro*, M. Krishnan*, B. Obrodovic***, K.-T. Lee*, H. Tsai*, W.-E. Wang***, W. Spratt*, K. Chan*, S. Lee*, J.-B. Yau*, P. Hashemi*, M. Khojasteh*, M. Cantoro**, J. Ott*, T. Rakshit***, Y. Zhu*, D. Sadana*, C.-C. Yeh*, V. Narayanan*, R. T. Mo*, Y.-C. Heo**, D.-W. Kim**, M. S. Rodder*** and E. Leobandung*, *IBM T. J. Watson Research Center, USA, **Samsung Electronics Co., Ltd., Korea and ***Samsung Advanced Logic Lab, USA

We report the fabrication of short-channel FinFETs on InGaAs-on-silicon wafers using the aspect ratio trapping (ART) technique. We demonstrate excellent short-channel control down to 20 nm gate length due to scaled fin width down to 9 nm and reduction of parasitic bipolar effect (PBE). PBE that plagues III-V NFETs with gate-all-around (GAA) or III-V-on-insulator (III-V-OI) structures can be significantly suppressed by optimized ART FinFET technology. We demonstrate record high on-current I_{ON} and low drain leakage current for short gate lengths in the 20-32 nm range for InGaAs-on-silicon NFETs.

SESSION 4

Technology Focus Session - 1D and 2D Atomic Thin Materials and Devices [Shunju II, III]

Tuesday, June 6, 16:00-17:40

Chairpersons: K. Uchida, Keio Univ.
T. Palacios, MIT

T4-1 - 16:00 (Invited)
Scaling, Stacking, and Printing: How 1D and 2D Nanomaterials still Hold Promise for a New Era of Electronics, A. D. Franklin, Duke Univ., USA

1D and 2D nanomaterials continue to show promise for use in electronic devices. Their atomically thin size and superb transport properties make them of great value for transistors *scaled* in size and, more importantly, in voltage. Meanwhile, their substrate independence and van der Waals nature allows for ready *stacking* of nanomaterials at the device (interdigitated channels) or chip (monolithic 3D integrated) level. Finally, with dispersion into solution-phase inks, nanomaterials can be *printed* into thin-film devices for a new era of low-cost, flexible electronics that outperform competing printable materials. Each of these areas—scaling, stacking, and printing—benefit from uniquely from nanomaterials and will be reviewed herein.

T4-2 - 16:25 (Invited)
One and Two Dimensional Nanocarbon Materials for Innovative Functional Devices, S. Sato, Fujitsu Laboratories Ltd. and Fujitsu Ltd., Japan

One and two dimensional nanocarbon (NC) materials, including carbon nanotubes (CNTs), graphene and graphene nanoribbons (GNRs) have excellent properties and can therefore be building blocks of future electronic devices. It has been predicted and demonstrated that transistor channels and interconnects (More Moore devices) made of NC materials have excellent properties. NC-based Beyond CMOS and More than Moore (MtM) devices have also been proposed and demonstrated. In this paper, we briefly review some of MtM or functional devices using NC materials, which include terahertz (THz) wave detectors, strain sensors, and gas sensors. A novel gas sensor based on a graphene-gate transistor we have recently developed is also described.

T4-3 - 16:50
Experimental Demonstration of Electrically-Tunable Bandgap on 2D Black Phosphorus by Quantum Confined Stark Effect, L. Yang*, Y.-M. Lin**, W. Tsai** and P. D. Ye*, *Purdue Univ., USA and **TSMC, Taiwan

We report that the bandgap of 2D few layer black phosphorus (BP) can be electrically tuned by applying a perpendicular electric/displacement field. The variation of bandgap is as large as 200 meV with 2V/nm displacement field. The bandgap modulation can be understood with the quantum confined stark effect within the SiO2/BP/boron nitride (BN) sandwiched structure. This unique material property provides a new route to design and fabricate novel electronic and photonic devices based on black phosphorus

T4-4 - 17:15
Statistical Analyses of Random Telegraph Noise Amplitude in Ultra-Narrow (Deep Sub-10nm) Silicon Nanowire Transistors, H. Qiu*, K. Takeuchi*, T. Mizutani*, T. Saraya*, J. Chen**, M. Kobayashi* and T. Hiramoto*, *The Univ. of Tokyo, Japan and **Shandong Univ., China

Size dependence of random telegraph noise (RTN) in ultra-narrow silicon nanowire transistors with width far less than 10nm is experimentally measured and statistically analyzed for the first time. Single-trap RTN amplitude shows nearly exponential distributions, which reaches 170mV at 1.8% quantile for the narrowest transistor. The origins of long tail distributions and strong size dependence are discussed.

SESSION 5

Hetero Integration [Shunju I]

Tuesday, June 6, 16:00-17:40

Chairpersons: T. Tanaka, Tohoku Univ.
N. Collaert, imec

T5-1 - 16:00
Wafer Level Integration of an Advanced Logic-Memory System Through 2nd Generation CoWoS® Technology, W. C. Chen, C. Hu, K. C. Ting, V. Wei, T. H. Yu, S. Y. Huang, V. C. Y. Chang, C. T. Wang, S. Y. Hou, C. H. Wu and D. Yu, TSMC, Taiwan

State-of-the-art silicon interposer technology of chip-on-wafer-on-substrate (CoWoS®) has been applied for the first time in fabricating high performance wafer level system-in-package (WLSiP) containing the 2nd-generation high bandwidth memory (HBM2). An ultra-large Si interposer up to 1200 mm^2 made by a two-mask stitching process is used to form the basis of the 2nd-generation CoWoS® (CoWoS®-2) to accommodate chips of logic and memory to achieve the highest possible performance. Yield challenges associated with the high warpage of such a large heterogeneous system are resolved to achieve high package yield. Compared to alternative interposer integration approach such as chip-on-substrate first (CoS-1st), CoWoS® offers more competitive design rule to result in better power consumption, transmission loss, and eye diagram. CoWoS®-2 has positioned itself as a flexible 3D IC platform for logic-memory heterogeneous integration between logic SoC and HBM for various high performance computing applications.

T5-2 - 16:25
Enabling Low Power and High Speed OEICs: First Monolithic Integration of InGaAs n-FETs and Lasers on Si Substrate, A. Kumar*, S.-Y. Lee**, S. Yadav*, K. H. Tan**, W. K. Loke**, D. Li**, S. Wicaksono**, G. Liang*, S.-F. Yoon**, X. Gong*, D. Antoniadis*** and Y.-C. Yeo*, *National Univ. of Singapore, **Nanyang Technological Univ., Singapore and ***Massachusetts Institute of Technology, USA

The first monolithic integration of InGaAs channel transistors with lasers on a Si substrate is reported, achieving a milestone in the direction of enabling low power and high speed opto-electronic integrated circuits. The III-V layers for realizing transistors and lasers were grown epitaxially on the Si substrate using MBE. InGaAs n-FETs with I_{on}/I_{off} ratio of more than 6 orders and very low off-state leakage current were realized. In addition, fabrication process with a low overall processing temperature (≤ 400 °C) was used to realize electrically-pumped GaAs/AlGaAs quantum well lasers with a lasing wavelength of 795 nm and a linewidth of less than 0.5 nm at room temperature.

T5-3 - 16:50
Enhancement-Mode N-Channel TFT and Room-Temperature Near-Infrared Emission Based on n^+/p Junction in Single-Crystalline GeSn on Transparent Substrate, H. Oka, M. Koyama, T. Hosoi, T. Shimura and H. Watanabe, Osaka Univ., Japan

We demonstrated an integration of enhancement-mode single-crystalline n-channel thin-film transistor (TFT) and n^+/p diodes for light detection/emission based on the single-crystalline GeSn alloy grown on a transparent substrate. Owing to the excellent crystal quality of GeSn layer and a high-quality n^+/p junction, a record-high electron mobility of 271 cm^2/Vs and a room-temperature near-infrared electroluminescence (EL) were achieved. The present technology will offer an ideal platform for future GeSn-based optoelectronic integration.

T5-4 - 17:15
High V_{th} Enhancement Mode GaN Power Devices with High $I_{D,max}$ Using Hybrid Ferroelectric Charge Trap Gate Stack, C. H. Wu*, S. C. Liu*, C. K. Huang*, Y. C. Chiu*, P. C. Han**, P. C. Chang*, F. Lumbantoruan*, C. A. Lin*, Y. K. Lin*, C. Y. Chang*, C. Hu***, H. Iwai*,** and E. Y. Chang*, *National Chiao Tung Univ., Taiwan, **Tokyo Institute of Technology, Japan and ***Univ. of California, Berkeley, USA

In this work, we demonstrate a new concept for realizing high threshold voltage (V_{th}) E-mode GaN power devices with high maximum drain current ($I_{D,max}$). A gate stack ferroelectric blocking film with charge trap layer, achieved a large positive shift of V_{th}. The E-mode GaN MIS-HEMTs with high V_{th} of 6 V shows $I_{D,max}$ 720 mA/mm. The breakdown voltage is above 1100 V.

IEEE SSCS Young Professional Mentoring Event [Suzaku I]

Tuesday, June 6, 18:15-19:30

Symposium on VLSI Circuits

30th Anniversary Celebration [Suzaku II, III]

Tuesday, June 6, 19:30-20:00

Alcoholic and Non-Alcoholic beverages will be served.

Both Technology/Circuits Symposia attendees are cordially invited.

Technology / Circuits Joint Evening Panel Discussion

How will We Survive the Post-Scaling Era? [Shunju II, III]

Tuesday, June 6, 20:00-21:30

Organizers: S. Nimmagadda, Intel Technology India Pvt Ltd.
T. Tsunomura, Tokyo Electron Ltd.
C. Mazure, Soitec Group

Moderator: T. Letavic, GLOBALFOUNDRIES

Panelists: R. Moore, ARM Ltd.
J. Burns, IBM
Y. Jeon, Samsung Electronics Co., Ltd.
F. Boeuf, The Univ. of Tokyo
J. Ryckaert, imec

For many decades the semiconductor industry has enjoyed the benefits of scaling. Every 2 years or so a new process node would arrive, bringing with it reduced area, along with improved performance and power. In recent years, we have seen and overcome many challenges to the scaling model, necessitating considerable efforts in VLSI circuits and technology. While we have largely maintained area scaling, obtaining even modest node-to-node improvements in performance and power has been difficult.
New applications require much higher level compute than ever before which we are aiming to do via accelerators, programmable fabrics etc. These implementations respond very well with technology scaling.
However, we are now approaching the biggest challenge yet. What happens when scaling slows to the point that it has, for practical purposes, stopped? How will we survive the post-scaling era? Our panel of experts, spanning VLSI technology, circuits, and business, looks at the difficulties ahead and potential ways forward.

Technology Evening Panel Discussion

Transistor Future; How Does It Evolve after FinFET Era? [Shunju I]

Tuesday, June 6, 20:00-21:30

Organizers: T. Tsunomura, Tokyo Electron Ltd.
C. Mazure, Soitec Group

Moderators: J. Woo, Univ. of California, Los Angeles

Panelists: D. McCann, GLOBALFOUNDRIES
C. Chidambaram, Qualcomm Inc.
D. Mocuta, imec
H. Bu, IBM
I. Radu, Soitec

The FINFET has become widely used for nodes below 16nm. Its introduction in the manufacturing world has extended scalability of transistor dimensions. Beyond 5nm it is uncertain if the benefits of a FINFET structure will be maintained or lost. Alternative MOSFET structures may emerge to secure scaling. Nanosheet or nanowire have the potential to suppress short channel effect but these devices have an issue in enhancing on-state current without stacking multiple nanosheets or nanowires. Another approach is scaling channel thickness toward atomic scale. 2D materials like transition metal di-chalcogenide, black phosphorus are extensively studied. Synthesized 2D materials with single crystal structure has not been realized, and electrical characteristic are still poor compared with latest Si channel FET.
Although electrical characteristicsare improved with alternative transistor structures, size scaling will approach physical limitation. Adopting 3D structures is one of ways to maintain “equivalent size scaling”. NAND flash already uses this approach by transferring from 2D NAND to 3D NAND. Does this strategy work well in case of logic devices? There are many issues in 3D logic.
Overlay between different layers, choice of FET structure (lateral, vertical), Joule heating during operation, and cost / area merit.
In this panel discussion, future roadmap of FET will be discussed by 1D, 2D, and 3D FET experts.

SESSION 6

Highlight [Shunju I, II, III]

Wednesday, June 7, 8:30-10:10

Chairpersons: Y.-C. Yeo, TSMC
W. Rachmady, Intel Corp.

T6-1 - 8:30
Highly Manufacturable 7nm FinFET Technology Featuring EUV Lithography for Low Power and High Performance Applications, D. Ha, C. Yang, J. Lee, S. Lee, S. H. Lee, K.-I. Seo, H. S. Oh, E. C. Hwang, S. W. Do, S. C. Park, M.-C. Sun, D. H. Kim, J. H. Lee, M. I. Kang, S.-S. Ha, D. Y. Choi, H. Jun, H. J. Shin, Y. J. Kim, J. Lee, C. W. Moon, Y. W. Cho, S. H. Park, Y. Son, J. Y. Park, B. C. Lee, C. Kim, Y. M. Oh, J. S. Park, S. S. Kim, M. C. Kim, K. H. Hwang, S. W. Nam, S. Maeda, D.-W. Kim, J.-H. Lee, M. S. Liang and E. S. Jung, Samsung Electronics Co., Ltd., Korea

7nm CMOS FinFET technology featuring EUV lithography, 4th gen. dual Fin and 2nd gen. multi-eWF gate stack is presented, providing 20% faster speed or consuming 35% less total power over 10nm technology. EUV lithography, fully applied to MOL contacts and minimum-pitched metal/via interconnects, can reduce >25% mask steps with higher fidelity and smaller CD variation. A_{VT} of 6T HD SRAM cell are 1.29 for PD (PG) and 1.34 for PU, respectively.

T6-2 - 8:55
10nm High Performance Mobile SoC Design and Technology Co-Developed for Performance, Power, and Area Scaling, S. Yang*, Y. Liu*, M. Cai*, J. Bao*, P. Feng*, X. Chen*, L. Ge*, J. Yuan*, J. Choi*, P. Liu*, Y. Suh*, H. Wang*, J. Deng*, Y. Gao*, J. Yang*, X.-Y. Wang*, D. Yang*, J. Zhu*, P. Penzes*, S. C. Song*, C. Park**, S. Kim**, J. Kim**, S. Kang**, E. Terzioglu*, K. Rim* and P. C. Chidambaram*, *Qualcomm Technologies Inc., USA and **Samsung Electronics Co., Ltd., Korea

The industry’s first 10nm low power high performance mobile SoC has been successfully ramped in production. Thanks to a thorough design-technology co-development, 10nm SoC is 16% faster, 37% smaller, and 30% lower power than its 14nm predecessor. The latest SoC features a gigabit class modem and is set to advance AR/VR, AI, machine learning, and computing. 10nm FinFet technology scaling challenges such as sharply increased wiring resistance and variation and strong layout stress effects are discussed to illustrate design and technology co-development from technology definition to product ramp stage is imperative to realize scaling entitlements.

T6-3 - 9:20
First Demonstration of Flash RRAM on Pure CMOS Logic 14nm FinFET Platform Featuring Excellent Immunity to Sneak-Path and MLC Capability, E. R. Hsieh*, Y. C. Kuo**, C. H. Cheng*, J. L. Kuo*, M. R. Jiang*, J. L. Lin*, H. W. Cheng*, S. S. Chung*, C. H. Liu**, T. P. Chen***, Y. H. Yeah***, T. J. Chen*** and O. Cheng***, *National Chiao Tung Univ., **National Taiwan Normal Univ. and ***United Microelectronics Corp., Taiwan

For the first time, the ion-vacancy-based bipolar RRAM has been demonstrated on HKMG stack of FEOL logic 14nm FinFET. A unit cell with two identical FinFETs, one serves as a control transistor and the other one is the storage with resistance switching. It is performed by the edge tunneling and with bipolar switching. More importantly, the sneak path issue in an AND-type array based on this FinFET unit cell has been thoroughly investigated. To solve sneak path issue, a new active-fin-isolation (AFI) of FinFET in an AND-type array was proposed. This new AFI effectively increases the S/N margin of 10^3 and significantly reduces the standby power of 30% and active power of 99%, compared to original AND-type array. This work provides a promising candidate for the embedded FLASH memory on FinFET platform featuring fully-CMOS compatible integration and low cost solution in the more-than-Moore era.

T6-4 - 9:45
First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-Layer Contacts, V. Deshpande*, H. Hahn*, E. O'Connor*, Y. Baumgartner*, M. Sousa*, D. Caimi*, H. Boutry**, J. Widiez**, L. Brévard**, C. Le Royer**, M. Vinet**, J. Fompeyrine* and L. Czornomaz*, *IBM Research, Switzerland and **CEA-LETI, France

We demonstrate, for the first time, the 3D Monolithic (3DM) integration of In0.53GaAs nFETs on FDSOI Si CMOS featuring short-channel Replacement Metal Gate (RMG) InGaAs n-FinFETs on the top layer and Gate-First Si CMOS on the bottom layer with TiN/W inter-layer contacts. State-of-the-art device integration is achieved with the top layer InGaAs utilizing raised source drain (RSD) and the bottom layer CMOS having Si RSD for nFETs, SiGe RSD for pFETs, implants, silicide and TiN/W plug contacts. The top layer InGaAs n-FinFETs are scaled down to L_g =25 nm and both the Si nFETs and pFETs in the bottom layer are scaled down to L_g ~15 nm. Finally, utilizing the inter-layer contacts, we demonstrate a densely integrated 3D 6T-SRAM circuit with InGaAs nFETs stacked on top of Si pFETs showing considerable area reduction with respect to a 2D layout.

Technology / Circuits Joint Focus Session 1

Emerging Reliability Solutions [Suzaku III]

Wednesday, June 7, 10:30-12:35

Chairpersons: M. Yamaoka, Hitachi, Ltd.
E. Wang, Intel Corp.

JFS1-1 - 10:30
An Adaptive Clocking Control Circuit with 7.5% Frequency Gain for SPARC Processors, T. Hashimoto*, Y. Kawabe*, M. Hara**, Y. Kakimura**, K. Tajiri**, S. Shirota**, R. Nishiyama**, H. Sakurai**, H. Okano**, Y. Tomita*, S. Satoh** and H. Yamashita**, *Fujitsu Laboratories Ltd. and **Fujitsu Ltd., Japan

This paper presents an adaptive clocking control circuit to mitigate the processor performance degradation due to on-die supply voltage droops. The circuit utilizes multi-path TDC to reduce quantization errors and thermometer code-based data processing to eliminate latches, which shortens frequency modulation latency. This results in faster frequency/supply tracking. A test chip including the adaptive clocking control circuit with SPARC processor cores was fabricated in a 20-nm CMOS process. Experimental measurements demonstrated that the adaptive clocking control circuit achieved the state-of-the-art frequency gain of 7.5%, resulting in the operating frequency as high as 5 GHz.

JFS1-2 - 10:55
Statistical Characterization of Radiation-Induced Pulse Waveforms and Flip-Flop Soft Errors in 14nm Tri-Gate CMOS Using a Back-Sampling Chain (BSC) Technique, S. Kumar*, M. Cho**, L. Everson*, H. Kim*, Q. Tang*, P. Mazanec*, P. Meinerzhagen**, A. Malavasi**, D. Lake**, C. Tokunaga**, H. Quinn***, M. Khellah**, J. Tschanz**, S. Borkar**, V. De** and C. H. Kim*, *Univ. of Minnesota, **Intel Corp. and ***Los Alamos National Laboratory, USA

A novel BSC circuit with tunable current starved buffers demonstrates higher sensitivity, scalability & accurate statistical characterization of radiation-induced SET pulse waveforms & flip-flop SER in 14nm tri-gate CMOS, thus enabling improved SER estimation & analysis for a range of supply voltages including NTV. Neutron beam tests confirm that the proposed BSC chain can characterize Single Event Transients (SETs), Single Event Upsets (SEUs), and Multi Bit Upsets (MBUs) with high precision, thereby, offering insight into logic and memory SER, and its dependence on various circuit parameters.

JFS1-3 - 11:20
F_{MAX} / V_{MIN} and Noise Margin Impacts of Aging on Domino Read, Static Write, and Retention of 8T 1R1W SRAM Arrays in 22nm High-k/Metal-Gate Tri-Gate CMOS, J. P. Kulkarni, C. Tokunaga, M. Cho, M. M. Khellah, J. W. Tschanz and V. K. De, Intel Corp., USA

In this paper, we demonstrate by direct measurements and statistical analysis, progressive aging impacts on F_{MAX} and noise margin of the precharge-evaluate domino read, V_{MIN} for differential static write (with write assist), and retention over the operational lifetime of a 14KB 1R1W 8T SRAM array implemented in 22nm high-k/metal-gate tri-gate CMOS.

JFS1-4 - 11:45
Excellent Reliability of Ferroelectric $HfZrO_x$ Free from Wake-Up and Fatigue Effects by NH_3 Plasma Treatment, K.-Y. Chen, P.-H. Chen and Y.-H. Wu, National Tsing Hua Univ., Taiwan

With TiN/ferroelectric-$HfZrO_x$ (HZO)/TiN capacitors as the platform, NH_3 plasma treatment was employed at different HZO/TiN interfaces to investigate the impact on reliability. HZO free from wake-up and fatigue effects up to 10^6 cycles (± 2.5 MV/cm, long pulses width of 1 ms) with high κ value of 29~30, low leakage current and $2P_r$ of 20.2 μC/cm² can be achieved by treatments at both top and bottom interfaces. It is a great advance for HfO_2-based FE and can be mainly attributed to significant reduction of oxygen vacancies (Vo) in HZO, especially treatment at bottom interface so that the interfacial TiO_xN_y which causes oxygen-deficient HZO is effectively suppressed. NH_3-treated HZO has been physically confirmed with fewer Vo (lower non-lattice oxygen by 7 %) that is beneficial to suppress pinned domain walls and generation of new Vo during cycling, eliminating wake-up and fatigue effects. Conspicuously mitigated fatigue is also maintained at 85 °C.

JFS1-5 - 12:10
A 10MHz 5-to-40V EMI-Regulated GaN Power Driver with Closed-Loop Adaptive Miller Plateau Sensing, Y. Chen, X. Ke and D. B. Ma, The Univ. of Texas at Dallas, USA

To optimize the classic design trade-off between EMI noise and power efficiency in GaN power drivers at 10MHz and beyond, a closed-loop adaptive Miller Plateau sensing (AMPS) technique is proposed. In order to mitigate long delays and low accuracy issues in conventional Miller Plateau (MP) sensing approaches, an emulated MP tracking (EMPT) technique is adopted to achieve instant MP start point sensing. An isolated negative voltage sensor is designed for the EMPT to avoid considerable leakage current and enhance reliability without increasing circuit complexity. A noise-isolated feedback link ensures the closed-loop regulation accuracy by blocking the switching noise between HV and LV operation domains. Fabricated in a 0.35μm BCD process, the design achieves EMI reduction of 19.23dBμV in Band B (<30MHz) and over 9dBμV in Band C/D (>30MHz).

SESSION 7

Memory 1 PCM ReRAM [Shunju II, III]

Wednesday, June 7, 10:30-12:10

Chairpersons: H. Miyake, Micron Memory Japan, Inc.
N. Ramaswamy, Micron Technology Inc.

T7-1 - 10:30
Reduction of Cycle-to-Cycle Variability in ReRAM by Filamentary Refresh, K. Ohmori*, A. Shinoda*, K. Kawai**, Z. Wei**, T. Mikawa** and R. Hasunuma*, *Univ. of Tsukuba and **Panasonic Semiconductor Solutions, Japan

In this paper, we clarify a filamentary "*refresh*" mechanism of a resistive random access memory (ReRAM) cell. Based on this mechanism, we propose an intentional refresh introduction that enables a reduction in the standard deviation (σ) of current values. The activation energy (E_A) associated with oxygen vacancies (V_os) in ReRAM was investigated using low-frequency-noise spectroscopy, revealing continuous variation of E_A.

T7-2 - 10:55
Thermally Stable Integrated Se-Based OTS Selectors with >20 MA/cm² Current Drive, >3.10³ Half-Bias Nonlinearity, Tunable Threshold Voltage and Excellent Endurance, B. Govoreanu*, G. L. Donadio*, K. Opsomer*, W. Devulder, V. V. Afanas'ev**, T. Witters*, S. Clima*, N. S. Avasarala**, A. Redolfi*, S. Kundu*, O. Richard*, D. Tsvetanova*, G. Pourtois*, C. Detavernier***, L. Goux* and G. S. Kar*, *imec, **KU Leuven and ***Ghent Univ., Belgium

We report on novel integrated Se-based Ovonic Threshold Switching selector devices, with sizes down to 50nm, which can be operated reliably at high drive current densities, exceeding 20MA/cm², and have high half-bias nonlinearity exceeding well 10^3. We show functional devices after a thermal budget of 350°C. Their electrical properties are tunable by careful control of the Ge_xSe_{1-x} films composition, thickness or process condition.

T7-3 - 11:20
Innovative PCM+OTS Device with High Sub-Threshold Non-Linearity for Non-Switching Reading Operations and Higher Endurance Performance, G. Navarro, A. Verdy, N. Castellani, G. Bourgeois, V. Sousa, G. Molas, M. Bernard, C. Sabbione, P. Noé, J. Garrione, L. Fellouh and L. Perniola, CEA-LETI, France

In this paper we present the engineering of a non-volatile 1S1R memory based on a Phase-Change Memory cell (PCM), consisting in a GeN/$Ge_2Sb_2Te_5$ layer, stacked with a GeSe-based Ovonic Threshold Switching selector device (OTS). We optimize and analyze separately the two devices, and we propose for the first time an innovative reading strategy of the cross point device, enabled by the improved sub-threshold non-linearity of the OTS selector. A new memory concept is presented and demonstrated in which selector switching is performed only for SET and RESET programming operations and reading is operated without switching the OTS selector, strategy that allows to target outstanding endurances.

T7-4 - 11:45
A Novel Write Method for Improving RESET Distribution of PRAM, H. K. Park, K. W. Lee, S. H. Song, K. G. Lee, J. H. Shin, V. Gangasani, Y. S. Shin, D. H. Kang, J. H. Park, K. W. Song, G. H. Koh, G. T. Jeong, K. T. Park and K. H. Kyung, Samsung Electronics Co., Ltd., Korea

RESET distribution of phase-change random access memory (PRAM) is highly related to heat fluctuations during RESET write ($RESET_W$). In this work we investigate the effect of load resistance (R_L) with constant voltage write method and propose new $RESET_W$ method with an optimal R_L selection equation with considering Joule heating and thermoelectric effects. Since the optimal R_L compensates for intrinsic dynamic resistance variation in PRAM, the heat fluctuation is reduced and the RESET distribution is improved. With fabricated PRAM TEG, we verify that optimal R_L exists and achieve more improved RESET distribution with the optimized R_L by 41% than with R_L not optimized.

SESSION 8

Sensing [Shunju I]

Wednesday, June 7, 10:30-12:10

Chairpersons: N. Sugii, Hitachi, Ltd.
L. Selmi, Univ. of Udine

T8-1 - 10:30
Towards A Fully Integrated, Wirelessly Powered, and Ordinarily Equipped On-Lens System for Successive Dry Eye Syndrome Diagnosis, J.-C. Chiou, S.-H. Hsu, Y.-C. Huang, G.-T. Yeh, K.-S. Dai and C.-K. Kuei, National Chiao Tung Univ., Taiwan

This paper presents a smart contact lens (SCL) sensor system for successive evaluation of tear evaporation. The proposed SCL system integrated with 3D technology is composed of tunable sensitivity sensor-readout circuitry, a tear sensor, and an antenna, and is embedded into a biocompatible hydrogel-based contact lens by a commercial manufacturing process. Moreover, the on-lens system can be addressed using commercial radio-frequency identification (RFID) reader devices for sensor control and data communication. Subjects can wear the SCL for continuous tear-content monitoring. Furthermore, the recordings from the device can provide high distinguishability in different tear phantoms using a variation of capacitance or resistance rather than using the weight loss.

T8-2 - 10:55
A Powerless and Non-Volatile Counterfeit IC Detection Sensor in a Standard Logic Process Based on an Exposed Floating-Gate Array, M. Liu and C. H. Kim, Univ. of Minnesota, USA

Counterfeit ICs pose a threat to designing secure and reliable electronic systems, like IoT systems where security is of utmost importance. To better detect and prevent counterfeit ICs from entering the supply chain, an eflash based powerless non-volatile sensor using floating-gate (FG) technology is demonstrated in a 0.35μm standard logic process. By exposing the FG to the environment, the proposed sensor can record any physical tamper attempt affecting the charge stored on the exposed FG. Test results confirm that anomalous events such as temperature spikes, humidity changes, or increased dust particle density can be recorded by the sensor powerlessly, and later read out and analyzed whenever the power is available.

T8-3 - 11:20
An All Pixel PDAF CMOS Image Sensor with 0.64μm×1.28μm Photodiode Separated by Self-Aligned In-Pixel Deep Trench Isolation for High AF Performance, S. Choi, K. Lee, J. Yun, S. Choi, S. Lee, J. Park, E. S. Shim, J. Pyo, B. Kim, M. Jung, Y. Lee, K. Son, S. Jung, T.-S. Wang, Y. Choi, D.-K. Min, J. Im, C.-R. Moon, D. Lee and D. Chang, Samsung Electronics Co., Ltd., Korea

We present a CMOS image sensor (CIS) with phase detection auto-focus (PDAF) in all pixels. The size of photodiode (PD) is 0.64μm by 1.28μm, the smallest ever reported and two PDs compose a single pixel. Inter PD isolation was fabricated by deep trench isolation (DTI) process in order to obtain an accurate AF performance. The layout and depth of DTI was optimized in order to eliminate side effects and maximize the performance even at extremely low light condition up to 1lux. In particular the AF performance remains comparable to that of 0.70μm dual PD CIS. By using our unique technology, it seems plausible to scale further down the size of pixels in dual PD CIS without sacrificing AF performance.

T8-4 - 11:45
FET-Type Hydrogen Sensor with Short Response Time and High Drift Immunity, Y. Sasago, H. Nakamura, Y. Anzai, T. Moritsuka, T. Odaka and T. Usagawa, Hitachi, Ltd., Japan

New methods were studied to reduce response time and threshold voltage drift of the FET-type hydrogen sensor. The advantages of the Pt-Ti-O gate over other sensor gate materials were demonstrated. Extending Langmuir's dissociative ad-sorption theory to non-equilibrium states enabled us to reduce the response time, and the negative gate bias operation with P-FET-type sensor reduced the drift. Thus, we successfully achieved both a response time of 0.8 s and high drift immunity.

Technology / Circuits Joint Focus Session 2

Advanced Assembly [Suzaku III]

Wednesday, June 7, 14:00-15:40

Chairpersons: N. Miura, Kobe Univ.
B. Calhoun, Univ. of Virginia

JFS2-1 - 14:00
A Digitally Controlled Fully Integrated Voltage Regulator with 3D-TSV Based On-Die Solenoid Inductor with Backside Planar Magnetic Core in 14nm Tri-Gate CMOS, H. K. Krishnamurthy, S. Weng, G. E. Matthew, R. Saraswat, K. Ravichandran, J. Tschanz and V. De, Intel Corp., USA

A fully integrated digitally controlled buck VR, featuring hysteretic and PFM control for maximum light load efficiency, with 3D-TSV based on-die solenoid inductor with backside planar magnetic core in 14nm tri-gate CMOS demonstrates 111 nH/mm^2 inductance density & 80% conversion efficiency.

JFS2-2 - 14:25
A 6Gb/s Rotatable Non-Contact Connector with High-Speed/I²C/CAN/SPI Interface Bridge IC, M. Haraguchi*, A. Kosuge*, T. Igarashi**, S. Masaki**, M. Sueda**, M. Hamada* and T. Kuroda*, *Keio Univ. and **Socionext Inc., Japan

A 6Gb/s 9.8pJ/b rotatable non-contact connector applicable to robot arms is developed. The proposed rotatable transmission line coupler (RTLC) has a wide bandwidth at all rotation angles. An interface bridge IC is also developed to transfer a wide range of interface signals from slow legacy ones to high-speed ones. The proposed system improves power efficiency by a factor of 3.7, space efficiency by a factor of 1.8, and satisfies EMC regulations.

JFS2-3 - 14:50
High Density 3D Fanout Package for Heterogeneous Integration, S.-P. Jeng, S. M. Chen, F. C. Hsu, P. Y. Lin, J. H. Wang, T. J. Fang, P. Kavle and Y. J. Lin, TSMC, Taiwan

Three-dimensional (3D) fanout package stacking offers new levels of performance, high-density integration, and form factor advantages. Known-good fanout packages are stacked, and the vertical connection is built through Cu pillars in the molding area and solder bumps. Compared to existing TSV-based 3D integrated circuits (3DIC) technology, this solution reduces thermal crosstalk when integrating devices of different die sizes. Fanout package stacking potentially provides a cost-effective platform for highly flexible heterogeneous integration of digital, memory, analog, radio-frequency (RF) and optical devices.

JFS2-4 - 15:15
A Shutter-Less Micro-Bolometer Thermal Imaging System Using Multiple Digital Correlated Double Sampling for Mobile Applications, S. Park*, T. Cho*, M. Kim*, H. Park** and K. Lee*, *KAIST and **Seoul National Univ. of Science and Technology, Korea

A micro-bolometer focal plane array (MBFPA)-based long wavelength Infra-red thermal imaging sensor is presented. The proposed multiple digital correlated double sampling (MD-CDS) readout method employing newly designed reference-cell greatly reduces PVT variation-induced fixed pattern noise (FPN) and as a result features much relaxed calibration process, easier TEC-less operation and Shutter-less operation. The readout IC and MBFPA was fabricated in 0.35um CMOS and amorphous silicon MEMS process respectively. The fabricated MBFPA thermal imaging sensor has NETD performance of 0.1 kelvin even though the mechanical shutter is not used.

SESSION 9

SiGe/Ge FET 1 [Shunju II, III]

Wednesday, June 7, 14:00-15:40

Chairpersons: H. Morioka, Socionext Inc.
V. Narayanan, IBM

T9-1 - 14:00
High Performance and Record Subthreshold Swing Demonstration in Scaled RMG SiGe FinFETs with High-Ge-Content Channels Formed by 3D Condensation and a Novel Gate Stack Process, P. Hashemi, T. Ando, S. Koswatta, K.-L. Lee, E. Cartier, J. A. Ott, C.-H. Lee, J. Bruley, M. F. Lofaro, S. Dawes, K. K. Chan, S. U. Engelmann, E. Leobandung, V. Narayanan and R. T. Mo, IBM Research, USA

We demonstrate scaled high-Ge-content (HGC) strained SiGe pMOS FinFETs with very high short channel (SC) performance using a Replacement High-K/Metal Gate (RMG) flow, for the first time. A novel RMG gate stack process was introduced to create Ge-free interface-layer (IL) with excellent reliability and sub-threshold swing (SS) as low as 62mV/dec, the best reported to date for Si-cap-free SiGe FinFETs. We also present some structural details of the gate stack, for the first time. Short channel characteristics of HGC SiGe FinFETs have also been studied for various fin widths. Compared to our earlier RMG work, improved I/I free process with ultra-thin spacers has led to considerable R_{on} and R_{ext} reduction. As a result, we have demonstrated very high SiGe performance with I_{on}=0.45mA/μm at I_{off}=100nA/μm at V_{DD}=0.5V for L_G=25nm, matching our record for gate-first SiGe FinFETs and outperforming the gate-first results at such L_G.

T9-2 - 14:25
SiGe FinFET for Practical Logic Libraries by Mitigating Local Layout Effect, G. Tsutsui*, H. Zhou*, A. Greene*, R. Robison*, J. Yang*, J. Li*, C. Prindle**, J. R. Sporre*, E. R. Miller*, D. Liu*, R. Sporer**, B. Mulfinger**, T. McArdle**, J. Cho**, G. Karve*, F. L. Lie*, S. Kanakasabapathy*, R. Carter**, D. Gupta*, A. Knorr**, D. Guo* and H. Bu*, *IBM Research and **GLOBALFOUNDRIES, USA

SiGe FinFET has been explored for its benefit of high current drivability provided by channel strain. We have demonstrated SiGe CMOS FinFET at 10nm technology ground rules including epitaxial defectivity control, DC performance and reliability benefit. One concern of SiGe FinFET is channel strain relaxation by fin cut process inducing local layout effect (LLE), which is crucial for product design. In this paper, we thoroughly examined LLE in SiGe pFinFET and explored its mitigation techniques. Two techniques are proposed and demonstrated successful LLE mitigation, which drives forward SiGe FinFET insertion to technology.

T9-3 - 14:50
High Performance 4.5-nm-Thick Compressively-Strained Ge-On-Insulator pMOSFETs Fabricated by Ge Condensation with Optimized Temperature Control, W.-K. Kim, M. Takenaka and S. Takagi, The Univ. of Tokyo, Japan

We report high performance extremely-thin-body (ETB) Ge-on-Insulator (GOI) pMOSFETs fabricated by a new Ge condensation process with minimized temperature cycles and slow cooling-down rate. This new condensation process effectively suppresses strain relaxation during Ge condensation and creates high compressive strain. By combining the highly-strained GOI substrates with a digital etching process, we successfully realized 4.5-nm-thick strained-GOI pMOSFETs with excellent GOI thickness uniformity. The MOSFETs exhibit record high hole mobility of 138 cm^2/Vs in sub 5-nm GOI thickness with enhancement factor of 2.0 over that of best performance GOI pMOSFETs in this thickness range, that has been reported.

T9-4 - 15:15
Understanding the Interfacial Layer Formation on Strained $Si_{1-x}Ge_x$ Channels and Their Correlation to Inversion Layer Hole Mobility, C. H. Lee, R. G. Southwick III, R. Bao, S. Mochizuki, V. Paruchuri and H. Jagannathan, IBM Research, USA

We investigate the mechanism of interfacial layer formation on $Si_{1-x}Ge_x$ ($0 < x < 0.5$) channel and its correlation to hole mobility. It is found that the mobility degradation in low-Ge-content $Si_{1-x}Ge_x$ pFETs is attributed to a Ge-rich top surface in the channel directly induced by interfacial layer formation. In addition, the depth profile of a Si-rich top surface in high-Ge-content $Si_{1-x}Ge_x$ channel is presented to understand the surface atomic configuration of $Si_{1-x}Ge_x$ channel as well as mobility enhancement mechanism.

SESSION 10

Reliability [Shunju I]

Wednesday, June 7, 14:00-15:40

Chairpersons: S. Yamakawa, Sony Semiconductor Solutions Corp.
A. Ionescu, Swiss Federal Institute of Technology

T10-1 - 14:00
On-Die 16nm Metal Critical Peak Current Test Methodology with 100ps Pulse Width, Y.-T. Yang, W.-S. Chou, M.-H. Lin, P.-Z. Kang, A. S. Oates and Y.-C. Peng, TSMC, Taiwan

A new methodology to measure the product-like AC stress of metal critical peak current was implemented in 16nm High-K Metal Gate (HKMG) FINFET process. Traditional TLP tester can only generate minimum 1ns pulse width stress, which is still in thermal diffusion metal burn out regime. The proposed method can generate minimum pulse width of 100ps stress waveform through on-die tunable pulse-width generator and time-to-current duty detector circuits. The silicon data first demonstrated Cu critical peak current will enter the adiabatic regime under 100ps pulse width with 10X peak current than in thermal diffusion regime. This wafer-level measurable test vehicle can be put on scribe-line as Design-For-Manufacturing (DFM) DC-to-AC metal reliability monitor system.

T10-2 - 14:25
A Fully-Integrated Method for RTN Parameter Extraction, M. Simicic*,***, S. Morrison**,***, B. Parvais***, P. Weckx***, B. Kaczer***, K. Sawada****, H. Ammo****, S. Yamakawa****, K. Nomoto*****, M. Ohno*****, D. Linten***, D. Verkest***, P. Wambacq**,***, G. Groeseneken*,*** and G. Gielen*, *KU Leuven, **Vrije Universiteit Brussel, ***imec, Belgium, ****Sony Semiconductor Solutions Corp., Japan and *****Sony Semiconductor Solutions Corp. to imec, Belgium

A method for on-chip extraction of random telegraph noise (RTN) parameters from transistors is proposed. Exploiting the nature of exponential distributed RTN events, the proposed circuit enables the automatic extraction of mean RTN time constants from a large array of small-area transistors. The on-chip data processing provides a simplified measurement infrastructure, reduces the measurement time by parallelization and increased efficiency, reduces the data post-processing effort and extends the measurement frequency band. The methodology is demonstrated in a prototype chip fabricated in a 28nm High-k Metal Gate (HK/MG) CMOS technology. The 1.17 mm^2 chip includes two arrays of 18,144 transistors each, analog circuitry for sensing and digitizing the RTN signals and a digital signal processing block. The experimental results agree with expectations.

T10-3 - 14:50
New Insight on the Geometry Dependence of BTI in 3D Technologies Based on Experiments and Modeling, X. Garros*, A. Laurent*,**, S. Barraud*, J. Lacord*, O. Faynot*, G. Ghibaudo** and G. Reimbold*, *CEA-LETI and **IMEP-LAHC, France

In this paper we deeply investigate the dependence of BTI with transistor scaling. Unlike PBTI, NBTI is strongly enhanced in narrow devices like Nanowire or Finfet. We clearly prove by means of 3D electrostatic simulations that it is due to a defect density at the Sidewall (SW) of the transistor about 2.5 times higher than the one at the Top Surface (TS).

T10-4 - 15:15
Unified Self-Heating Effect Model for Advanced Digital and Analog Technology and Thermal-Aware Lifetime Prediction Methodology, H. Jiang*,**, L. Shen*, S. H. Shin**, N. Xu***, G. Du*, B.-Y. Nguyen****, O. Faynot*****, M. A. Alam**, X. Zhang* and X. Y. Liu*, *Peking Univ., China, **Purdue Univ., ***Univ. of California, Berkeley, ****Soitec, USA and *****CEA-LETI, France

Self-heating effect (SHE) has become a significant concern for device performance, variability and reliability co-optimization due to more confined layout geometry and lower-thermal-conductivity materials adopted in advanced transistor technology, which substantially impacts the integrated circuit (IC)'s design schemes. In this work, a new methodology for evaluation of SHE in both *digital* and *analog circuits* is demonstrated by using *pulse-aware* and existing *sine-aware analytical models* respectively. Correlating SHE to physics-based thermal-aware reliability models provides insights for design and sign-offs of advanced digital and analog ICs.

SESSION 11

CMOS Integration I [Shunju II, III]

Wednesday, June 7, 16:00-18:05

Chairpersons: T.-R. Yew, National Tsing-Hua Univ.
T. Skotnicki, STMicroelectronics

T11-1 - 16:00
14nm FinFET Technology for Analog and RF Applications, J. Singh, A. Bousquet, J. Ciavatti, K. Sundaram, J. S. Wong, K. W. Chew, A. Bandyopadhyay, S. Li, A. Bellaouar, S. M. Pandey, B. Zhu, A. Martin, C. Kyono, J.-S. Goo, H. S. Yang, A. Mehta, X. Zhang, O. Hu, S. Mahajan, E. Geiss, S. Yamaguchi, S. Mittal, R. Asra, P. Balasubramaniam, J. Watts, D. Harame, R. M. Todi, S. B. Samavedam and D. K. Sohn, GLOBALFOUNDRIES, USA

This paper highlights a 14nm Analog and RF technology based on a logic FinFET platform for the first time. An optimized RF device layout shows excellent F_t/F_{max} of (314GHz/180GHz) and (285GHz/140GHz) for NFET and PFET respectively. A higher PFET RF performance compared to 28nm technology is due to a source/drain stressor mobility improvement. A benefit of better FinFET channel electrostatics can be seen in the self-gain (G_m/G_{ds}), which shows a significant increase to 40 and 34 for NFET and PFET respectively. Superior 1/f noise of 17/35 $f(V^*\mu m)^2/Hz$ @ 1KHz for N/PFET respectively is also achieved. To extend further low voltage operation and power saving, ultra-low V_t devices are also developed. Furthermore, a deep N-well (triple well) process is introduced to improve the ultra-low signal immunity from substrate noise, while offering useful devices like VNPN and high breakdown voltage deep N-well diodes.

T11-2 - 16:25
High Performance 14nm FinFET Technology for Low Power Mobile RF Application, E.-Y. Jeong, M. Song, I. Choi, H. Shin, J. Song, W. Maeng, H. Park, H. Yoon, S. Kim, S. Park, B. H. You, H.-J. Cho, Y. C. An, S. K. Lee, S. D. Kwon and S.-M. Jung, Samsung Electronics Co., Ltd., Korea

RF-CMOS process employing 14nm FinFET technology is introduced for the first time and its RF performance is characterized. Compared with its 28nm planar counterpart, the optimized 14nm RF FinFET consumes 63% of DC power with 53% of device active area and 3.8 times higher intrinsic gain (gm/gds). Based on the 14 nm technology, VNCAP with higher cap density (8%) and Q-factor (23%) is also verified for mobile RF application.

T11-3 - 16:50
10nm 2nd Generation BEOL Technology with Optimized Illumination and LELELELE, W. C. Jeong, J. H. Ahn, Y. S. Bang, Y. S. Yoon, J. Y. Choi, Y. C. Kim, S. W. Paek, S. W. Ahn, B. S. Kim, T. J. Song, J. H. Jung, J. H. Do, S. M. Lim, H.-J. Cho, J. H. Lee, D. W. Kim, S. B. Kang, J.-H. Ku, S. D. Kwon, S.-M. Jung and J. S. Yoon, Samsung Electronics Co., Ltd., Korea

10nm 2nd generation BEOL technology is described with an optimized illumination system and multi-patterning lithography. While the optimized illumination system offered a possibility to pattern reduced metal pitches in the preferred orientation, difficulties of T-T and T-S patterning still remained. It was overcome by increasing the number of available multi-patterning colors from 2 to 4. First-ever implementation of LELELELE with tight inter-color misalignment control increased scalability up to 17.1% and was demonstrated with SRAM 128Mb yield.

T11-4 - 17:15
Trantenna: Monolithic Transistor-Antenna Device for Real-Time THz Imaging System, M. W. Ryu, R. Patel, S. H. Ahn, H. J. Jeon, M. S. Choe, E. Choi, K. J. Han and K. R. Kim, UNIST, Korea

We report a circular-shape monolithic transistor-antenna (trantenna) for high-performance plasmonic terahertz (THz) detector. By designing an asymmetric transistor on a ring-type metal-gate structure, more enhanced (45 times) channel charge asymmetry has been obtained in comparison with a bar-type asymmetric transistor of our previous work. In addition, by exploiting ring-type transistor itself as a monolithic circular patch antenna, which is designed for a 0.12-THz resonance frequency, we demonstrated the highly-enhanced responsivity (R_v) > 1 kV/W (x 5) and reduced noise-equivalent power (NEP) < 10 $pW/Hz^{0.5}$ (x 1/10).

T11-5 - 17:40 (Late News)
Comparison of Key Fine-Line BEOL Metallization Schemes for Beyond 7 nm Node, T. Nogami*, X. Zhang**, J. Kelly*, B. Briggs*, H. You**, R. Patlolla*, H. Huang*, P. McLaughlin*, J. Lee*, H. Shobha*, S. Nguyen*, S. DeVries*, J. Demarest*, G. Lian*, J. Li*, J. Maniscalco*, P. Bhosale*, X. Lin**, B. Peethala*, N. Lanzillo*, T. Kane*, C. C. Yang*, K. Motoyama*, D. Sil*, T. Spooner*, D. Canaperi*, T. Standaert*, S. Lian***, A. Grill*, D. Edelstein* and V. Paruchuri*, *IBM Research, **GLOBALFOUNDRIES, ***Samsung Electronics Inc., USA

For beyond 7 nm node BEOL, line resistance (R) is assessed among four metallization schemes: Ru; Co; Cu with TaN/Ru barrier, and Cu with through-cobalt self-forming barrier (tCoSFB) [1]. Line-R vs. linewidth of Cu fine wires with TaN/Ru barrier crosses over with barrier-less Ru and Co wires for beyond-7 nm node dimensions, whereas Cu with tCoSFB remains competitive, with the lowest line R for 7 nm and beyond. Our study suggests promise of this last scheme to meet requirements in line R and EM reliability.

SESSION 12

Ferroelectric [Shunju I]

Wednesday, June 7, 16:00-17:40

Chairpersons: B. H. Lee, Gwangju Institute of Science and Technology
S. Salahuddin, Univ. of California, Berkeley

T12-1 - 16:00
Nano-Scaled Ge FinFETs with Low Temperature Ferroelectric $HfZrO_x$ on Specific Interfacial Layers Exhibiting 65% S.S. Reduction and Improved I_{ON}, C.-J. Su*, Y.-T. Tang*, Y.-C. Tsou**, P.-J. Sung*,***, F.-J. Hou*, C.-J. Wang*, S.-T. Chung***, C.-Y. Hsieh****, Y.-S. Yeh*, F.-K. Hsueh*,***, K.-H. Kao**, S.-S. Chuang***, C.-T. Wu*, T.-Y. You*, Y.-L. Jian*, T.-H. Chou*, Y.-L. Shen*, B.-Y. Chen*, G.-L. Luo*, T.-C. Hong**, K.-P. Huang*****, M.-C. Chen*, Y.-J. Lee*, T.-S. Chao***, T.-Y. Tseng***, W.-F. Wu*, G.-W. Huang*, J.-M. Shieh*, W.-K. Yeh* and Y.-H. Wang**,******, *National Nano Device Laboratories, **National Cheng Kung Univ., ***National Chiao Tung Univ., ****National Sun Yat-Sen Univ., *****Industrial Technology Research Institute and ******National Applied Research Laboratories, Taiwan

Ge n- and p-FinFETs with different interfacial layer ferroelectric $HfZrO_x$ (IL-FE-HZO) gate stacks have been demonstrated systematically by various annealing conditions for the first time. Microwave annealing (MWA) not only shows enhanced FE characteristics but also suppresses the gate leakage and Ge interdiffusion compared with conventional rapid thermal annealing (RTA). While HZO on Al_2O_3 IL results in paraelectric behavior, HZO on GeO_x IL exhibits significant FE. High I_{ON}/I_{OFF} ($> 10^7$) and low subthreshold slope (S.S. ~ 58 mV/dec.) are demonstrated by a Ge nFinFET with a gate length (L_g) of 60 nm and a FE-HZO/GeO_x gate stack.

T12-2 - 16:25
Impact of Total and Partial Dipole Switching on the Switching Slope of Gate-Last Negative Capacitance FETs with Ferroelectric Hafnium Zirconium Oxide Gate Stack, P. Sharma*, K. Tapily**, A. K. Saha***, J. Zhang*, A. Shaughnessy*, A. Aziz***, G. L. Snider*, S. Gupta***, R. D. Clark** and S. Datta*, *Univ. of Notre Dame, **TEL Technology Centre, America and ***Penn State Univ., USA

We report, for the first time, a gate last process, used to fabricate Negative Capacitance field effect transistors (NCFETs) with $Hf_{0.5}Zr_{0.5}O_2$ (HZO) as ferroelectric (FE) dielectric in a metal/ferroelectric/insulator/semiconductor (MFIS) configuration. Long channel NCFET's with HZO thickness down to 5 nm exhibit consistent switching behavior with switching slope (SS_{rev}) below *kT/q* over four decades of drain current. Temperature dependent transport study shows that, the effective mobility of HZO NCFETs is 15 % higher than that of HfO_2 based control MOSFETs due to suppression of Hf diffusion into the interfacial SiO_2 layer (IL). Using the Preisach hysteresis model, which models dynamics of FE switching through a cluster of independent switching dipoles at arbitrary electric field, we (a) explain the asymmetric SS behavior of NCFETs in MFIS configuration, and (b) establish design guidelines for achieving sub-*kT/q* SS in both forward and reverse sweep direction.

T12-3 - 16:50
A Nonvolatile SRAM Integrated with Ferroelectric HfO_2 Capacitor for Normally-Off and Ultralow Power IoT Application, M. Kobayashi, N. Ueyama and T. Hiramoto, The Univ. of Tokyo, Japan

We have designed and fabricated a nonvolatile SRAM (NVSRAM) integrated with ferroelectric HfO_2 capacitor, and experimentally demonstrated its nonvolatile functionality, for the first time. Sub-10nm-thick ferroelectric HfO_2 capacitor shows excellent ferroelectricity and memory characteristics at low supply voltage. The NVSRAM with ferroelectric HfO_2 capacitor is capable of storing and recalling previous memory state before power shutdown, which is suitable for the intermittent operation of IoT devices with deep-sleep mode. The NVSRAM with ferroelectric HfO_2 capacitor can be a cost-effective, normally-off and ultralow power embedded memory solution.

T12-4 - 17:15
First Demonstration of Vertically Stacked Ferroelectric Al Doped HfO_2 Devices for NAND Applications, K. Florent*,**, S. Lavizzari**, L. Di Piazza**, M. Popovici**, E. Vecchio**, G. Potoms**, G. Groeseneken*,** and J. Van Houdt*,**, *KU Leuven and **imec, Belgium

A 3D ferroelectric Al doped HfO_2 device for NAND applications was fabricated for the first time. The polysilicon (poly-Si) channel, whose diameter ranges from 60 to 200 nm, was highly doped for a better understanding of the ferroelectric properties. Electrical results confirmed the presence of the ferroelectric phase with a coercive voltage (2Vc) of 6 V extracted from the hysteresis loop. The drain anneal was found to have a significant impact on HfO2 properties and needs to be reduced to preserve the ferroelectricity. Finally, reliability investigations showed an estimated time to failure of more than 10 years at 85 °C. This study lays the foundation for the fabrication of 3D ferroelectric field effect transistors (FeFET).

Technology / Circuits Joint Banquet [Shunju I, II, III]

Wednesday, June 7, 19:00-21:00

Technology / Circuits Joint Focus Session 3

Ultra Low Power for IoT [Shunju II, III]

Thursday, June 8, 8:30-10:10

Chairpersons: M. Tada, NEC Corp.
L. Bair, AMD

JFS3-1 - 8:30 (Invited)
Computing Platform for Automotive Electronics of Automated Driving Generation, H. Sugimoto, DENSO Corp., Japan

This paper addresses requirements from future automotive electronics system concept/design to computing technology or platform filling processing characteristics which will be used in applications of automated driving generation. We cannot completely predict future trends of functionality or application, so it is important to have flexible and scalable computing platform for that generation. The platform should also have a reasonable coverage of processing characteristics especially for parallelism point of view, because it will strongly affect to automotive electronics system efficiency and quality. Here, we'll mainly point to automotive unique processing characteristics which should be improved in near future.

JFS3-2 - 8:55 (Invited)
Semiconductor Platforms for Ultra Low Power IoT Solutions, T. Dry and T. Letavic, GLOBALFOUNDRIES, USA

Intelligent connected sensor and actuator endpoint nodes enable the Internet-of-Things (IoT). A brief overview of endpoint node functional blocks and requirements for low-power consumption are discussed. VLSI technology enablers for IoT include Ultra low Power (ULP) and Ultra Low Leakage (ULL) semiconductor process platform extensions. ULP and ULL implementations for bulk silicon technologies are presented and compared to fully-depleted silicon-on-insulator (FDSOI) technology. FDSOI utilizes Back Bias (BB) to improve performance and achieve the lowest dynamic and static power, enabling cost-effective low-power IoT applications.

JFS3-3 - 9:20
Performance Boost of Crystalline In-Ga-Zn-O Material and Transistor with Extremely Low Leakage for IoT Normally-Off CPU Application, S. H. Wu*, X. Y. Jia*, X. Li*, C. C. Shuai*, H. C. Lin*, M. C. Lu*, T. H. Wu*, M. Y. Liu*, J. Y. Wu*, D. Matsubayashi**, K. Kato** and S. Yamazaki**, *United Microelectronics Corporation, Singapore and **Semiconductor Energy Laboratory Co., Ltd., Japan

The worldwide first 100MHz dynamic oxide semiconductor RAM (DOSRAM) is successfully demonstrated using a new high-mobility crystalline In-Ga-Zn-O (IGZO) material. The new IGZO exhibits around two times carrier mobility of conventional IGZO, while still achieving an extremely low off-state leakage (I_{off}) at ~10^{-21}A (zA) level. Attributed to DOSRAM performance improvement, 100MHz normally-off (Noff) CPU is successfully demonstrated with drastically reduced power consumption (~94% power reduction for ARM Cortex-M0 and ~70% power reduction for memory), making it a promising candidate for IoT application. In addition, an OS-FPGA is successfully fabricated by integration of 65nm SiFET and 60nm oxide semiconductor FET (OSFET) with an operation frequency of 360MHz. The application of the OSFET in analog circuits will also be discussed in this paper.

JFS3-4 - 9:45
A 65 nm 1.0 V 1.84 ns Silicon-On-Thin-Box (SOTB) Embedded SRAM with 13.72 nW/Mbit Standby Power for Smart IoT, M. Yabuuchi*, K. Nii*, S. Tanaka*, Y. Shinozaki**, Y. Yamamoto*, T. Hasegawa*, H. Shinkawata* and S. Kamohara*, *Renesas Electronics Corp. and **Nippon Systemware Co. Ltd., Japan

A 65-nm Silicon-on-Thin-Box (SOTB) embedded SRAM is demonstrated. By using back-bias (BB) control in the sleep mode, 13.72 nW/Mbit ultra-low standby power is observed, which is reduced to 1/1000 compared to the normal standby mode. The measured read access time with forward BB is 1.84 ns at 1.0 V overdrive and 25°C, which is improved by 60% and thus we achieved over 380 MHz operation. Up to 20% active read power reduction is also achieved by using proposed localized adoptive wordline width control.

SESSION 13

Quantum Neuromorphic Computing [Shunju I]

Thursday, June 8, 8:30-10:10

Chairpersons: K. Endo, AIST
G. Jurczak, ASM

T13-1 - 8:30
Towards Quantum Computing in Si MOS Technology: Single-Shot Readout of Spin States in a FDSOI Split-Gate Device with Built-In Charge Detector, M. Urdampilleta*, L. Hutin**, B. Jadot*, B. Bertrand**, H. Bohuslavskyi**.***, R. Maurand***, S. Barraud**, C. Bäuerle*, M. Sanquer***, X. Jehl***, S. De Franceschi***, T. Meunier* and M. Vinet**, *Institut Néel, **CEA-LETI and ***CEA, INAC-PHELIQS, France

We report on the first demonstration of real-time monitoring of the electron spin in a Quantum Dot using foundry-compatible Si MOS technology and a Split-Gate design with built-in charge detector. Since single-shot readout is an indispensable step in the pursuit of Si-based fault-tolerant quantum computing, this work contributes to asserting the fabrication of Si spin qubits in a MOS technology platform as a viable and promising option.

T13-2 - 8:55
Achieving Ideal Accuracies in Analog Neuromorphic Computing Using Periodic Carry, S. Agarwal, R. B. J. Gedrim, A. H. Hsia, D. R. Hughart, E. J. Fuller, A. A. Talin, C. D. James, S. J. Plimpton and M. J. Marinella, Sandia National Laboratories, USA

Analog resistive memories promise to reduce the energy of neural networks by orders of magnitude. However, the write variability and write nonlinearity of current devices prevent neural networks from training to high accuracy. We present a novel periodic carry method that uses a positional number system to overcome this while maintaining the benefit of parallel analog matrix operations. We demonstrate how noisy, nonlinear TaO_x devices that could only train to 80% accuracy on MNIST, can now reach 97% accuracy, only 1% away from an ideal numeric accuracy of 98%. On a file type dataset, the TaO_x devices achieve ideal numeric accuracy. In addition, low noise, linear $Li_{1-x}CoO_2$ devices train to ideal numeric accuracies using periodic carry on both datasets.

T13-3 - 9:20
Novel Ferroelectric FET Based Synapse for Neuromorphic Systems, H. Mulaosmanovic*, J. Ocker*, S. Müller*, M. Noack*, J. Müller**, P. Polakowski**, T. Mikolajick*,*** and S. Slesazeck*, *NaMLab gGmbH, **Fraunhofer IPMS and ***IHM TU Dresden, Germany

A compact nanoscale device emulating the functionality of biological synapses is an essential element for neuromorphic systems. Here we present for the first time a synapse based on a single ferroelectric FET (FeFET) integrated in a 28nm HKMG technology, having hafnium oxide as the ferroelectric and a resistive element in series. The gradual and non-volatile ferroelectric switching is exploited to mimic the synaptic weight. We demonstrate both the spike-timing dependent plasticity (STDP) and the signal transmission and discuss the effect of the spike properties and circuit design on STDP.

T13-4 - 9:45
Design-Technology Co-Optimization for OxRRAM-Based Synaptic Processing Unit, A. Mallik*, D. Garbin*, A. Fantini*, D. Rodopoulos*, R. Degraeve*, J. Stuijt**, A. K. Das**, S. Schaafsma**, P. Debacker*, G. Donadio*, H. Hody*, L. Goux*, G. S. Kar*, A. Furnemont*, A. Mocuta* and P. Raghavan*, *imec-BE, Belgium and **imec-NL, The Netherlands

In this paper, we present a design-technology tradeoff analysis to implement a fully connected neural network using non-volatile OxRRAM cells. The requirement of a high number of distinct levels in synaptic weight has been established as a primary bottleneck for using a single NVM as a synaptic unit. We propose a mixed-radix encoding system for a multi-device synaptic unit achieving high classification accuracy (94%) including device variability. To our knowledge, this is the first paper to discuss the tradeoff between single and multi-device synaptic weight in terms of design and technology using silicon data. We have demonstrated that high level of variability can be handled by the neuromorphic algorithm. The results presented in the paper has been obtained from 1Mb array.

Technology / Circuits Joint Focus Session 4

Computing Beyond Von Neumann [Shunju II, III]

Thursday, June 8, 10:30-12:10

Chairpersons: M. Kobayashi, The Univ. of Tokyo
M. Vinet, CEA-LETI, MINATEC

JFS4-1 - 10:30 (Invited)
Implementation Challenges for Scalable Neuromorphic Computing, S. Yamamichi, A. Horibe, T. Aoki, K. Hosokawa, T. Hisada and H. Mori, IBM Research, Japan

In the big data era, a new computing system, called Cognitive Computing, that can handle unstructured data, learn and extract the insights is required. A neuromorphic device is a key component for this, and several architectures are reported. Compared to the neuromorphic device with SRAM-based spiking neural network, a cross-bar structure device realizes on-chip leaning, but requires high-density off-chip interconnect, much higher than those for conventional high-end logic devices. Recent progress of solder bumping and 3-dimentional integration technologies are described.

JFS4-2 - 10:55 (Invited)
Distributed Quantum Computing Systems: Technology to Quantum Circuits, R. Van Meter, Keio Univ., Japan

Quantum computers, both solid-state and other, are developing rapidly in the laboratory and commercialization has begun. We discuss their potential applications and the challenges of manufacturing, managing errors, and creating full-scale systems.

JFS4-3 - 11:20
Ultra-Low Power Probabilistic IMT Neurons for Stochastic Sampling Machines, M. Jerry*, A. Parihar**, B. Grisafe*, A. Raychowdhury** and S. Datta*, *Univ. of Notre Dame and **Georgia Institute of Technology, USA

Stochastic sampling machines (SSM) utilize neural sampling from probabilistic spiking neurons to escape local minima and prevent overfitting of training datasets. This enables improved error rates compared to deterministic implementations, and, in turn, enables lower bit precision, decreased chip area, and reduced energy consumption. In this work, we experimentally demonstrate: (i) Insulator-to-Metal Phase Transition (IMT) neurons with record low peak operating power of 11.9μW at V_{DD}=0.7V; (ii) the IMT in vanadium dioxide (VO_2) provides a natural probabilistic hardware substrate for realizing a compact stochastic IMT neuron for SSMs; (iii) implementation of SSM for pattern recognition on MNIST database using experimentally calibrated device modeling. These results are compared to a 22nm CMOS ASIC which shows stochastic IMT neuron based SSMs result in a 4.5x reduction in system power consumption.

JFS4-4 - 11:45
A 462GOPs/J RRAM-Based Nonvolatile Intelligent Processor for Energy Harvesting IoE System Featuring Nonvolatile Logics and Processing-In-Memory, F. Su*, W.-H. Chen**, L. Xia*, C.-P. Lo**, T. Tang*, Z. Wang*, K.-H. Hsu**, M. Cheng*, J.-Y. Li**, Y. Xie***, Y. Wang*, M.-F. Chang**, H. Yang* and Y. Liu*, *Tsinghua Univ., China, **National Tsing Hua Univ., Taiwan and ***Univ. of California, Santa Barbara, USA

An energy-efficient nonvolatile intelligent processor (NIP) is proposed for battery-less energy harvesting system. This NIP employs RRAM-based nonvolatile logics (NVL) with self-write-termination (SWT) scheme and low-power processing-in-memory (PIM) to achieve energy-efficient computing against frequent power-off situations. An NIP test chip was fabricated in 150nm CMOS process using HfO RRAM. This NIP chip achieves 462GOPs/J energy efficiency at 20MHz clock frequency, showing 13× performance improvement over state-of-the-arts. This work presents the first nonvolatile processor capable of general as well as neural network computing in addition to the first integrated chip using RRAM-based PIM.

SESSION 14

SiGe / Ge FET 2 [Shunju I]

Thursday, June 8, 10:30-12:10

Chairpersons: S. Takagi, The Univ. of Tokyo
T. Palacios, Massachusetts Institute of Technology

T14-1 - 10:30
First Experimental Observation of Channel Thickness Scaling (Down to 3 nm) Induced Mobility Enhancement in UTB GeOI *n*MOSFETs, W. H. Chang, T. Irisawa, H. Ishii, H. Hattori, H. Ota, H. Takagi, Y. Kurashima, N. Uchida and T. Maeda, AIST, Japan

Electron mobility of ultra thin body (UTB) GeOI *n*MOSFETs with body thickness (T_{body}) down to 3 nm has been systematically investigated and significant mobility enhancement with *decreasing* T_{body} has been observed for the first time. This channel thickness scaling induced mobility enhancement can be attributed to the unique physical property of ultra thin Ge where the electron effective mass reduces with scaling T_{body} through the band structure modification.

T14-2 - 10:55
Strained Germanium Gate-All-Around PMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition, L. Witters*, F. Sebaai*, A. Hikavyy*, A. P. Milenin*, R. Loo*, A. De Keersgieter*, G. Eneman*, T. Schram*, K. Wostyn*, K. Devriendt*, A. Schulze*, R. Lieten**, S. Bilodeau**, E. Cooper**, P. Storck***, C. Vrancken*, H. Arimura*, P. Favia*, E. Vancoille*, J. Mitard*, R. Langer*, A. Opdebeeck*, F. Holsteyns*, N. Waldron*, K. Barla*, V. De Heyn*, D. Mocuta* and N. Collaert*, *imec, **Entegris, Inc. and ***Siltronic AG, Belgium

Strained Ge p-channel Gate-All-Around (GAA) FETs are demonstrated on 300mm SiGe Strain Relaxed Buffer (SRB) and 45nm Fin pitch with the shortest gate lengths (L_G=40nm) and smallest Ge nanowire (NW) diameter (d=9nm) reported to date. Optimization of groundplane doping (GP) is required to minimize the impact of the parasitic channel in the SRB. The strained Ge GAA devices maintain excellent electrostatic control at the shortest gate lengths studied (L_G=40nm) with DIBL of 30mV/V and sub-threshold slope (SS_{SAT}) of 79mV/dec. This work shows a significant improvement not only compared to our previous work on strained Ge finFETs but also when benchmarked to published Ge GAA devices.

T14-3 - 11:20
Performance and Electrostatic Improvement by High-Pressure Anneal on Si-Passivated Strained Ge pFinFET and Gate All Around Devices with Superior NBTI Reliability, H. Arimura*, L. Witters*, D. Cott*, H. Dekkers*, R. Loo*, J. Mitard*, L.-Å. Ragnarsson*, K. Wostyn*, G. Boccardi*, E. Chiu**, A. Subirats*, P. Favia*, E. Vancoille*, V. De Heyn*, D. Mocuta* and N. Collaert*, *imec, Belgium and **Poongsan Corp., USA

This paper shows high-pressure anneal (HPA) as a performance booster for Si-passivated strained Ge (sGe) p-channel FinFET and gate-all-around (GAA) devices. Improved interface quality and hole mobility (~600 cm^2/Vs) are obtained on FinFET after HPA at 450°C. While V_{TH} is tuned by ~400 mV using TiAl work function metal (WFM), HPA-induced increases in J_G and NBTI are suppressed by barrier layer engineering under the TiAl. Finally, the optimized HPA is also shown to improve the electrostatics and overall performance of GAA devices, reaching SS_{LIN} of 65 mV/dec at L_G=60 nm and a Q factor of 15 with low I_{OFF} of ~$3x10^{-9}$ A/μm.

T14-4 - 11:45
The First GeSn FinFET on a Novel GeSnOI Substrate Achieving Lowest *S* of 79 mV/decade and Record High $G_{m,int}$ of 807 μS/μm for GeSn P-FETs, D. Lei*, K. H. Lee**, S. Bao**.***, W. Wang*, S. Masudy-Panah*, S. Yadav*, A. Kumar*, Y. Dong*, Y. Kang*, S. Xu*, Y. Wu*, Y.-C. Huang****, H. Chung****, S. S. Chu****, S. Kuppurao****, C. S. Tan**.***, X. Gong* and Y.-C. Yeo*.*****, *National Univ. of Singapore, **Singapore MIT Alliance for Research and Technology, ***Nanyang Technological Univ., Singapore, ****Applied Materials., USA and *****Currently with TSMC, Taiwan

The world's first GeSn p-FinFETs formed on a novel GeSn-on-insulator (GeSnOI) substrate is reported, with channel lengths L_{CH} down to 50 nm and fin width W_{Fin} down to 20 nm. In comparison with other reported GeSn p-FETs, record low *S* of 79 mV/decade, record high $G_{m,int}$ of 807 μS/μm (V_{DS} of -0.5 V), and the highest $G_{m,int}/S_{sat}$ were achieved. The highest high-field hole mobility of 208 cm^2/V·s (at inversion carrier density N_{inv} of $8×10^{12}$ cm^{-2}) for GeSn p-FETs with CVD grown GeSn channel was also obtained.

Luncheon Talk [Suzaku I]

Thursday, June 8, 12:40-14:00

Organizers: M. Ikeda, The Univ. of Tokyo
M. Masahara, AIST

Approach to Develop Prosthetic Technology as a Part of Body, K. Endo, Xiborg

Once a part of human body is disabled physically or functionally, he would lose a huge amount of his quality of life, and the current available technology is not functional enough to compensate lost function in comprehensive way. On the other hand, several fields such as paralympic long jump show possibility of technology which could exceed human normal function. We are currently focusing on developing prosthetic technology to optimize sprint gait which is eventually useful to develop device supporting human life.

SESSION 15

Memory 2 Flash MRAM [Shunju II, III]

Thursday, June 8, 14:00-15:40

Chairpersons: H.-T. Lue, Macronix International Co., Ltd.
N. Ramaswamy, Micron Technology, Inc.

T15-1 - 14:00
High-Speed and Logic-Compatible Split-Gate Embedded Flash on 28-nm Low-Power HKMG Logic Process, Y. K. Lee, C. Jeon, H. Min, B. Seo, K. Kim, D. Kim, K. Min, J. S. Woo, H. Kang, Y. S. Chung, M. Kim, J. Jang, K. S. Yeom, J.-S. Kim, M. H. Oh, H. Lee, S. Cho and D. Lee, Samsung Electronics Co., Ltd., Korea

We developed a 4Mb split-gate e-flash on 28-nm low-power HKMG logic process, which demonstrates the smallest bit-cell size (0.03x-um^2) for high performance IoT applications. High speed operation (25us write time and 2ms erase operation) and robust reliability (500K cycle, 10 years retention) are achieved through optimization of triple-gate flash architecture and scaling of word-line (WL) transistor. New type of high-voltage transistor with LDD-first scheme is applied to enable further scaling of decoder block in Flash IP. Digital-Vdd (1.0V) read operation is used by lowering threshold voltage (Vth) of HV transistor without sacrificing break-down during Flash P/E operation. By using module process concept, the existing RF and logic IP is reused without modification.

T15-2 - 14:25
First Demonstration of Diode-Type 3-D NAND Flash Memory String Having Super-Steep Switching Slope, N. Choi, H.-J. Kang, S. Chung, S.-H. Bae, B.-G. Park and J.-H. Lee, Seoul National Univ. and SK hynix Inc., Korea

Super-steep switching is successfully demonstrated using positive feedback (PF) in fabricated diode-type 3-D NAND flash memory strings. Thanks to the PF, the subthreshold swing (*SS*) measured in a cell of a string during read operation is less than 1 mV/dec at turn-on voltage (V_{on}) regardless of the polarity and the amount of the charge stored in the cell. This string has memory characteristics similar to conventional FET-type string while keeping much better *SS* than that of the FET -type string even after program/erase (P/E) cycling.

T15-3 - 14:50
Flash Reliability Boost Huffman Coding (FRBH): Co-Optimization of Data Compression and V_{TH} Distribution Modulation to Enhance Data-Retention Time by Over 2900x, Y. Deguchi, A. Kobayashi, H. Watanabe and K. Takeuchi, Chuo Univ., Japan

Highly reliable data compression technique, Flash Reliability Boost Huffman coding is proposed for Triple-Level Cell (TLC) NAND Flash memory. The problem of TLC Flash is the poor reliability. In the proposed SSD, the data compression is performed to increase the endurance of TLC Flash. Because the data size written to TLC Flash is reduced, the write/erase cycle is also reduced. In addition, to further enhance the reliability, the proposed SSD controller optimizes the Vth distribution by allocating more frequent data to Huffman tree branches with more reliable Vth states. By the combined benefit of reduced write/erase cycles and optimized V_{th} distribution, memory cell errors decrease by 92% and the data-retention time extends by over 2900 times. Although conventional high reliability techniques such as Flex-nLC require 37% cell area overhead, the proposed SSD requires no cell area overhead and thus is the lowest cost and highest reliability storage solution.

T15-4 - 15:15
CMOS-Embedded STT-MRAM Arrays in 2x nm Nodes for GP-MCU Applications, D. Shum*, D. Houssameddine*, S. T. Woo*, Y. S. You*, J. Wong*, K. W. Wong*, C. C. Wang*, K. H. Lee*, K. Yamane*, V. B. Naik*, C. S. Seet*, T. Tahmasebi*, C. Hai*, H. W. Yang*, N. Thiyagarajah*, R. Chao*, J. W. Ting*, N. L. Chung*, T. Ling*, T. H. Chan*, S. Y. Siah*, R. Nair*, S. Deshpande**, R. Whig**, K. Nagel**, S. Aggarwal**, M. DeHerrera**, J. Janesky**, M. Lin**, H.-J. Chia**, M. Hossain**, H. Lu**, S. Ikegawa**, F. B. Mancoff**, G. Shimon**, J. M. Slaughter**, J. J. Sun**, M. Tran**, S. M. Alam** and T. Andre**, *GLOBALFOUNDRIES Singapore Pte, Ltd., Singapore and **Everspin Technologies, Inc., USA

Perpendicular Spin-Transfer Torque (STT) MRAM is a promising technology in terms of read/write speed, low power consumption and non-volatility, but there has not been a demonstration of high density manufacturability at small geometries. In this paper we present an unprecedented demonstration of a robust STT-MRAM technology designed in a 2x nm CMOS-embedded 40 Mb array. Key features are full array functionality with low BER (bit error rate), process uniformity and reliability, 10 years data retention at 125C with extended endurance to ~ 10^7 cycles. All achieved with standard BEOL process temperatures. Data retention post 260°C solder reflow temperature cycle is demonstrated.

SESSION 16

Process [Shunju I]

Thursday, June 8, 14:00-15:40

Chairpersons: T. Miyashita, Toshiba Corp.
Y. Liang, nVidia

T16-1 - 14:00
Dual Beam Laser Annealing for Contact Resistance Reduction and Its Impact on VLSI Integrated Circuit Variability, Z. Liu*, O. Gluschenkov*, H. Niimi**, B. Liu**, J. Li*, J. Demarest*, S. Mochizuki*, P. Adusumilli*, M. Raymond**, A. Carr*, S. Chen***, Y. Wang***, H. Jagannathan* and T. Yamashita*, *IBM Research, **GLOBALFOUNDRIES and ***Ultratech Inc, USA

Introduction of a dual beam (DB) millisecond (mSec) or nanosecond (nSec) laser annealing in contact module results in a drastic reduction of contact resistivity. Dependence of this benefit on laser annealing parameters is detailed. The annealing power/temperature condition needed for initiating solid or liquid phase epitaxy (SPE, LPE) defines a lower process boundary, while impact of laser annealing on transistor parameters, such as V_t and gate stack, defines an upper process boundary and translates to with-in-die (WID) V_t variation. Combining DB laser annealing technique with process-friendly layouts enables contact resistance benefit without degrading product level variability.

T16-2 - 14:25
Sub-10^{-9} Ω.cm² Contact Resistivity on p-SiGe Achieved by Ga Doping and Nanosecond Laser Activation, J.-L. Everaert*, M. Schaekers*, H. Yu*,**, L.-L. Wang*,**,***, A. Hikavyy*, L. Date****, J. del Agua Borniquel****, K. Hollar****, F. A. Khaja****, W. Aderhold****, A. J. Mayur****, J. Y. Lee****, H. van Meer****, Y.-L. Jiang***, K. De Meyer*,**, D. Mocuta* and N. Horiguchi*, *imec, **KU Leuven, Belgium, ***Fudan Univ., China and ****Applied Materials, USA

We report record breaking values for PMOS source drain (S/D) contact resistivity < 10^{-9} Ω.cm². These were obtained by shallow Ga ion implantation on $Si_{0.4}Ge_{0.6}$ in combination with subsequent pulsed nanosecond laser anneal (NLA). Cross section transmission electron microscopy (XTEM) shows the contact resistivity reduction mechanism is based on Ga and Ge segregation towards the surface.

T16-3 - 14:50
Highly-Selective Superconformal CVD Ti Silicide Process Enabling Area-Enhanced Contacts for Next-Generation CMOS Architectures, N. Breil*, A. Carr**, T. Kuratomi*, C. Lavoie**, I.-C. Chen*, M. Stolfi*, K. D. Chiu*, W. Wang**, H. Van Meer*, S. Sharma*, R. Hung*, A. Gelatos*, J. Jordan-Sweet**, E. Levrau**, N. Loubet**, R. Chao**, J. Ye*, A. Ozcan**, C. Surisetty** and M. Chudzik*, *Applied Materials and **IBM Research, USA

We investigate a novel Ti Chemical Vapor Deposition (CVD Ti) technique for source/drain and trench contact silicidation. This work is a first demonstration of a highly selective, superconformal Ti process that exhibits a low p-type CVD Ti/SiGe:B contact resistivity (ρ_c) down to *2.1x10^{-9} Ω.cm²* (a 40% reduction vs. PVD Ti), matching the lowest published values. A competitive n-type CVD Ti/Si:P with a ρ_c at *2.6x10^{-9} Ω.cm²* is measured. We demonstrate up to 90% superconformality for this process, with a tunnel silicidation at lengths up to 500nm, showing an exceptional selectivity to oxide. This process is an enabler for the next generation of area-enhanced contact CMOS architectures.

T16-4 - 15:15
Record Low Specific Contact Resistivity (1.2×10^{-9} Ω-cm²) for P-Type Semiconductors: Incorporation of Sn into Ge and *In-Situ* Ga Doping, Y. Wu*, S. Luo*, W. Wang*, S. Masudy-Panah*, D. Lei*, X. Gong*, G. Liang* and Y.-C. Yeo*,**, *National Univ. of Singapore, Singapore and **Currently with TSMC, Taiwan

Record-low specific contact resistivity down to 1.2×10^{-9} Ω-cm² is achieved for Ti/p^+-$Ge_{0.95}Sn_{0.05}$ contact by incorporating Sn into Ge and *in-situ* Ga doping with active doping concentration of 1.6×10^{20} cm^{-3}. As compared with Ni(GeSn)/p^+-$Ge_{0.95}Sn_{0.05}$ contact, Ti/p^+-$Ge_{0.95}Sn_{0.05}$ contact exhibits lower specific contact resistivity and is more thermally stable. In addition, theoretical calculation shows that for a given doping concentration, incorporating Sn into Ge lowers the specific contact resistivity as compared with metal/p-Ge contacts.

SESSION 17

CMOS Integration II [Shunju II, III]

Thursday, June 8, 16:00-18:05

Chairpersons: K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.
V. Narayanan, IBM

T17-1 - 16:00
Low-Variation SRAM Bitcells in 22nm FDSOI Technology, V. Joshi, H. Ramamurthy, S. Balasubramanian, S. Seo, H. Yoon, X. Zou, N. Chan, J. Yun, T. Klick, E. Smith, J. Schmid, R. van Bentum, J. Faul and C. Weintraub, GLOBALFOUNDRIES, USA

We present the SRAM bitcell offering from 22FDX™ (a 22nm FDSOI technology) with competitive 1.46mV-µm FinFET-like transistor mismatch coefficient (AVt) built with low cost planar architecture. Extremely low minimum operating voltages (Vmin) are reported for both the high-density (HD) 0.110µm² and high-current (HC) 0.124µm² bitcells without any assist, showing 95% limited yield (LY) Vmin values of 0.6V and 0.5V for 64Mb HD and 128Mb HC arrays, respectively. Due to FDSOI architecture, bitline capacitance (Cbl) of the HD 0.110um² bitcell is similar to 14nm FinFET HD 0.064um² bitcell, and more than 30% lower compared to 28nm high-k metal gate (HKMG) HD 0.127um² bitcell. Finally, we tune SRAM performance and stability with the use of back-gate bias to demonstrate HD standby leakage of 5pA/cell and two-port (TP) 0.185 µm² assisted 64Mb 95% LY Vmin of 0.44V.

T17-2 - 16:25
Impact of Strain on Access Resistance in Planar and Nanowire CMOS Devices, R. Berthelon*.**.***, F. Andrieu*, F. Triozon*, M. Cassé*, L. Bourdet*, G. Ghibaudo****, D. Rideau**, Y. M. Niquet**, S. Barraud*, P. Nguyen*, C. Le Royer*, J. Lacord*, C. Tabone*, O. Rozeau*, D. Dutartre**, A. Claverie***, E. Josse**, F. Arnaud** and M. Vinet*, *CEA-LETI, **STMicroelectronics, ***CEMES and ****IMEP-LaHC, France

We fabricated and in-depth characterized advanced planar and nanowire CMOS devices, strained by the substrate (sSOI or SiGe channel) and by the process (CESL, SiGe source/drain). We have built a novel access resistance (R_{ACC}) extraction procedure, which enables us to clearly evidence the strong impact of back-bias and strain on R_{ACC} (-21% for 4V VB and -53% for -1GPa stress on pMOS FDSOI). This is in agreement with Non-Equilibrium-Green-Functions (NEGF)simulations. This R_{ACC}(strain) dependence has been introduced into SPICE, leading to +6% increase of the RO frequency under strain n/p =0.8%/-0.5%, compared to the state-of-the-art model. It is thus mandatory for predictive benchmarking and optimized IC designs.

T17-3 - 16:50
Key Process Steps for High Performance and Reliable 3D Sequential Integration, C.-M. V. Lu*.**, F. Deprat*, C. Fenouillet-Beranger*, P. Batude*, X. Garros*, A. Tsiara*, C. Leroux*, R. Gassilloud*, D. Nouguier**, D. Ney**, X. Federspiel**, P. Besombes*, A. Toffoli*, G. Romano**.*, N. Rambal*, V. Delaye*, D. Barge**, M.-P. Samson**.*, B. Previtali*, C. Tabone*, L. Pasini**.*, L. Brunet*, F. Andrieu*, J. Micoud*, T. Skotnicki** and M. Vinet*, *CEA-LETI and **STMicroelectronics, France

This work provides breakthroughs in key technological modules for high performance and reliable 3D Sequential Integration with intermediate BEOL (iBEOL) in-between tiers. We demonstrate that (i) a high-quality solid phase epitaxy process is possible at 500°C, (ii) TiN native oxide removal prior to poly deposition leads to an improvement in gate stack reliability below 525°C and (iii) state-of-the-art SiOCH ULK in iBEOL is reliable up to 550°C 5h with W metal lines. A process integration is thus proposed to match the process windows of bottom layers (bottom FET and iBEOL) stability and top devices performance and reliability, opening perspectives for a wide range of applications and technologies using 3D Sequential Integration.

T17-4 - 17:15
Influence of Stress Induced CT Local Layout Effect (LLE) on 14nm FinFET, P. Zhao, S. M. Pandey, E. Banghart, X. He, R. Asra, V. Mahajan, H. Zhang, B. Zhu, K. Yamada, L. Cao, P. Balasubramaniam, M. Joshi, M. Eller, F. Benistant and S. Samavedam, GLOBALFOUNDRIES, USA

In this paper, we present a new local layout effect in 14nm FinFET due to different CT layout designs (CT extension, CT spacing, and PC past RX distance). Based on 14nm FinFET experimental data, the CT LLE effect induces up to 50mV Vtsat shift, and ~20% current change. NFET performance is enhanced by about 7%, while the PFET performance shows slight degradation. Based on TCAD simulation, the CT LLE is fully analyzed and explained by the tensile stress induced in the inter-layer dielectric (ILD).

T17-5 - 17:40 (Late News)
Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET, N. Loubet*, T. Hook*, P. Montanini*, C.-W. Yeung*, S. Kanakasabapathy*, M. Guillorn*, T. Yamashita*, J. Zhang*, X. Miao*, J. Wang*, A. Young*, R. Chao*, M. Kang**, Z. Liu*, S. Fan*, B. Hamieh*, S. Sieg*, Y. Mignot*, W. Xu*, S.-C. Seo*, J. Yoo**, S. Mochizuki*, M. Sankarapandian*, O. Kwon**, A. Carr*, A. Greene*, Y. Park**, J. Frougier***, R. Galatage***, R. Bao*, J. Shearer*, R. Conti*, H. Song**, D. Lee**, D. Kong*, Y. Xu*, A. Arceo*, Z. Bi*, P. Xu*, R. Muthinti*, J. Li*, R. Wong*, D. Brown***, P. Oldiges*, R. Robison*, J. Arnold*, N. Felix*, S. Skordas*, J. Gaudiello*, T. Standaert*, H. Jagannathan*, D. Corliss*, M.-H. Na*, A. Knorr***, T. Wu*, D. Gupta*, S. Lian**, R. Divakaruni*, T. Gow*, C. Labelle***, S. Lee**, V. Paruchuri*, H. Bu* and M. Khare*, *IBM, **Samsung Electronics Co., Ltd., ***GLOBALFOUNDRIES, USA

In this paper, for the first time we demonstrate that horizontally stacked gate-all-around (GAA) Nanosheet structure is a good candidate for the replacement of FinFET at the 5nm technology node and beyond. It offers increased W_{eff} per active footprint and better performance compared to FinFET, and with a less complex patterning strategy, leveraging EUV lithography. Good electrostatics are reported at L_g=12nm and aggressive 44/48nm CPP (Contacted Poly Pitch) ground rules. We demonstrate work function metal (WFM) replacement and multiple threshold voltages, compatible with aggressive sheet to sheet spacing for wide stacked sheets. Stiction of sheets in long-channel devices is eliminated. Dielectric isolation is shown on standard bulk substrate for sub-sheet leakage control. Wrap-around contact (WAC) is evaluated for extrinsic resistance reduction.

2017 Symposium on VLSI Techonlogy / Circuits

International Forum on Singularity: Exponential X (Friday Forum)

Friday, June 9, 9:00-16:30

General Chair: T. Hiramoto, Univ. of Tokyo
Program Committee Chair K. Yano, Hitachi

8:30 **Welcome to Exponential X,** K. Yano, Hitachi

Session 1. Exponential Technology

9:15 **Exponential Neuromorphic Systems for Singularity,** V. De, Intel

9:45 **Exponential Computing for Singularity,** M. Saito, PEZY

10:15 **Exponential Connectivity for Singularity,** A. Amerasekera, UCB/BWRC

10:45 **Exponential Commerce for Singularity,** T. Kitagawa, Rakuten

11:15 Panel **"Where will the Next Exponential Technology Arise?"**

12:00 **Lunch Time**

Session 2. Exponential Humans

13:30 **Exponential Intelligence for Singularity,** K. Ataka, Yahoo

14:00 **Exponential Healthcare for Singularity,** Y. Ishikawa

14:30 **Exponential Mind for Singularity,** J. Tani, KAIST

15:00 **Exponential Robotics for Singularity,** K. Kanaoka, Ritsumeikan Univ.

15:30 **Break**

15:45 Panel **"How will Human Beings Change in the Future?"**