Complete Extraction of Defect Bands Responsible for Instabilities in n and pFinFETs

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Abstract: Bias temperature instabilities (BTI) are serious reliability issues in high-k technologies and occur for positive and negative stress voltages in both n and pMOSFETs. The cases with the strongest degradation, namely negative BTI (NBTI) in pMOS and positive BTI (PBTI) in nMOSFETs, are typically studied and modeled separately, which led to *considerable inconsistencies* regarding the distributions of the responsible defects. Here we present *the first study which successfully describes all four combinations of BTI in n/pMOSFETs within a single model*. This was achieved by determining the physical properties of the defects in HfO_2 and in SiO_2. Using our extraction method, any ambiguity regarding the location of the defect bands is completely eliminated, allowing for correct physics-based extrapolation of degradation data to use conditions.

Introduction: Bias temperature instabilities (BTI) remain a serious reliability concern in high-k FinFETs. Although a number of controversial issues are not yet resolved,[1,2] BTI is typically considered to be due to two components, one of them recoverable, and the other one more permanent. The recoverable component is often assumed to be due to charge trapping in the gate stack, with PBTI in nMOSFETs being due to electron traps[3–5] and NBTI in pMOSFETs due to hole traps.[6–8] Usually, the focus is put on only one of these two dominant degradation modes even though the same dielectric stack is used for n and pFETs. Also the two weaker degradation modes, namely NBTI in nMOSFETs and PBTI in pMOSFETs, are only studied occasionally.[6,9–11] Here we demonstrate for the first time that the bias and time dependence of the recoverable components of all four combinations of BTI *is a direct consequence of the unique position of the defect bands in the gate stack*. Most importantly, any deviation in the defect band may go unnoticed for one combination, say NBTI in pMOSFETs, but lead to serious errors in another one.

Measurement setup: The experiments in this work were conducted on a high-k FinFET technology with a 1.2 nm (EOT) gate stack (HfO_2 with a SiO_2 interface layer), targeting the 14 nm node. In order to separate the recoverable from the more permanent contribution, we employ $I_D V_G$ ramps from accumulation to inversion,[12] which remove the majority of the bias-dependent trapped charges, see **Fig. 1**. As shown in **Fig. 2** for an exemplary stress setup, this method allows for reproducible extraction of the recoverable component even after a different stress "history".

In order to extract the average degradation representative for the investigated technology, PBTI and NBTI on pMOS and nMOS devices were measured on 220 FinFETs connected in parallel for various gate voltages (positive and negative, for PBTI and NBTI, respectively) at 125°C. Also, for further validation, structures with two parallel Fins were measured to study the statistical distribution of the step-heights.

Physical modeling: We base our defect model on our previously developed four-state non-radiative multiphonon model.[13] This model has already been succesfully applied to various aspects of charge trapping in oxides, most importantly RTN, SILC, and BTI.[8,14–17] For the simulation of ΔV_{thR} a set of microscopic defects was generated assuming that the model parameters, such as relaxation energies and defect levels, are normally distributed, while the traps were uniformly distributed across the SiO_2 (hole traps) or the HfO_2 (electron traps).

By calibrating our model to the comprehensive experimental data sets which cover all four combinations of BTI, these distributions were determined for HfO_2 and SiO_2. The distributions of the defect levels E_T (w.r.t. the respective valence band edge), together with the defect concentrations N_{OT} are given in the table below.

	$\langle E_T \rangle \pm \sigma_{E_T}$ [eV]	N_{OT} [cm^{-3}]	N_{OT} [cm^{-2}]
HfO_2	3.82 ± 0.43	2.9×10^{20}	6.4×10^{13}
SiO_2	4.44 ± 0.35	0.9×10^{20}	2.0×10^{13}

NBTI/PBTI in pMOSFETs: The pronounced degradation during **NBTI** is a direct consequence of the position of the defect bands as can be seen in the band diagrams in **Fig. 3** for equilibrium conditions: Most hole defects in the SiO_2 are below the Fermi level of the channel and are thus neutral in the "pristine" device at $V_G = 0$ V. The shift of the trap levels of these defects due to the application of a negative gate voltage during NBTI enables hole capture from the channel. Additionally, some initially occupied electron traps in the HfO_2 now tend to emit electrons to the channel as they are far above the channel Fermi level. However, some electron traps will remain occupied because the rate of electrons coming from the gate can be larger than the rate of electron emission into the channel. Naturally, these defects will contribute to trap-assisted tunneling currents. Note that this effect does not necessarily depend on the position of the traps in the oxide but on the configurational details of the traps, for instance their relaxation energy.[16]

Under application of a positive gate voltage (**PBTI**), again both, defects in the HfO_2 and in the SiO_2 cause degradation, but towards positive V_{th}. Since most SiO_2 defects are already neutral in the "pristine" device, their effect is much weaker, while the contribution of HfO_2 defects is found to be on the same order of magnitude as for NBTI of the same device.

The relative contributions of the electron and hole traps in the HfO_2 and SiO_2 are shown in **Fig. 4** as a function of the stress bias. While electron trapping in the HfO_2 does contribute to both NBTI and PBTI, the degradation is dominated by hole trapping in the SiO_2 at all bias conditions. This is consistent with the observation that NBTI in high-k technologies is often perceived to be very similar to SiO_2 and SiON technologies.[18,19]

NBTI/PBTI in nMOSFETs: Since the oxide materials and therefore the oxide defects are assumed to be the same for pMOS and nMOSFETs, all four degradation modes must be consistent with a single set of defect parameters. This is insofar a challenge to the model as the degradation for nMOSFETs is visibly different from the pMOSFET case. However, this *difference is correctly reproduced by our model and can be again traced back to the location of the defect bands in the* HfO_2 *and* SiO_2. Putting it differently, the peculiar behavior of NBTI/PBTI in n/pMOSFETs can *only* be explained by a particular location of the defect bands, which can thus be used for a precise extraction of their location.

As shown in the band diagrams for the nMOS in **Fig. 5**, hole trapping in the SiO_2 during **NBTI** is less pronounced compared to pMOSFETs because the defects are shifted above the Fermi level of the channel to a smaller extent. This is due to the different work function differences for the nMOS compared to the pMOS (about 0.7 eV). For the same reason, the defects in the HfO_2 are shifted further below the Fermi level from the channel for **PBTI**, hence reducing the barrier for electron capture from the channel dramatically. This shifts the balance for *electron emission towards the gate* and *electron capture from the channel* in favor of the latter, resulting in stronger PBTI than NBTI.

As in Fig. 4, **Fig. 6** compares the contributions of electron and hole traps to PBTI/NBTI of the nMOSFETs. Curiously, due to the unique position of the defect bands, PBTI is purely due to electron trapping in the high-k, consistent with previous high-k PBTI-only models[5,20] and also fully consistent with the absence of PBTI in SiON technologies.[6] The technologically less relevant case of NBTI, on the other hand, is due to about equal contributions of both trap types.

The "Four" Cases: NBTI/PBTI in n/pMOSFETs: The final modeling results for all four cases are shown in **Fig. 7** for a number of gate bias conditions, where good agreement is obtained for all cases. In order to demonstrate the unique locations of the defect bands, extra hole traps were added around midgap in the SiO_2. These traps do not modify the dominant cases of NBTI/pMOS and PBTI/nMOS but spuriously amplify the other two as shown in **Fig. 8**.

Conclusions: We have demonstrated that all combinations of NBTI/PBTI in n/pFinFETs can be accurately understood at the physical level by considering an electron trap band in the HfO_2 and a hole trap band in the SiO_2 of a high-k gate stack. Correct physical modeling and understanding of all combinations of these instabilities is essential particularly from a circuit perspective where the gate voltages can cover wide ranges of both polarities.
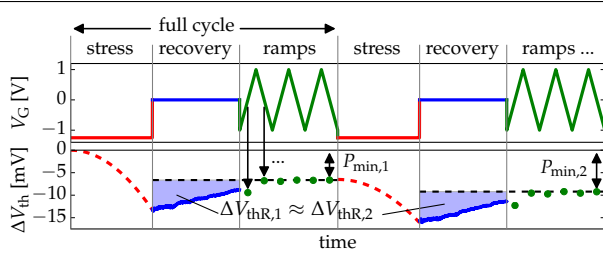
Measurement setup

Figure 1: After stressing a device, V_{th} can be reset to its "fresh" state, except for a "permanent" offset (P_{min}) by applying I_DV_G ramps after stress. Subtracting this offset allows to extract the recoverable part of BTI (ΔV_{thR}) in a fully reproducible manner as depicted in blue.
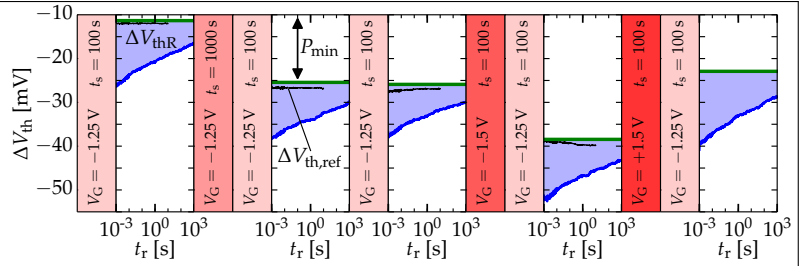
Figure 2: In particular elevated V_G and large t_s can cause a "permanent" shift of ΔV_{th}. Nevertheless, ΔV_{thR} can be measured reproducibly, independently of the stress history. This is shown for the measurement of ΔV_{thR} (blue) for an exemplary stress setup ($V_G = -1.25\,\text{V}$, $t_s = 100\,\text{s}$, $T = 125°\text{C}$).
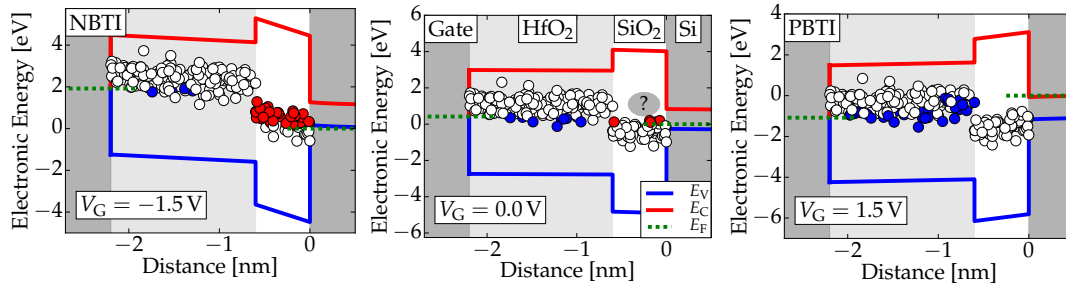
pMOS

Figure 3: The oxide defects used in all simulations (represented by a randomly selected subset) depicted as circles in the band diagram of a pMOS. **NBTI** (left) causes severe hole trapping of SiO_2 defects from the channel (red circles). Additionally, some electrons are released from HfO_2 defects (blue circles). Both contributes to a negative shift of ΔV_{th}. During **PBTI** (right) HfO_2 defects capture electrons from the channel and cause a positive shift of ΔV_{th}. At the same time, these defects are likely to emit electrons to the gate, which leads to tunneling currents. In addition, initially charged SiO_2 defects emit holes, leading to further positive shifts of ΔV_{th}. The question mark denotes a possible defect location as indicated by SiO_2 RTN studies. However, for BTI there was no contribution identified in this region which might be related to a weak contribution of these defects.[21,22]
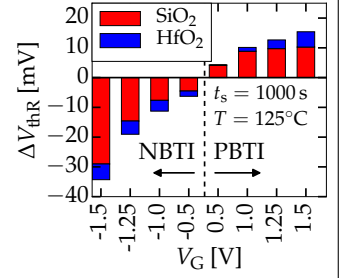
Figure 4: SiO_2 defects are the main contributors to degradation of pMOS devices for both, PBTI and NBTI. However, the share of HfO_2 defect grows towards lager V_G, in particular for PBTI.
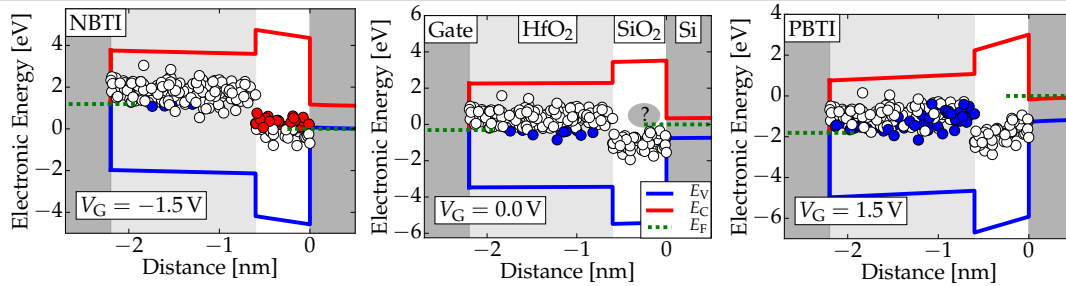
nMOS

Figure 5: Same as in Fig. 3 but for nMOS. **NBTI** (left): For electrostatic reasons, the energetic positions of the defects in the SiO_2 provoke less hole trapping compared to pMOS devices which leads to a smaller impact on ΔV_{th}. For **PBTI** (right) however, the HfO_2 defects are farther below the Fermi level of the channel, compared to pMOS. This causes severe electron trapping, leading to a substantial degradation of the device. Additionally, these defects are likely to contribute to tunneling currents.
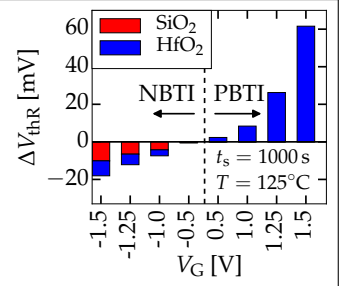
Figure 6: While the HfO_2 is responsible for PBTI degradation in nMOS devices, NBTI is caused by both, SiO_2 and HfO_2.
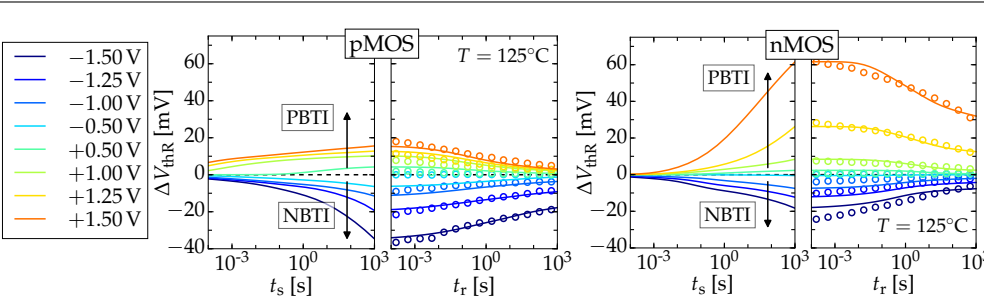
Degradation

Figure 7: The comprehensive experimental results (circles) covering PBTI and NBTI on high-k n and pFinFETs are correctly reproduced by our model (lines). *All* simulations use the *same* microscopic oxide defects. These oxide defects have physical parameters, unique for HfO_2 and SiO_2. The peculiarities of n/pMOSFET degradation are accurately captured based on the correct energetic alignment of the defect bands.
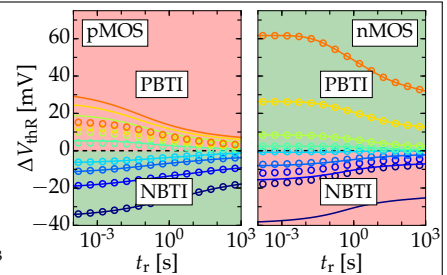
Figure 8: Valid models for pMOS NBTI and nMOS PBTI (green areas) can still substantially overestimate ΔV_{th} for the other cases (red areas) as shown for an increased distribution of traps towards midgap (lines) compared to our reference (circles).

References

[1] T. Grasser *et al.*, T-ED **58**, 3652 (2011). [2] S. Mahapatra *et al.*, T-ED **60**, 901 (2013). [3] C. Shen *et al.*, *IEDM* (2004), p. 733. [4] T. Wang *et al.*, T-ED **53**, 1073 (2006). [5] D. Veksler *et al.*, JAP **115**, 1 (2014). [6] V. Huard *et al.*, MR **46**, 1 (2006). [7] D. Ang *et al.*, T-DMR **8**, 22 (2008). [8] T. Grasser *et al.*, IRPS (2010), p. 16. [9] G. Pobegen *et al.*, MR **51**, 1530 (2011). [10] K. Rott *et al.*, T-DMR **52**, 18911894 (2012). [11] M. Waltl *et al.*, IRPS, p. XT18.1. [12] T. Grasser *et al.*, *IEDM* (2015), p. 401. [13] T. Grasser, MR **52**, 39 (2012). [14] T. Grasser *et al.*, IRPS (2014), p. 4A.5.1. [15] W. Goes *et al.*, SISPAD (2014), p. 77. [16] G. Rzepa *et al.*, SISPAD (2015), p. 144. [17] *Minimos-NT (www.globaltcad.com)*. [18] S. Ramey *et al.*, IRPS (2014), p. XT.2.1 . [19] S. Novak *et al.*, IRPS (2015), p. 2F.2.1 . [20] L. Vandelli *et al.*, T-ED **61**, 2287 (2014). [21] T. Nagumo *et al.*, *IEDM* (2009), p. 759. [22] T. Nagumo *et al.*, *IEDM* (2010), p. 628.