2014 SYMPOSIA ON VLSI TECHNOLOGY & CIRCUITS

Semiconductor industry's premier event on advances in microelectronics technology & circuits

Hilton Hawaiian Village
HONOLULU
June 9-13, 2014

2014 VLSI SYMPOSIA HIGHLIGHTS

The 2014 VLSI Symposia technical program consists of overlapping sessions from June 9 – 12 (Technology) and June 10 – 13 (Circuits), with more than 200 presentations, short courses and panel discussions by the leading researchers and scientists. Program is designed to highlight recent advances in microelectronics technology and circuits, and promote networking amongst participants.

SYMPOSIUM ON VLSI TECHNOLOGY

PLENARY PRESENTATIONS
Tuesday morning, June 10

Device & Technology Implications of the Internet of Things
– Robert Aitken, ARM

Customer Value Creation in the Information Explosion Era
– Keiichiro Shimada, Sony Corporation

RUMP SESSION (panel discussion)
Tuesday evening, June 10

450mm, EUV, III-V, 3D – All in 7nm? Are You Serious?!
– Moderator: Andrzej Strojwas, PDF Solutions
    Expert panelists from Applied Materials, ASML, IBM, imec, Lam Research, Soitec

TECHNOLOGY FOCUS SESSIONS

Embedded NV Memory Technologies
Session T5 (Tuesday, June 10, 3:25pm)

Interconnect: Local & Global
Session T16 (Wednesday, June 11, 8:05am)

PROFESSIONAL DEVELOPMENT OPPORTUNITIES (TECHNOLOGY)

SHORT COURSE

High Performance Mobile SoCs Enabled by 10nm SoC Technology
Monday, June 9

Key Semiconductor Products, Applications & Device Drivers
– CPU Applications – Robert Aitken, ARM
– GPU Applications – Larry Bair, AMD
– Modem/DSP/VPR Applications – Martin Saint-Laurent, Qualcomm
– FPGA Applications – Xin Wu, Xilinx

System On Chip – Applications & Key Aspects
– RF/MS Transceiver & Connectivity – Masoud Zargari, Qualcomm
– RF-Frontend – RFMD

FEOL Scaling & Integration, 3rd Gen FinFET Devices & Architectures
– Andy Wei, GLOBALFOUNDRIES

BEOL Interconnect Scaling, Processes & Integration
– Terry Spooner, IBM

Technology/Design Co-Optimization (FET/circuits, Standard Cell, eMemory, DDR)
– Charles Young, TSMC

Embedded SoC Memory: eSRAM, eNVM & eDRAM
– Gyuhong Kim, Samsung

Variability & DFM
– Andrzej Strojwas, PDF Solutions

2.5D or 3D Packaging for Mobile SIP
– Geert Van der Plas, imec

JOINT PROGRAM HIGHLIGHTS

JOINT FOCUS SESSIONS

- 3D Circuits & Applications
  Session C4 (Wednesday, June 11, 1:30pm)
- 3D Systems & Packaging
  Session T14 (Wednesday, June 11, 3:25pm)
- Design Technology Co-Optimization II
  Session T17 (Thursday, June 12, 10:25am)
- Non-volatile & Emerging Memory
  Session C12 (Thursday, June 12, 1:30pm)
- SRAM & DRAM
  Session C14 (Thursday, June 12, 3:25pm)

JOINT RUMP SESSION (panel discussion)
Tuesday evening, June 10

Who Gives Up on Scaling First: Device & Process Technology Engineers, Circuit Designers or Company Executives? Which Scaling Ends First – Memory or Logic?
– Moderators: Elad Alon, UC Berkeley / Yee Chia Yeo, NUS
– Expert panelists from Intel, NVIDIA, Qualcomm, Renesas, Sandisk, SK Hynix, TSMC, UC Berkeley

LUNCHEON & EXECUTIVE PANEL DISCUSSION
Thursday, June 12

Emerging Semiconductor Industry Trends & Implications
– Moderator: Dan Hutcheson, CEO of VLSI Research, Inc., with senior industry executives from Applied Materials, IBM, Micron, Panasonic, TI, TSMC

JOINT RECEPTION
Tuesday, June 10

JOINT BANQUET
Wednesday, June 11

SATELLITE WORKSHOPS

IEEE Silicon Nanoelectronics Workshop
– June 8&9

Spintronics Workshop
– June 9

SYMPOSIUM ON VLSI CIRCUITS

PLENARY PRESENTATIONS
Wednesday morning, June 11

Data Center 2020: Near-memory Acceleration for Data-Oriented Applications
– Ed Doller, Micron Technology

Technology Development for Printed LSIs Based on Organic Semiconductors
– Jun Takeya, University of Tokyo

RUMP SESSIONS (panel discussion)
Thursday evening, June 12

What Should Circuit Designers do in an Era of System Level Design?
– Moderator: Jan Rabaey, UC Berkeley
Expert panelists from AMD, MediaTek, Qualcomm, Samsung, UC Berkeley, Waseda University, Xilinix

Lessons & Challenges for Future Mixed-Signal, RF & Memory Circuits
– Moderators: Tom Lee, Stanford / Nicky Lu, Etron
Expert panelists from Analog Devices, Micron, Oregon State University, Samsung, Tokyo Institute of Technology, UCLA, University of Twente

PROFESSIONAL DEVELOPMENT OPPORTUNITIES (CIRCUITS)

SHORT COURSES

Advanced Data Converter & Mixed-Signal Circuit Design
Tuesday, June 10

A/D Converter Trends: Power Efficiency & Digitally Assisted Architectures
– Boris Murmann, Stanford University

System Design for Direct Sampling RF Front Ends
– Ray Gomez, Broadcom Corporation

Advances in SAR ADCs with the Scaling of CMOS
– Ron Kapusta, Analog Devices

Ultra-wideband Time-interleaved SAR ADCs for Wireline/Optical Communications
– Lukus Kull, IBM

Digitally Assisted Wireless Transceivers & Synthesizers
– Kenichi Okada, Tokyo Institute of Technology

Digital Error Correction of Time-interleaved A/D Converters
– Asad Abidi, UCLA

Advanced Energy-Efficient Digital Design
Tuesday, June 10

Overview & Advances in Energy Efficient Digital Design
– David Blaauw, University of Michigan

Low Power CPUs for SoC Integration
– David Flynn, ARM

Energy-Efficient System Architectures
– Manish Goel, TI

Fine-Grained Power Management Using Integrated DC-DC Converters
– Jonathan Douglas, Intel

Challenges & Techniques for Ultra-Low Voltage Logic with Nearly-Minimum Energy
– Massimo Alioto, National University of Singapore

Advanced Energy Efficient SRAM Design
– Shinji Miyano, Toshiba

For complete conference and registration information, visit: **http://www.vlsisymposium.org/**

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Electron Devices Society

SSCS

IEEE

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