Technical Highlights from the 2018 Symposia on VLSI Technology & Circuits

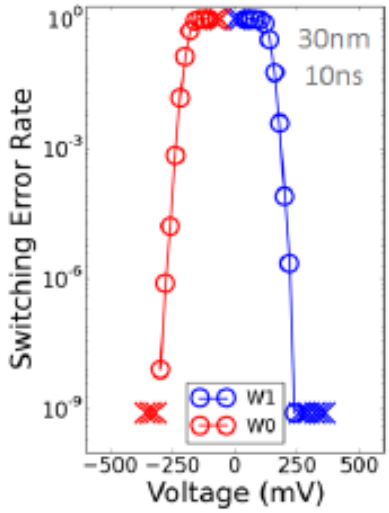
The 2018 Symposia on VLSI Technology & Circuits is a premiere international conference that defines the pace, progress and evolution of microelectronics, scheduled from June 19-21, 2018, in Honolulu, Hawaii. The two Symposia feature a fully overlapping technical program that includes many joint sessions. The Symposia is preceded by full day Short Courses on June 18, and followed by a Friday Forum dedicated to machine learning/AI topics on June 22.

The Symposia's overall theme, **"Technology, Circuits & Systems for Smart Living,"** integrates advanced technology developments, innovative circuit design, and the applications that they enable as part of our global society's transition to a new era of smart, connected devices and systems that change the way humans interact with each other.

Following are some of the highlighted papers that address this theme:

ADVANCED MEMORIES

Low Voltage/Low Power STT MRAM for Embedded LLC Applications
TDK/Headway show that by engineering the tunnel barrier of 30nm devices, writing voltages as low as 0.17V for a 1ppm error rate, 20ns writing operation and 35μA writing current can be achieved. They can further improve the Bit error rate to 10^{-9} for writing voltages of 0.25V, writing currents of 50μA and 10ns pulses while maintaining 400°C thermal budget and requisite retention at 85°C.
Paper T6-4 "Demonstration of Ultra-Low Voltage pSTT-MRAM designed for compatibility with 0x node embedded LLC applications" G. Jan et al., TDK/Headway Technologies

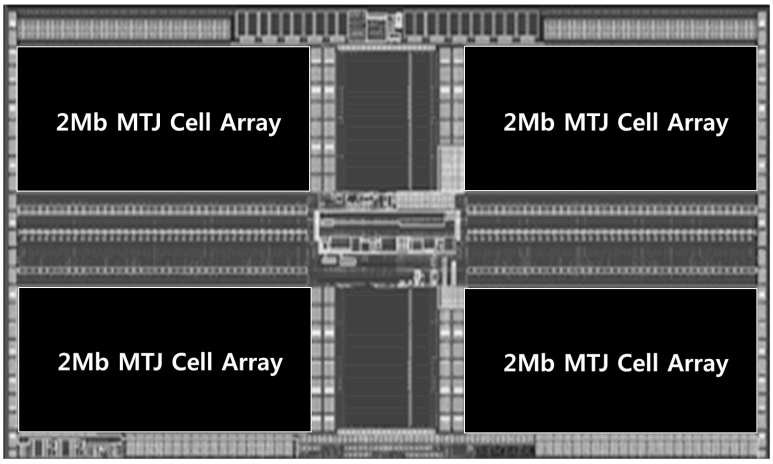


T6-4 Bit error rate of 30nm device using 10ns pulses showing that no error occurred during 10^9 write cycles at those voltages.

Embedded STT-MRAM in a 28FDSOI Logic Process

Samsung electronics will present on a embedded STT-MRAM built on a 28FDSOI process that is operating across the full temperature range (-40°C to 125°C) while exhibiting high endurance (>1e6) on a 8Mb array and retention (>10 years). They also demonstrate robust cell operation at solder reflow conditions (260°C, 90s) and under external magnetic disturbance.

Paper T17.1 "Embedded STT-MRAM in 28-nm FDSOI Logic Process for Industrial MCU/IoT Application" Y. K. Lee, et al., Samsung Electronics



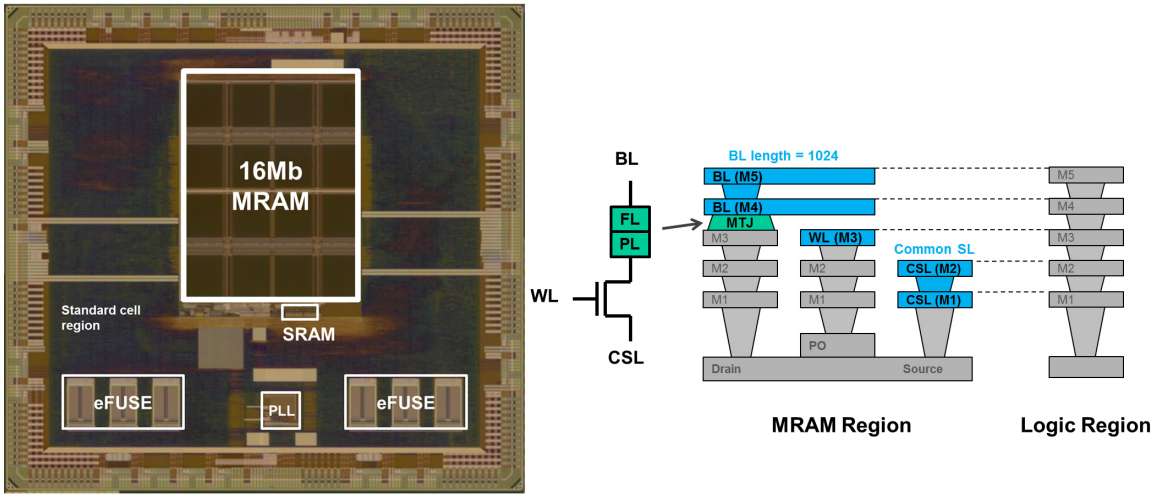
T17.1 Micrographic view of an 8Mb eMRAM macro

16Mb Embedded Perpendicular-MRAM with Hybrid-Resistance Reference.

MRAM is a promising embedded non-volatile memory solution due to its high endurance and data retention capabilities, but its small read window is challenging due to the finite tunnel-magneto-resistance ratio. To this end, TSMC will present an embedded perpendicular-MRAM with a hybrid-resistance-reference that addresses the read window issue. In addition, a trimmed current-mode latch-sense amplifier is described, which

further improves the read window across process variation. The measured results show better than 1μA sense resolution and a fast 17.5ns access time across -40 to 125°C for a 16Mb embedded MRAM in a 40nm CMOS logic process.

Paper C8-1 "Logic Process Compatible 40nm 16Mb, Embedded Perpendicular-MRAM with Hybrid-Resistance Reference, sub-μA Sensing Resolution, and 17.5nS Read Access Time" Y.-C. Shih, et al., TSMC

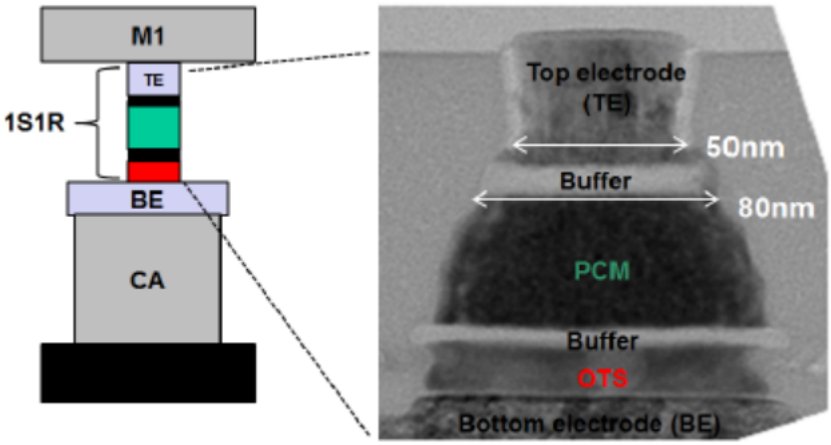


C8-1 Bitcell structure with double metal layers to reduce parasitics and die photo.

OTS-PCM 3D Stackable Memory

Macronix and IBM will present integration of TeAsGeSiSe OTS (Ovonic Threshold Switch) and PCM with Ge2Sb2Te5 into a 3D stackable 1T1S memory pillar. The use of an etch buffer layer and RIE damage-free process resulted in 100% array yield without composition change. Fast selector turn-on/off speed enables 10ns RESET, write endurance of 1e9 cycles and read endurance of 1e11 cycles. Thermal stability demonstrated at 400°C, 30min guarantees cell compatibility for BEOL integration.

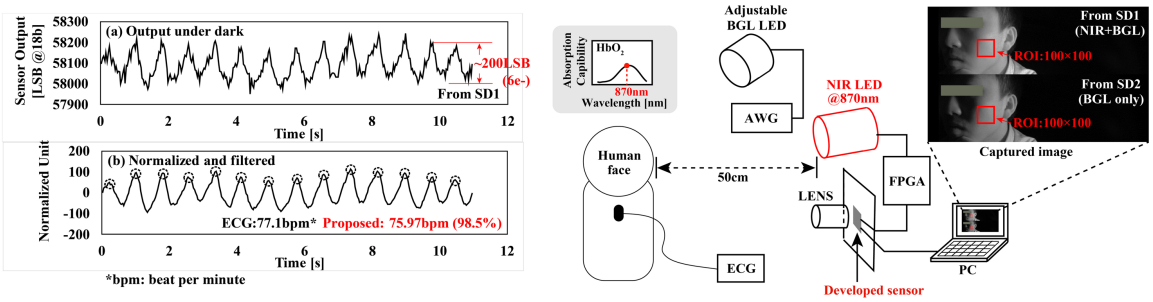
Paper 19-3 "High Endurance Self-Heating OTS-PCM Pillar Cell for 3D Stackable Memory", C.W. Yeh, et al., Macronix, IBM



T19-3 1S1R OTS-PCM pillar memory cell structure.

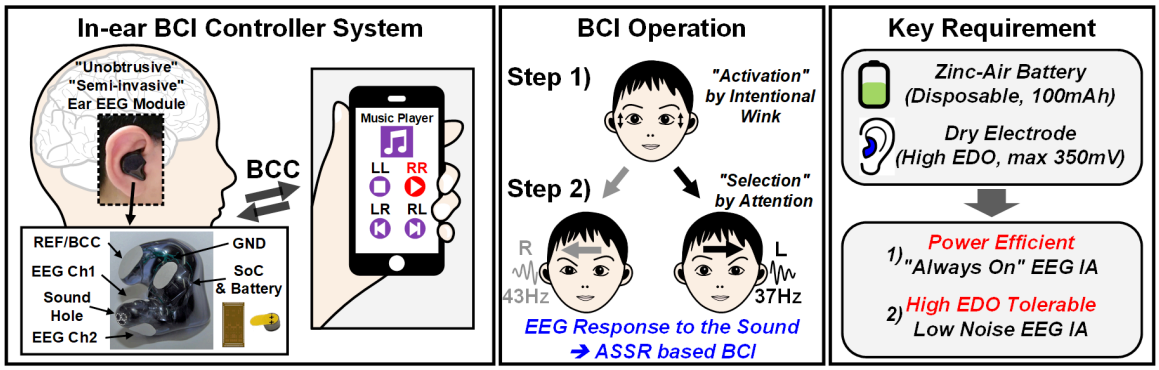
SENSORS, RF, IoT & BIOMEDICAL

Two-Tap NIR Pixel CMOS Image Sensor for Non-Contact Heart Rate Detection
Sensor technologies, whether for the Internet of Things, industrial electronics, or biomedical applications, have been and continue to be an important part of the VLSI Symposia. This year, both Technology and Circuits papers fall into this category. First, C. Cao from Shizuoka University will present a CMOS image sensor using two-tap near infrared lock-in pixels for non-contact heart rate detection. The two-tap pixels are used to cancel background light, achieving >98% detection precision even in the presence of sinusoidal varying bright ambient light, comparable to the latest visible-band-based ISP-assisted method. Fabricated in a 0.11µm CIS technology, the achieved maximum modulation ratio is 90%, as well as a low random noise of 1.1e$^-_{rms}$.
Paper C7-1 "A Two-Tap NIR Lock-In Pixel CMOS Image Sensor with Background Light Cancelling Capability for Non-Contact Heart Rate Detection" C. Cao, et al., Shizuoka University, Brookman Technology, Chiba University



C7-1 Non-contact heart-rate detection system demonstrating 98.5% accuracy.

In-ear Brain-Computer Interface Controller SoC
Work from KAIST, in cooperation with co-authors at the MIT Media Lab, will demonstrate a complete in-ear brain-computer interface controller system-on-chip that includes EEG readout and a body channel communication (BCC) transceiver. Compared to prior work, this fully integrated solution enables EEG measurement that is compact and unobtrusive and achieves higher accuracy than other placements, such as the scalp. The controller is fabricated in 65nm CMOS and dissipates only 83µW with the EEG readout and BCC enabled. A state-of-the-art power efficiency factor of 8.8 is measured.
Paper C12-1 "A 0.8V 82.9µW In-ear BCI Controller System with 8.8 PEF EEG Instrumentational Amplifier and Wireless BAN Transceiver" J. Lee, et al., KAIST, MIT

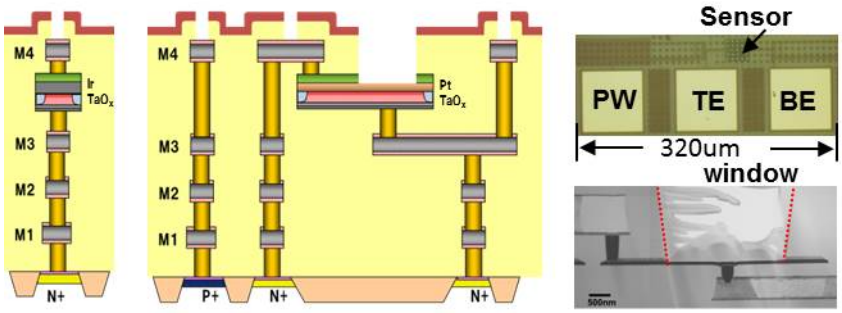


C12-1 In-ear brain-computer interface system diagram and operation.

Hydrogen Sensor Based on RRAM Technology

Panasonic and NIAIST, Japan will present a hydrogen sensor that uses a Ta_2O_5 based 0.18µm RRAM process that exhibits high sensitivity, wide H concentration range (up to 4 vol%) and high gas selectivity. The lack of a heater results in very low power consumption (0.35mW), enabling an ultra low power hydrogen sensor for IOT applications.

Paper T6-3 "From Memory to Sensor: Ultra-Low Power and High Selectivity Hydrogen Sensor Based on ReRAM Technology" Z. Wei, et al., Panasonic Corporation & National Institute of Advanced Industrial Science and Technology, Japan

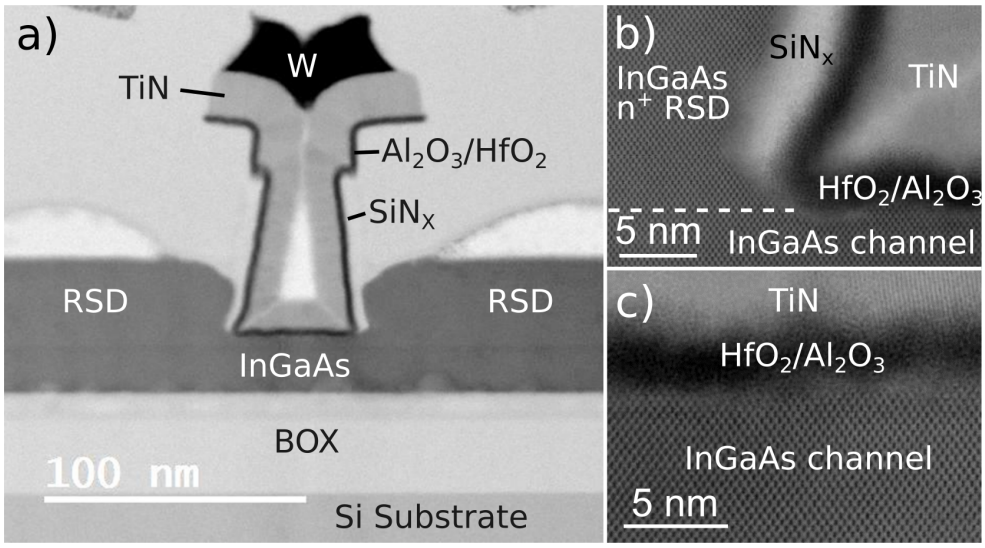


T6-3 Schematic Cross-section of (a) an RRAM cell, (b) H Sensor cell and (c) H sensor chip. (a) TEM X-section of window.

InGaAs-on-Insulator MOSFET with Record RF Performance

IBM will present a InGaAs-on-insulator technology enabling scaled FinFET for low power logic and planar MOSFET for high frequency applications integrated on the same Si wafer with performance of both devices matching state-of-the-art. Simultaneous ft/fmax of 400/100GHz and 215/300GHz is demonstrated, together with strong logic performance in FinFET with I_{ON}=250µA/µm at V_{DD}=0.5V and I_{off}=100nA/µm.

Paper T15-5, "InGaAs-on-Insulator MOSFET Featuring Scaled Logic Devices and Record RF Performance" C.B. Zota, et al., IBM, Fraunhofer IAF.

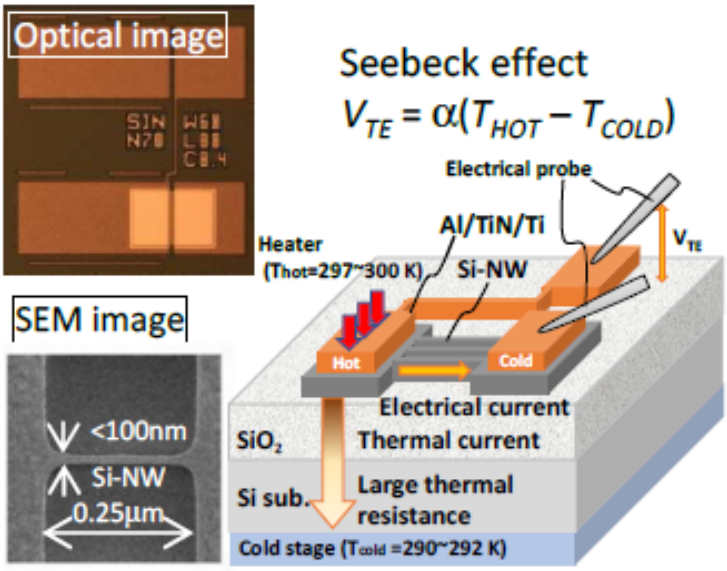


T15-5 STEM cross section InGaAs FET on Insulator (a), S/D region (b) and channel and gate oxide (c).

10µW/cm²-Class Si Nanowire Thermoelectric Energy Harvester

Authors from Waseda University, Osaka University, Shizuoka University and AIST, Japan will present on a CMOS compatible Si nanowire based thermoelectric energy harvester that achieves a 12µW/cm² power density by shortening the Si nanowire to sub-micron scales and suppressing the thermal resistance by thinning the Si-substrate. The demonstrated power realized within these harvesters can be used to drive IoT devices.

Paper T9-1, "10µW/cm²-Class High Power Density Silicon Thermoelectric Energy Harvester Compatible with CMOS-VLSI Technology" M. Tomita et al., Waseda Univ., Osaka Univ., Shizuoka Univ. and AIST Japan



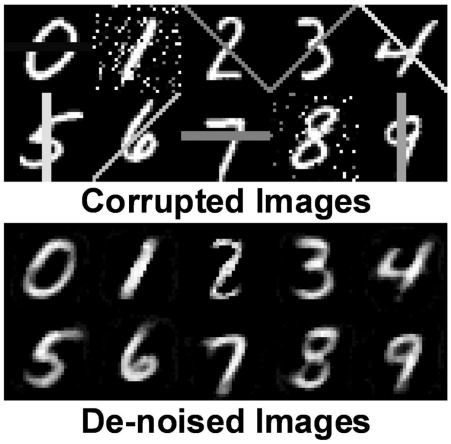
T9-1 Fabrication of Si nanowire thermoelectric harvester where the Si nanowires were patterned using argon fluoride (ArF) immersion lithography.

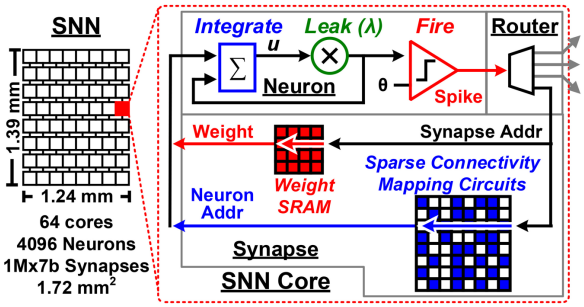
ARTIFICIAL INTELLIGENCE & QUANTUM COMPUTING

Spiking Neural Network with On-chip STDP Learning

A focus on energy efficiency, whether at the core technology or circuit level, is a recurring focus in artificial intelligence (AI) applications. Spiking Neural Networks (SNNs) perform cognitive tasks using sparse spikes, resulting in improved efficiency when compared to CPU designs, and improved scalability and noise margin as compared to mixed-signal designs. G. Chen from Intel will present their SNN chip, which combines sparse connectivity, stochastic operation, voltage scaling, and power gating. As a result, more than 4x higher throughput and 6x energy improvement is gained over previously reported designs. Further, the energy efficiency can be as low as 3.8pJ per synaptic operation (SOP) at 2.6GSOP/s.

Paper C24-1 "A 4096-neuron 1M-synapse 3.8pJ/SOP Spiking Neural Network with On-chip STDP Learning and Sparse Weights in 10nm FinFET CMOS" G. Chen, et al., Intel



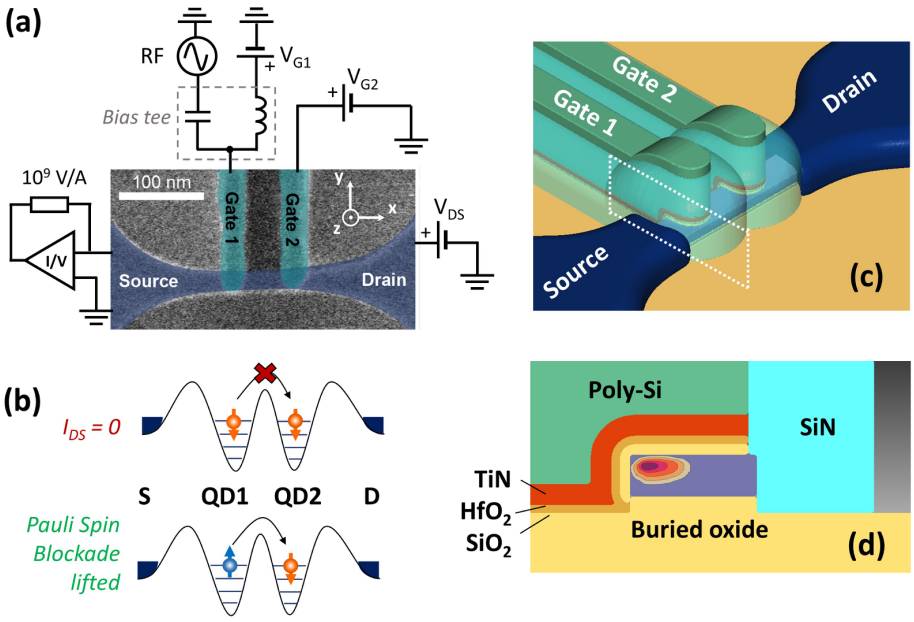


C24-1 Spiking neural network overview (left), along with de-noised MNIST images (right).

Electrical Control of Qubit in SOI CMOS Technology

Leti will demonstrate experimental evidence of Quantum Dot (QD) device with the spin of electrons fully controlled by electrical field. The back-gate control of the device fabricated in a standard SOI CMOS technology enables switching a quantum bit between electrically addressable, yet charge noise-sensitive configuration, and a protected configuration.

Paper T12-1 "All-Electrical Control of a Hybrid Electron Spin/Valley Quantum Bit in SOI CMOS Technology" L. Hutin, et al., CEA LETI, CEA INAC and CNRS



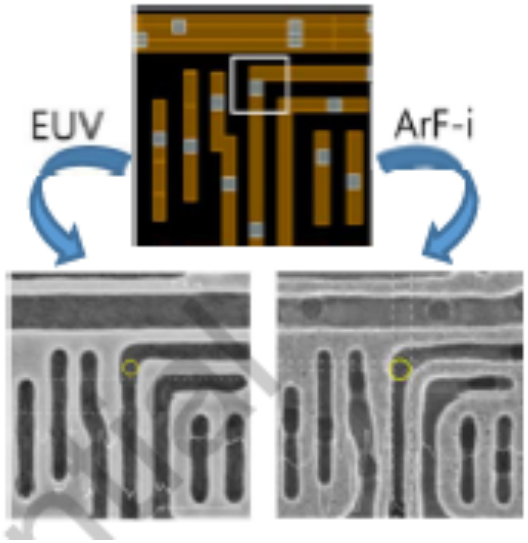
T12-1 Schematic and top view SEM of the two-gate device with measurement setup description. Spin filtering mechanism across the double QD, (d) Cross-section along a gate and representation of the asymmetrical electron wavefunction along the mesa edge.

ADVANCED PLATFORM & SOCs

7nm Platform Paper with EUV

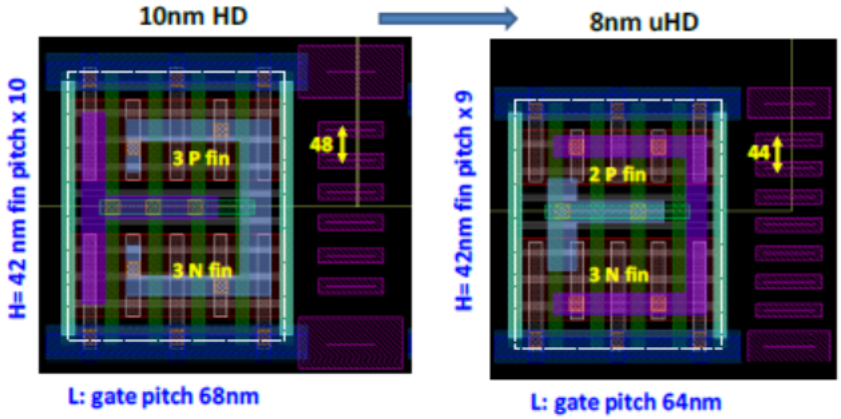
Samsung Electronics will present a 7nm platform technology that utilizes single patterning EUV for MOL and BEOL levels with a fin pitch and CPP of 27nm and 54nm, respectively. They show 20-30% AC performance improvement and 50-60% reduction in power compared to their 10nm technology. They report on the smallest transistor size and SRAM cell size of 0.0262µm^2 for a mainstream technology and use special constructs and single diffusion break for further area scaling. They have demonstrated 256Mbit SRAM and large scale logic (including CPU and GPU) while meeting the requisite NBTI reliability requirements.

Paper T6-1 "True 7nm Platform Technology Featuring Smallest FinFET and Smallest SRAM Cell by EUV, Special Constructs and 3rd Generation Single Diffusion Break"
WC Jeong, et al., Samsung Electronics



T6-1 Demonstration that EUV 2D fidelity is 70% better than ArF.

High Performance SoC with 2nd Generation 10nm FINFET Technology
Qualcomm and Samsung will present their new mobile SoC Snapdragon SDM845 fabricated in the 2nd generation 10nm FinFET technology (10LPP). SDM845 exhibits 30-40% CPU/GPU performance gain over its first generation, together with 10% battery life increase driven by new design features and technology improvements in transistor performance and uniformity. Further technology scaling to 8nm node (8LPP) with gate and metal pitch reduction enabled by LE^4 patterning results in 15% smaller logic circuits area over 10nm technology node.
Paper T18-4 "High Performance Mobile SoC Productization with Second-Generation 10nm FinFET Technology and Extension to 8-nm Scaling" Y. Yuan, et al., Qualcomm, Samsung

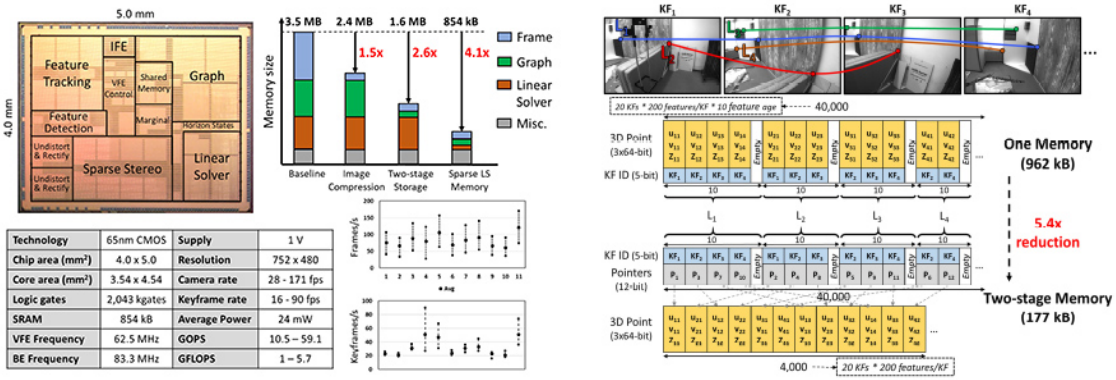


T18-4 Standard cell scaling from 10nm HD cell to 8nm uHD cell with gate pitch scaled from 68nm to 64nm, Mx from 48nm to 44nm with LE^4 process.

Energy-Efficient Odometry Accelerator for Autonomous Nano Drone Navigation

One of the highlighted topics for the 2018 Symposia is *Robotics and Autonomous Transportation*. This topic is at the heart of a paper from MIT on Navion, which is the first fully integrated odometry accelerator for autonomous miniaturized robots. The chip uses inertial measurements and mono-stereo images to estimate a drone's trajectory, as well as to generate a 3D map of the environment. The on-chip integration reduces energy and footprint, and it eliminates costly off-chip processing and storage. Fabricated in 65nm CMOS, it can process 752x480 stereo images at up to 171fps and inertial measurements at up to 52kHz. Further, the chip is configurable to maximize accuracy, throughput, and energy-efficiency across various environmental conditions.

Paper C13-1 "Navion: A Fully Integrated Energy-Efficient Visual-Inertial Odometry Accelerator for Autonomous Navigation of Nano Drones" A. Suleiman, et al., MIT



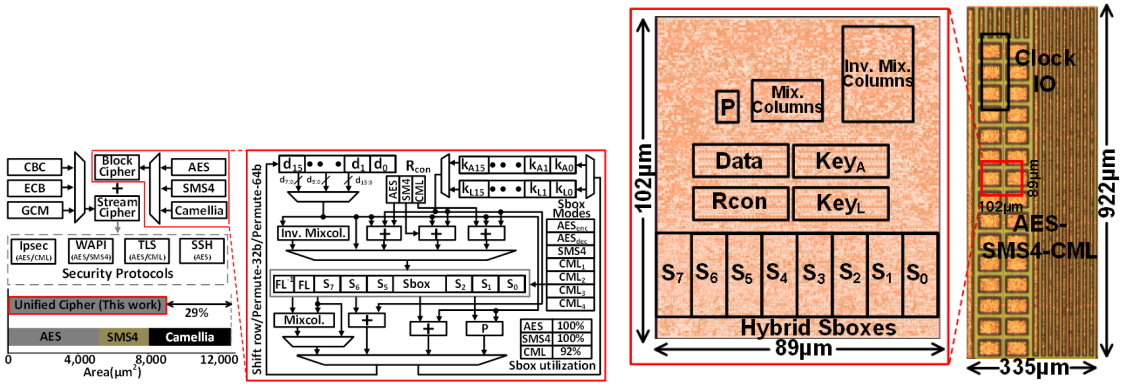
Technology	65nm CMOS	Supply	1 V
Chip area (mm²)	4.0 x 5.0	Resolution	752 x 480
Core area (mm²)	3.54 x 4.54	Camera rate	28 - 171 fps
Logic gates	2,043 kgates	Keyframe rate	16 - 90 fps
SRAM	854 kB	Average Power	24 mW
VFE Frequency	62.5 MHz	GOPS	10.5 – 59.1
BE Frequency	83.3 MHz	GFLOPS	1 – 5.7

C13-1 Tracking of features through keyframes (top) and memory usage reduction (bottom).

14nm Tri-gate CMOS Reconfigurable Symmetric-key Cipher Accelerator SoC

Similar to autonomous functionality, security and cryptography is another rapidly evolving area for circuits. This year, S. Satpathy from Intel will present a reconfigurable symmetric-key cipher accelerator fabricated in 14nm CMOS, a critical component of content protection and authentication protocols. This SoC supports multiple standard and geo-specific ciphers, including AES, SMS4, and Camellia. The design features a LUT-free unified implementation for all three ciphers, leveraging polynomial iso-morphism for acceleration and a shared $GF(2^4)^2$ datapath to enable ultra-low voltage operation. Measured results demonstrate operation down to 0.22V supply with only 7µW total power. At higher 0.75V supply, roughly 3Gbps throughput is achieved at 600MHz operation, while still only dissipating ~25mW.

Paper C16-4 "220mV-900mV 794/584/754 Gbps/W Reconfigurable $GF(2^4)^2$ AES/SMS4/Camellia Symmetric-Key Cipher Accelerator in 14nm Tri-gate CMOS" S. Satpathy, et al., Intel



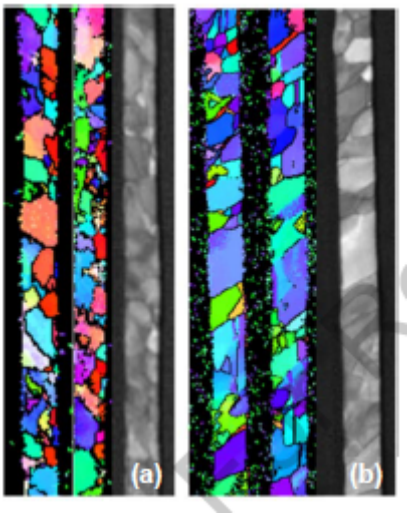
C16-4 Unified cipher accelerator datapath (left) and die photo (right).

ADVANCED TRANSISTOR TECHNOLOGY

Nanosecond Laser Anneal for BEOL Performance Boost

GLOBALFOUNDRIES will present their results on laser-induced grain growth within Cu interconnects. They demonstrate a 30% reduction in Cu line resistance, which delivers a 15% improvement in RC and improvement in IDsat of 2-5%. The performance improvement is concomitant with improved dielectric VBD and Cu EM reliability, without impact on ULK mechanical stability, thereby providing a path for Cu interconnect extendability

Paper T6-2, "Nanosecond Laser Anneal for BEOL Performance Boost in Advanced FinFETs" R.T.P. Lee, et al., GLOBALFOUNDRIES)

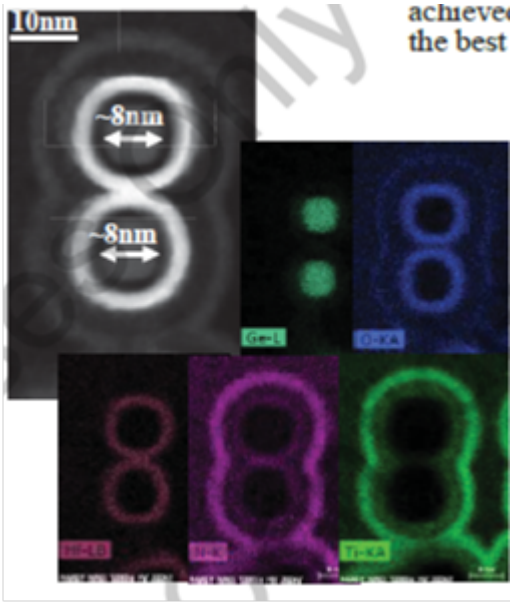


T6-2 Orientation, Phase and TEM maps of Cu lines for (a) Control (b) Devices with ns laser anneal

Vertical Ge Nanowire PFET

imec will present progress in development of p-type Ge Gate-All-Around devices fabricated on 300mm SiGe Strain-Relaxed-Buffer (SRB) demonstrating two vertically stacked strained Ge nanowires. Thanks to process optimization and uniaxial stress along the Ge wire of 1.7GPa, 8nm GAA features increased Q factor of 25, I_{on} of 500µA/µm at I_{off} of 100nA/µm, which is within the range of the best published results on Ge FinFETs.

Paper T20-2 "First demonstration of vertically stacked Gate-All-Around highly-strained Germanium nanowire p-FETs" E. Capogreco, et al., imec



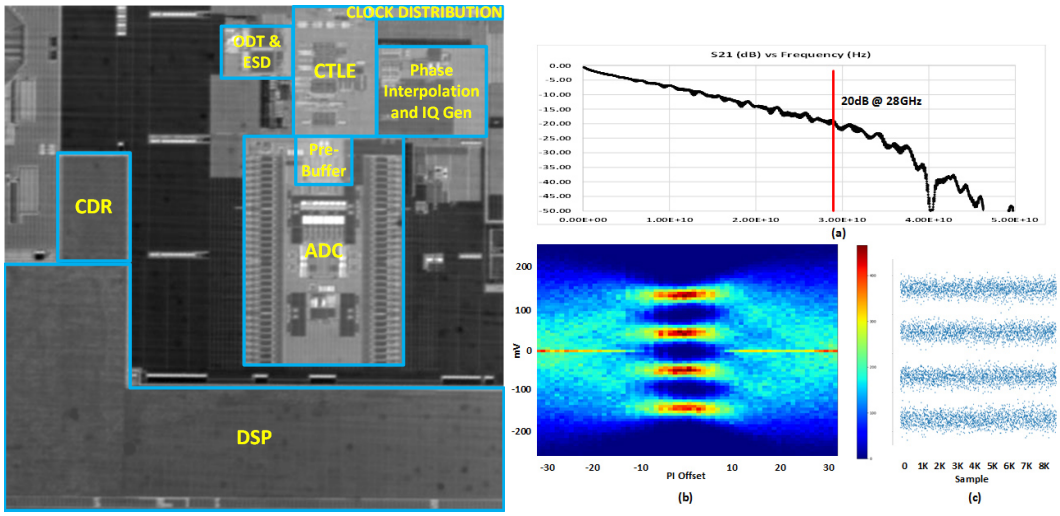
T20-2 8nm double Ge NW with RMG.

WIRELINE & CONVERTER CIRCUITS

World's First Integrated 112Gb/s PAM4 Receiver

Wireline technology has been pushing analog-to-digital converter technology to increasingly higher speeds, enabling ultra-high data rate electrical interfaces. At the 2018 Symposium on VLSI Circuits, this is evidenced by the publication of the world's first integrated 112Gb/s PAM4 receiver. The work, by J. Hudner from Xilinx, is implemented in 16nm FinFET and utilizes 64-way interleaved SAR ADCs. Using peaked-follower buffering, multi-rank sampling, and timing skew calibration, the ADC samples at 56GS/s and allows for digital correction of channel impairments. The receiver consumes 590mW and achieves a pre-FEC raw BER of $2x10^{-5}$ over a channel with 20dB loss.

Paper C5-2 "A 112Gb/s PAM4 Wireline Receiver Using a 64-way Time-Interleaved SAR ADC in 16nm FinFET" J. Hudner, et al., Xilinx

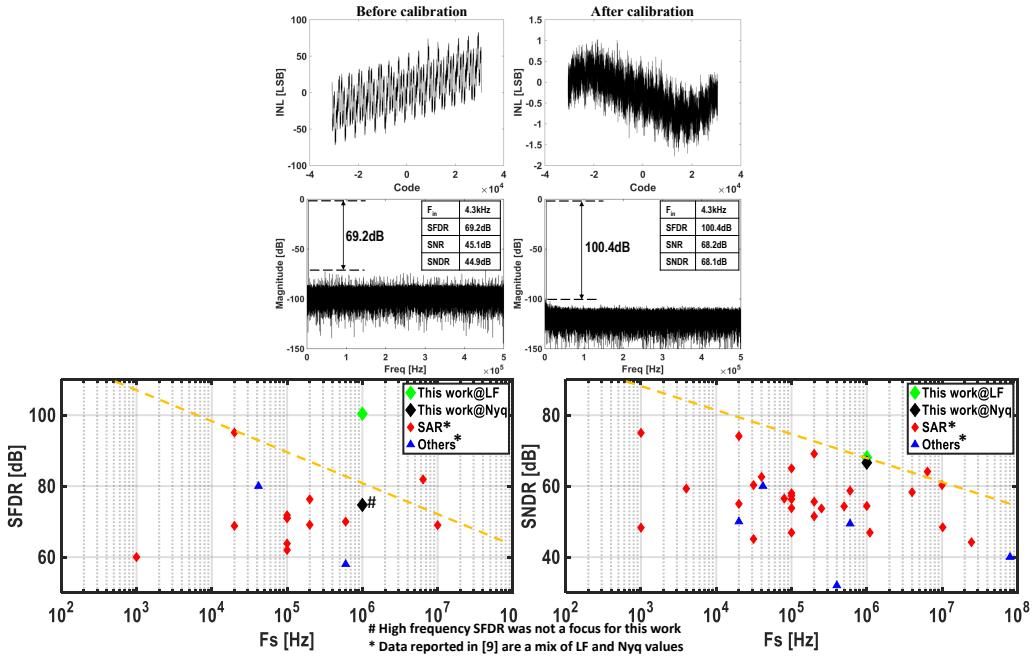


C5-2 112Gb/s PAM4 receiver (a) chip photo and (b,c) eye diagram with data samples.

Data Converter with On-Chip Input-Signal-Independent Calibration

In the area of higher linearity data converters, a paper from Analog Devices by J. Shen demonstrates a signal-independent background calibration technique. This technique uses double-conversion and improves AC linearity by more than 30dB, achieving 16-bit level static non-linearity. More significantly, the calibration is shown to work with any input signal and converges within a few milliseconds. The overall converter consumes roughly 100µW at 1MS/s while achieving 100dB SFDR, despite being implemented in a very scaled 40nm CMOS process.

Paper C9-1 "A 12-bit 31.1uW 1MS/s SAR ADC with On-Chip Input-Signal-Independent Calibration Achieving 100.4dB SFDR using 256fF Sampling Capacitance" J. Shen, et al., Analog Devices



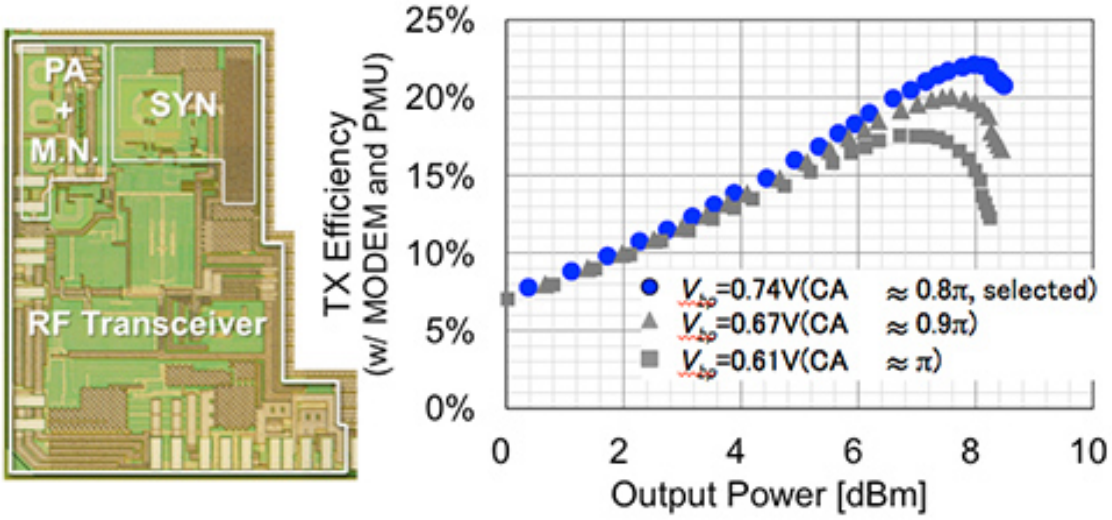
C9-1 >30dB linearity improvement (left-to-middle) from ADC background calibration along with state-of-art comparison graph (right).

WIRELESS CIRCUITS & FREQUENCY GENERATION

Bluetooth-5 SoC

Bluetooth Low Energy (BLE) is emerging as a leading candidate for wirelessly connected IoT devices, and this requires high-efficiency and high-output-power transmitters. To this end, Toshiba Corporation will present a System-on-Chip supporting Bluetooth-5 features. An 8dBm power amplifier is proposed, utilizing waveform symmetric feedback to suppress harmonic distortion. The SoC also includes an RX for a complete solution. It is implemented in 65nm CMOS, and the measured TX efficiency is 22% when delivering 8dBm output power. The overall SoC achieves 113dB link-budget and achieves harmonic levels well below the FCC limit of -41.3dBm/MHz.

Paper C3-2 "An 113dB-Link-Budget Bluetooth-5 SoC with an 8dBm 22%-Efficiency TX" T. Wang, et al., Toshiba

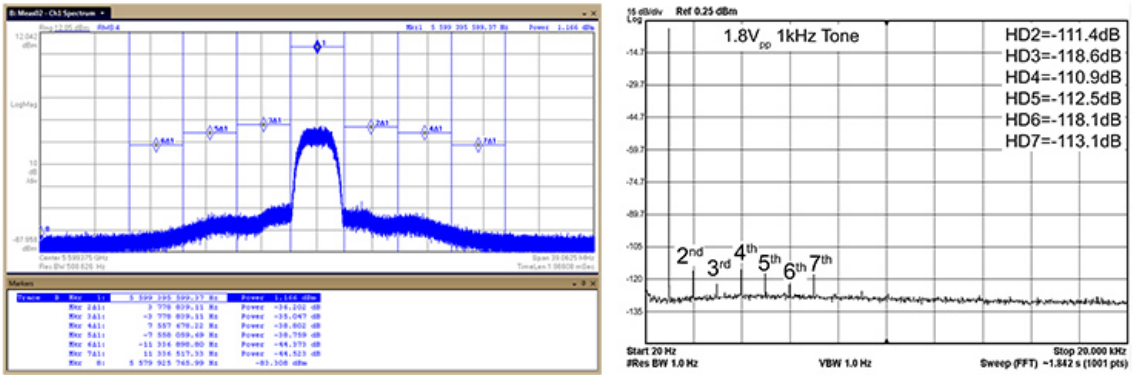


C3-2 Die photo of Bluetooth-5 SoC.

5.5 GHz Background-Calibrated Sub-sampling Polar Transmitter

A paper by N. Markulic and co-authors at imec describes the first sub-sampling polar transmitter. It is implemented in 28nm CMOS and consists of a low-noise phase modulating digital subsampling PLL and a digital power amplifier (DPA) for amplitude modulation. Unlike a conventional design, the DPA is placed within the PLL with phase-error detection directly at the DPA output. The amplitude sensitivity of the phase detector enables AM distortion to be canceled automatically, improving EVM by more than 14dB. In transmit mode, with -2.7dBm average output power, the chip consumes 46mW and achieves -41.3dB EVM, with measured ACLR1/2/3 of -36dB/-38dB/-44dB, respectively.

Paper C20-3 "A 5.5 GHz Background-Calibrated Subsampling Polar Transmitter with -41.3 dB EVM at 1024 QAM in 28nm CMOS" N. Markulic, et al., imec, Vrije Universiteit Brussel

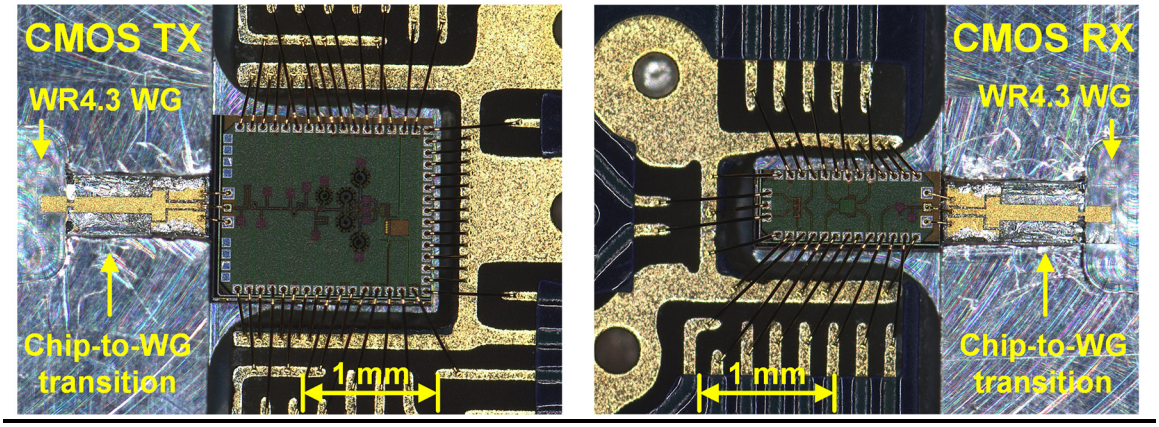


C20-3 ACLR1/2/3 measurements of sub-sampling polar transmitter.

CMOS Molecular Clock

Many systems, wireless or otherwise, require highly stable reference frequencies. This is particularly true for on-chip spectroscopic systems. As an alternative to traditional atomic clocks, C. Wang from MIT is proposing to use the 231.061GHz spectral line of carbonyl sulfide, and has demonstrated the first chip-scale molecular clock. In comparison to atomic clocks, the proposed clock does not require the power-consuming heaters for alkali evaporation and is, by nature, less sensitive to external electromagnetic fields. The measured phase noise is -68.4dBc/Hz at an offset of 1MHz while consuming 66mW. In addition, the clock is quite stable at 3.8×10^{-10}, as measured by Allan deviation, and the startup time of 1sec is dramatically faster than chip-scale atomic clock alternatives.

Paper C11-1 "A CMOS Molecular Clock Probing 231.061-GHz Rotational Line of OCS with Sub-ppb Long-Term Stability and 66-mW DC Power" C. Wang, et al., MIT



C11-1 Photograph of wire-bonded CMOS transmitter and receiver for molecular clock.

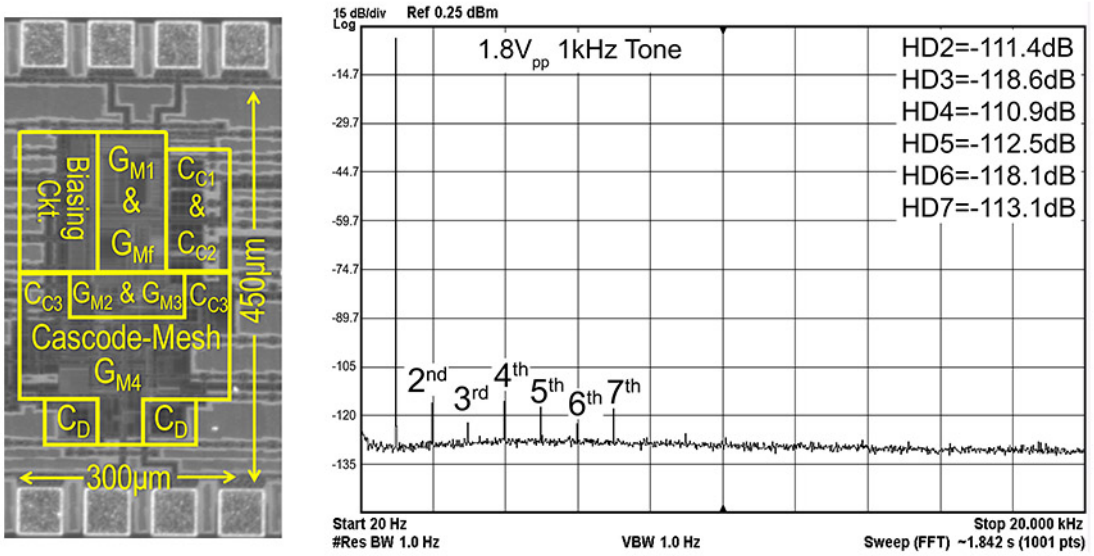
ANALOG CIRCUITS

High-Fidelity Headphone Driver in 65nm CMOS

An extremely high linearity, high SNR headphone driver will be presented by UC Berkeley and TU Delft. It is implemented as a class-AB driver and, targeting modern

mobile devices, is implemented in 65nm CMOS. To improve on the typically challenged distortion in CMOS amplifiers, the proposed design uses improved output stage biasing and a new frequency compensation scheme. As a consequence, it is able to achieve significantly improved performance relative to comparable CMOS designs, including >12dB better linearity and >15dB higher SNR while delivering nearly 50% more power to the load.

Paper C22-1 "A 1mW -101dB THD-N Class-AB High-Fidelity Headphone Driver in 65nm CMOS" N. Mehta, et al., University of California, Berkeley, TU Delft



C22-1 65nm headphone driver with better than -100dB distortion.