Technical Highlights from the 2025 Symposium On VLSI Technology and Circuits

The 2025 Symposium on VLSI Technology and Circuits is a premiere international conference that records the pace, progress, and evolution of micro/nano integrated electronics, scheduled for June 8-12, 2025. The Symposium will be held in-person at the Rihga Royal Hotel, Kyoto Japan to foster networking opportunities.

The Symposium's overall theme, **" Cultivating the VLSI Garden: From Seeds of Innovation to Thriving Growth "** integrates advanced technology developments, innovative circuit designs, and the applications that they enable as part of our global society's transition to a new era of smart connected devices, infrastructure and systems that change the way humans interact with each other.

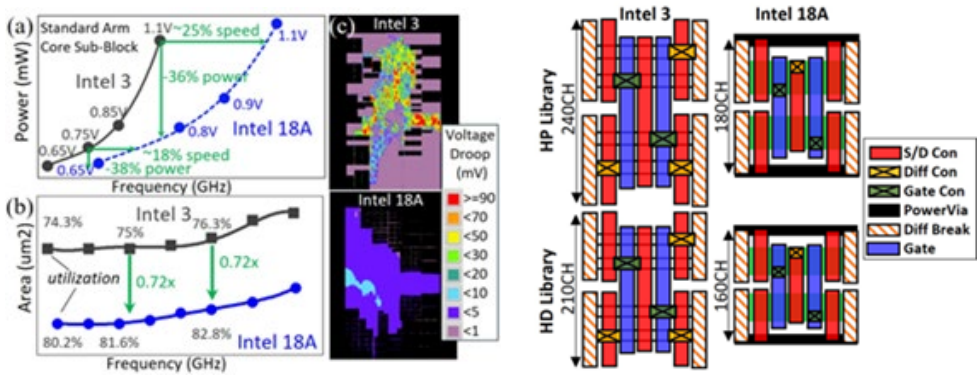
The following are some of the highlight papers that address this theme:

Technology Highlights

Advanced CMOS Technology

"Intel 18A Platform Technology Featuring RibbonFET (GAA) and Power Via for Advanced High-Performance Computing" – Intel (Paper T1-1)

An advanced Intel 18A technology featuring RibbonFET and Power Via provides over 30% density scaling and a full node of performance improvement compared to Intel 3. Intel 18A offers high-performance (HP) and high-density (HD) libraries with full-featured technology design capabilities and enhanced design ease of use.

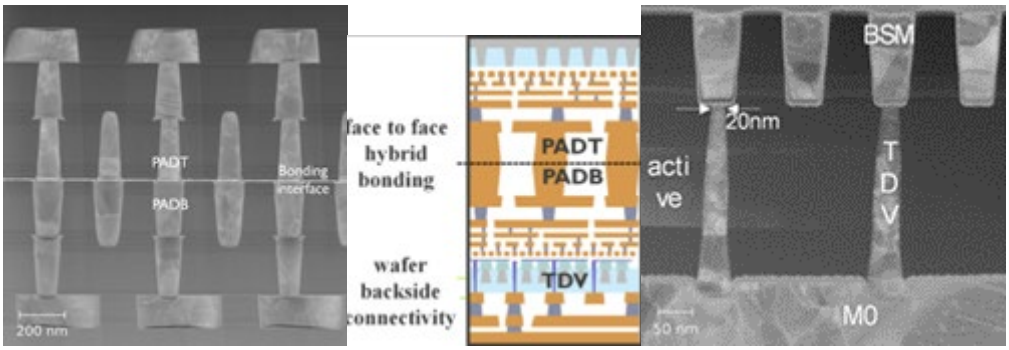


Figures：(Left)Intel 18A vs. Intel 3 PPA (Power, Performance, Area) comparison (Right) Intel 18A vs Intel 3 High Density Library, High Performance Library

Advanced Packaging

"High-density wafer level connectivity using frontside hybrid bonding at 250nm pitch and backside through-dielectric vias at 120nm pitch after extreme wafer thinning" – imec (Paper T6-1)

imec demonstrates high-density wafer level connection using face-to-face hybrid bonding at 250nm pitch and backside through-dielectric vias at 120nm pitch. Access from the wafer backside is demonstrated through extreme wafer thinning beyond shallow trench isolation floor.



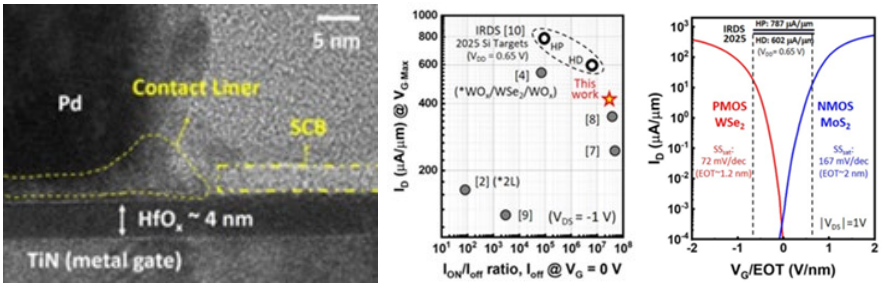
Figures: (Left) face-to-face hybrid bonding at 250nm pitch, (middle) schematic image of face to face hybrid bonding and backside connection in a heterogeneous 3D package, and (right) front to backside connection with through dielectric vias (TDV).

Process and Materials for CMOS Scaling and New Devices

"Performance Step-up in PMOS with Monolayer WSe_2 Channel" – Taiwan Semiconductor Manufacturing Company (TSMC) (Paper T1-4)

TSMC demonstrates that back-gated PMOS with monolayer (1L) WSe_2 channel and equivalent gate oxide thickness of 1.2 nm reaches ON-current of 400 μA/μm at V_{DS} of -1 V with subthreshold swing of 72 mV/dec., ON/OFF ratio of 7 orders, nearly hysteresis-free

characteristics, while operating in enhancement-mode. These results make 1L WSe_2 more competitive as a scaled p-channel candidate.

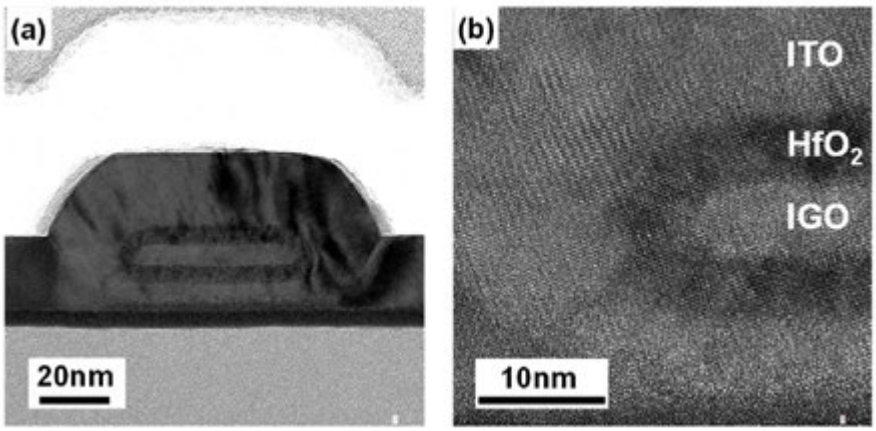


Figures: (Left) High resolution cross-sectional TEM image of a WSe_2 device with the physical back-gate dielectric thickness of 4 nm, sacrificial contact buffer (SCB) layer, and contact liner. (Middle) Benchmark of ON current versus ON/OFF ratio, (Right) Potential combination of PMOS-WSe_2 and NMOS-MoS_2 compared with IRDS 2025 targets.

Process and Materials for CMOS Scaling and New Devices

"A Gate-All-Around Nanosheet Oxide Semiconductor for Transistor by Selective Crystallization of InGaOx for Performance and Reliability Enhancement" – The University of Tokyo, AIST and Nara Institute of Science of Technology (Paper T6-3)

The University of Tokyo and Nara Institute of Science and Technology demonstrated outstanding mobility improvement with crystalline InGaOx grown by ALD process in comparison to conventional amorphous material. They also found the optimum composition ratio for mobility and bias stress reliability. Furthermore, they developed an integration process flow of gate-all-around nanosheet transistors with crystalline InGaOx, and demonstrated normally-off operation and high bias stress reliability. This research achievement will promote device scaling of oxide semiconductor transistors for LSI applications.

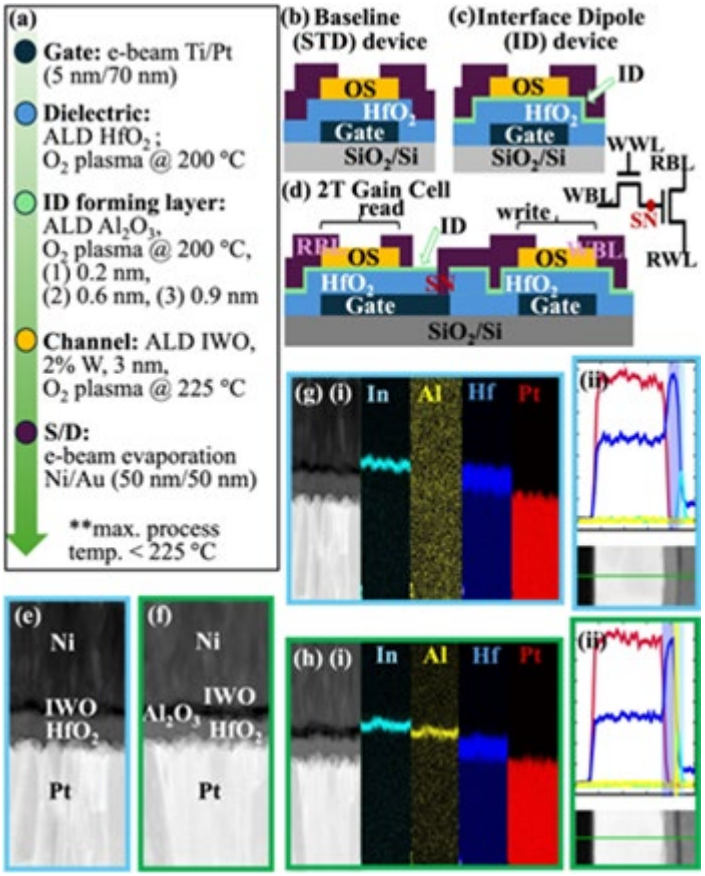


Figures: Cross sectional TEM images of the gate-all-around nanosheet InGaOx transistor fabricated in this research. The right figure is a magnified one of the left.

Process and Materials for CMOS Scaling and New Devices

"Orthogonal V_T Tuning for Oxide Semiconductor 2T Gain Cell enabled by Interface Dipole Engineering" – Stanford University and Taiwan Semiconductor Manufacturing Company (TSMC) (Paper T19-1)

Interface engineering of the gate dielectric as an independent knob to tune the threshold voltage of Oxide Semiconductor FETs for two-transistor gain-cell memories. By leveraging Interface Dipole engineering for Indium-Tungsten-Oxide(IWO) FETs, 450-500mV threshold voltage increase compared to the standard HfO2, maintaining ΔVt from 85℃ to cryogenic temperatures, was achieved.



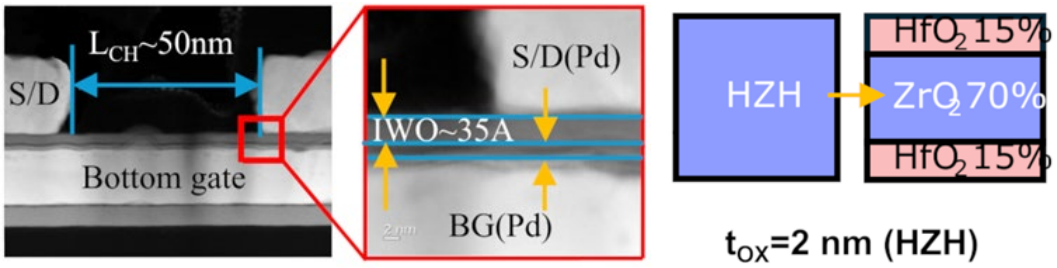
Figures: Process flow of Oxide Semiconductor gain-cell with Interface Dipole engineering. Cross-sectional TEM images along with EDS elemental maps.

Device Physics, Characterization, Modeling and Reliability

"Demonstration of Tungsten-doped Indium Oxide MOSFETs with 3 Angstrom EOT, Improved Stability and High On-Current" – Georgia institute of Technology and Samsung Electronics Co., Ltd (Paper T1-3)

Georgia Institute of Technology and Samsung Electronics demonstrates high on-current and improved stability in W-doped In_2O_3 (IWO) channel MOSFETs. Employing HfO_2-ZrO_2-HfO_2 (HZH) laminated gate dielectric enables EOT scaling down to 0.3 nm, resulting in a high on-state current of 244 μA/μm. Additionally, the HZH gate stack effectively suppresses both

positive and negative bias instabilities. The presented IWO MOSFETs with the HZO gate stack paves the way for developing reliable 3D-integrated circuits using BEOL process.

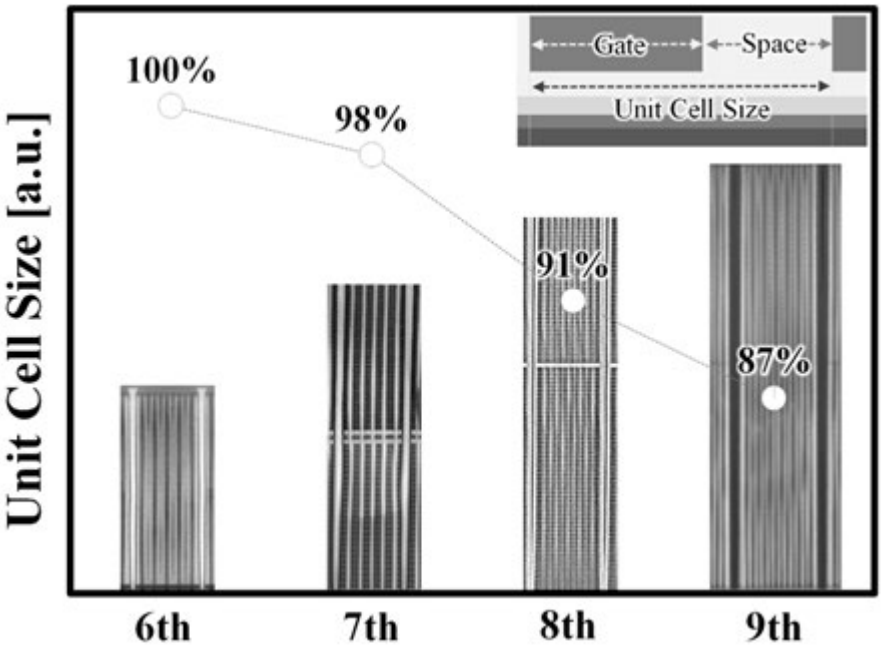


Figures: (Left) Cross-sectional STEM showing L_{ch} = 50 nm, 3.5 nm IWO channel, and 2 nm HZH gate stack. (Right) $HfO_2/ZrO_2/HfO_2$ thickness composition in the HZH stack.

Memory Technology

"Highly Scalable and Reliable Cell Characteristics for 1Tb 9th Generation 3D-NAND Flash Technology" – Samsung Electronics Co.,Ltd (Paper T1-5)

Samsung details the 286-layer 9th generation 3D-NAND flash memory. Bit density was improved by 50% compared to previous generation owing to aggressive scaling down in both vertical and lateral dimensions. Advanced ONO material engineering overcame the reliability concerns due to the extreme scaling, offering highly reliable 3D-NAND with the smallest cell volume.

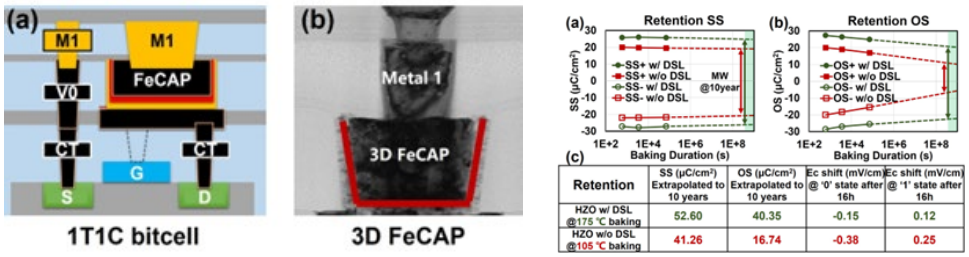


Figures. Vertical cross-sectional SEM views and unit cell size of 3DNANDflash memory across each generation from the 6th to the 9th.3D-NAND flash memory.

Memory Technology

"1T1C 3D HZO FeRAM with High Retention (>125℃) and High Endurance (>1E13) for Embedded Nonvolatile Memory Application" – Huawei Technologies Co., Ltd (Paper T6-5)

Huawei announces a high-performance 1T1C 3D FeRAM test chip utilizing hafnium zirconium oxide (HZO) material. This test chip features a trench-structured ferroelectric capacitor (FeCAP) composed of a 7nm thick HZO film formed on a 40nm CMOS platform, achieving 10 years of data retention and stable operation at 125°C. Additionally, thanks to a new stack design with defect shielding layers (DSL) placed on both sides of the HZO film, common issues in ferroelectric memory such as fatigue, imprint, and the pinch phenomenon have been effectively suppressed. The memory array boasts a capacity of 32Mb, demonstrating a memory window of approximately 340mV even at -5.2σ (0.1ppm), and maintains a memory window of over 200mV after 10^{11} write cycles and 10^{13} read cycles, as well as high-temperature baking at 125°C. These results significantly enhance the potential of replacing eFlash in embedded non-volatile memory (eNVM) applications.

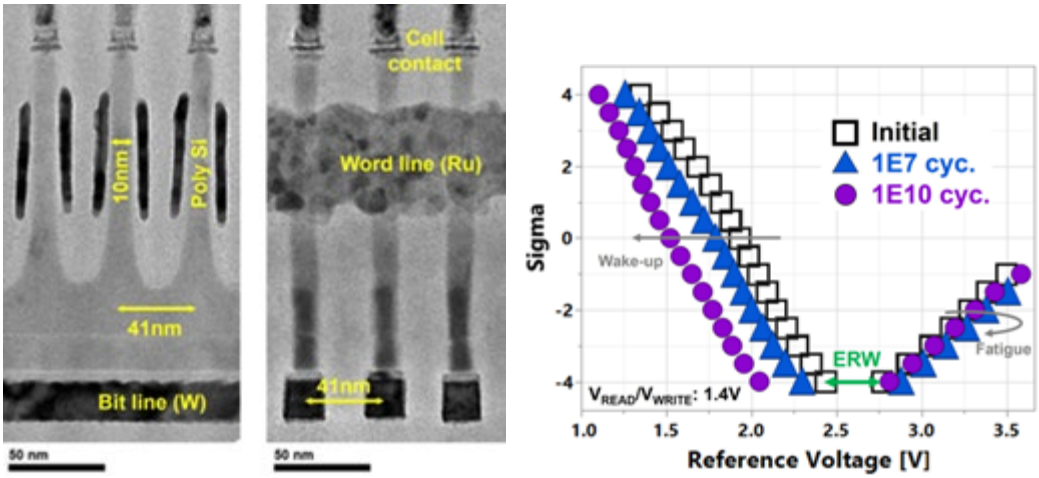


Figures: (Left) The schematic structure and TEM cross section of the 3D FeRAM (Right) Retention characteristics

Memory Technology

"Voltage Reduction (1.4V) and Array Scaling (41nm) of Ferroelectric NVDRAM for Low-Power and High-Density Applications" – Micron Technology Inc., (Paper T6-2)

A second generation of scaled Ferroelectric NVDRAM with a reduced x- and y-direction pitch (41nm), a thinner ferroelectric stack (5nm) and a lower array operation voltage (Read/write at 1.4V). Full chip array data shows a >250mV window at -4 σ after 1E10 cycles. This is the densest 1T1C ferroelectric technology with such high performance. Multiple material and electrical challenges addressed to ensure performance was maintained at reduced dimensions.

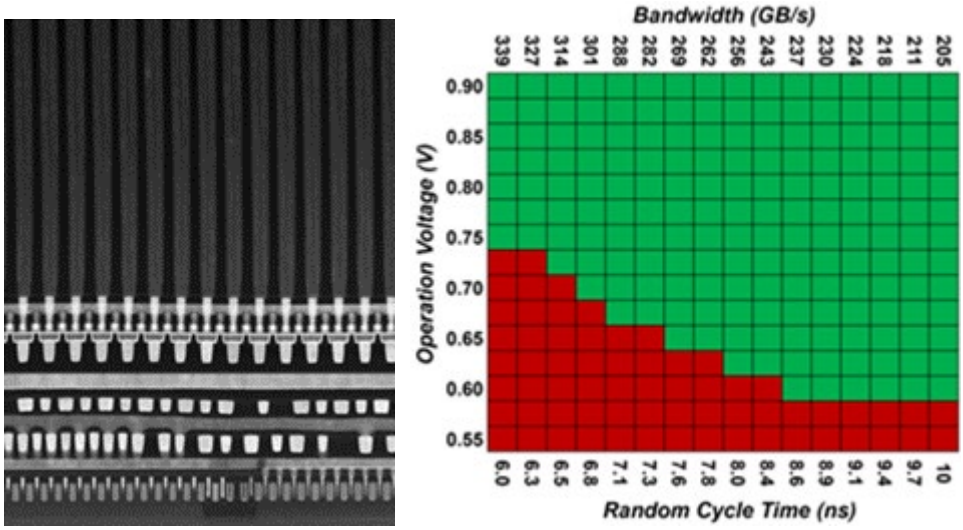


Figures: (left) TEM cross-sections of the Access Device. (right) Endurance characteristics of a 5nm ferroelectric stack operating at 1.4V, 95℃

Memory Technology

"Integration of 0.75V V_{DD} Oxide-Semiconductor 1T1C Memory with Advanced Logic for An Ultra-Low-Power Low-Latency Cache Solution" – Taiwan Semiconductor Manufacturing Company (TSMC) (Paper T2-1)

TSMC successfully demonstrated the monolithic integration of a BEOL memory with advanced logic. The memory array is completely embedded in the BEOL, featuring an oxide-semiconductor channel selector and a low-temperature process capacitor. This advanced logic-compatible BEOL memory technology offers a customizable, ultra-low-power, low-latency cache solution with a higher density than SRAM.

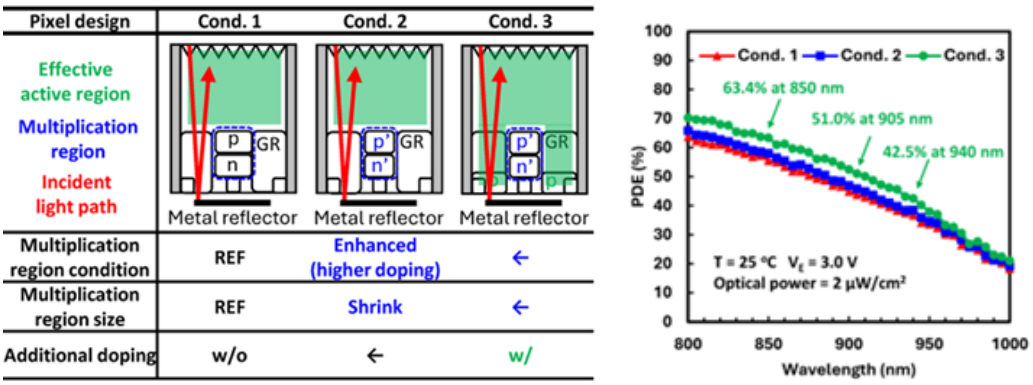


Figures : (Left)Cell array region cross-sectional TEM (Right) Shmoo at 85℃ and 128ms retention.

Image Sensor Technology

""A Back-illuminated 10 um-pitch SPAD Depth Sensor with 42.5% PDE at 940 nm using Optimized Doping Design" – Sony Semiconductor Solutions (Paper T1-2)

The research was conducted using a 10 µm-pitch single-photon avalanche diode (SPAD) depth sensor with a back-illuminated (BI) structure on a 300 mm CMOS platform. To enhance photon detection efficiency (PDE), the multiplication region design was optimized to increase the triggering probability for the Geiger mode, and an optimized doping design was introduced to enable more efficient charge collection. As the results, the world's highest PDE of 42.5% at 940 nm was achieved.

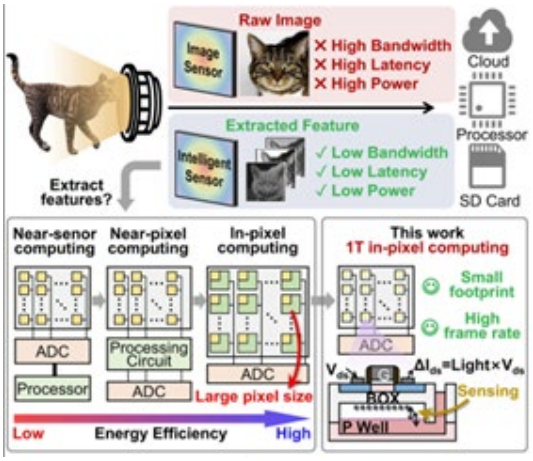


Figures: (Left) Pixel design comparison, (Right) Experimental result of PDE

Image Sensor Technology

"First Demonstration of 1T FDSOI-based > 1000fps Image Sensor with In-pixel Computing" – Peking University (Paper T6-4)

Peking University demonstrates a 128x128 image sensor based on 1T 22nm FDSOI pixel, which leverages the deep depletion region under buried oxide for optical sensing. Key features include: (1) extremely high photosensitivity of $5x10^5$ A/W, due to the amplifying effect of the FET; (2) photosensitivity can be tuned by gate/drain voltage, enabling in-pixel computing capability in 1T structure; (3) the chip can achieve over 1000 fps imaging and feature extraction utilizing the in-pixel processing capability and the proposed exposure/sampling/readout uncoupled pipeline design.



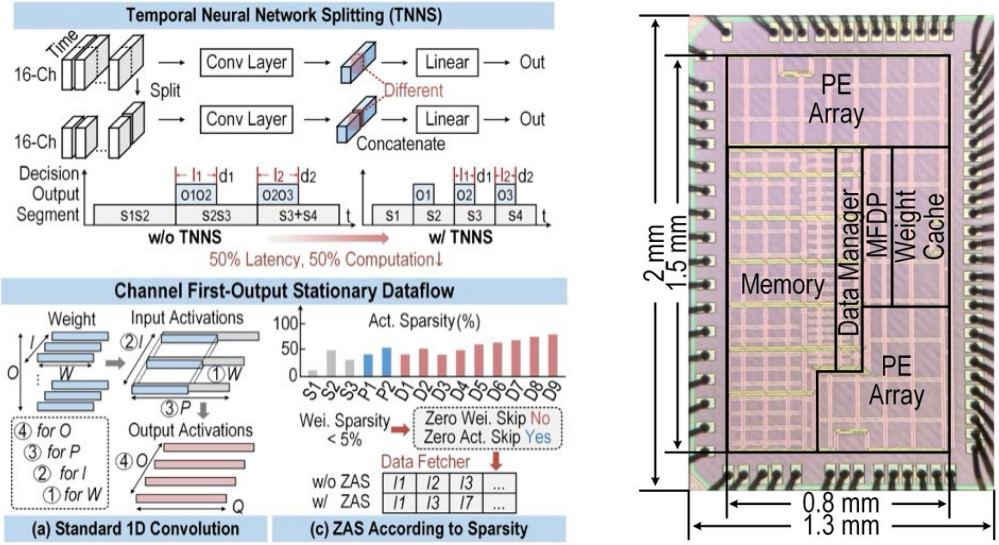
Figures: Various architectures of intelligent sensors and this work proposed to address issues occurred during transmission of sensor data.

Circuit Highlights

Biomedical devices, circuits, and systems

“PANDA: A 3.178 TOPS/W Reconfigurable Seizure Prediction ANd Detection Neural Network Accelerator for Epilepsy Monitoring" (Paper C21-1)

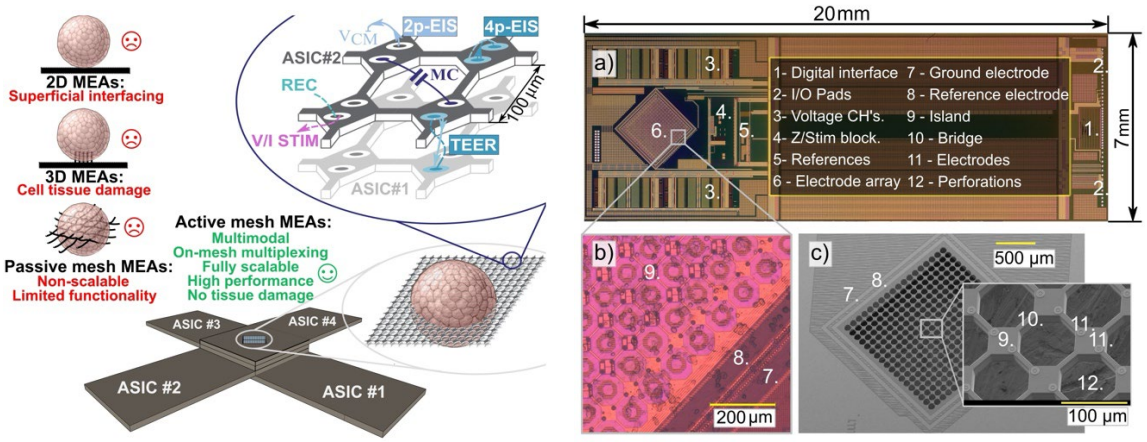
A group from Peking University, Southern Medical University and Southern University of Science and Technology will present a reconfigurable neural network accelerator for seizure detection and prediction called PANDA. The authors improved the efficiency of detection/prediction operations by temporal partitioning of the neural network and improvement of data flow using statistical information. They achieved a sensitivity of 99% and a false positive rate of 0.43 times/h with an efficiency of 3.178 TOPS/W for epileptic seizures.



Figures: (Left) Proposed architecture, (Right) Chip micrograph.

“An Active Silicon Perforated MEA for Seamless 3D Organoid Interfacing with Low-Noise, Scalable Multimodal Electrophysiology“ (Paper C24-1)

Imec reports an active silicon perforated MEA (Micro-Electrode Array) for 3D organoid interfacing, integrating CMOS electronics for low-noise, high-resolution recording, stimulation, and Electrochemical Impedance spectroscopy (EIS). The MEA features a scalable 256-island mesh with multiplexed operation, achieving low input-referred noise (9.1±1.5 μV_{rms}、300Hz~10kHz) and low power (11.3 µW per island). In vitro tests with cardiomyocytes demonstrate accurate recordings, network propagation mapping, and intracellular recordings via voltage stimulation. This perforated MEA offers unparalleled functionality and scalability for advancing organ-on-chip research.

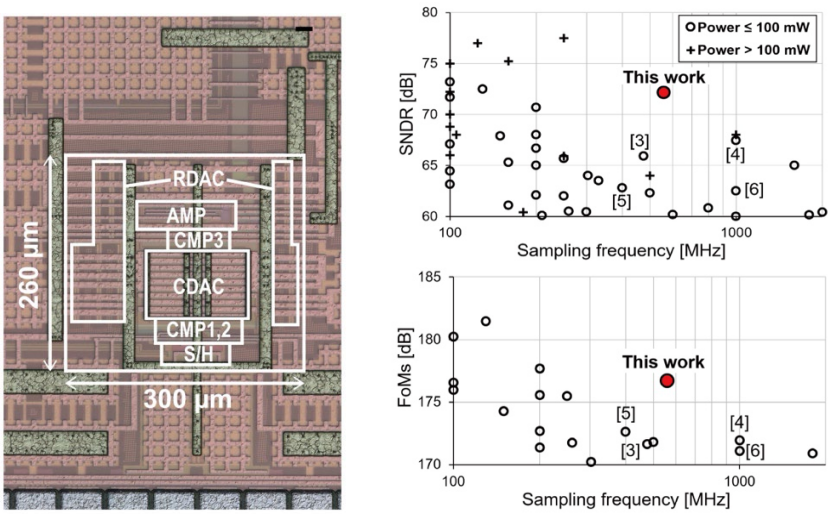


Figures: (Left) Concept of a 3D CMOS MEA system with 4 stacked perforated MEAs, (Right) a) Die photo b) Cardiomyocyte culture on the electrode array c) SEM image of the fully-fabricated suspended mesh with its perforations, islands and electrodes.

Data converters

“An 11.9-ENOB 560-MS/s Subranging ADC Employing Amplifier-Switching Architecture with Multi-Threshold Comparators (Paper C8-1)

The University of Tokyo proposes a 14-bit 560-MS/s ADC, which employs an amplifier-switching subranging architecture. A multi-threshold comparator with time-latch stages is also proposed to achieve 16-level decisions with a single input pair. Fabricated in 28nm CMOS, this work achieves 72.14 dB SNDR at Nyquist input and consumes 9.76 mW at 560 MS/s, which leads to 176.7 dB Schreier FoM.



Figures: A chip photo of the 28nm CMOS prototype and the performance comparison with state-of-the-art Nyquist-rate ADCs with Fs > 100 MHz.

Devices and Accelerators for ML/DL and New Compute

"NuVPU: A 4.8~9.6 mJ/frame Progressive NTT-based Unified Video Processor for Stable Video Streaming and Processing with Neural Video Codec (Paper C10-2)

KAIST researchers introduce NuVPU, the first unified neural video processor that accelerates both streaming and post-processing of Neural Video Codec (NVC) with up to 36.9 TOPS/W, outperforming prior designs by up to 9.2×. Leveraging a Selective Convolution-mode Neural Engine (SCNE) and Progressive NTT Unit (PNTU), NuVPU adaptively switches computation domains and reduces logic and memory overheads by up to 80%, enhancing throughput by 3.35×. A novel memory architecture with frequency-aware compression and adaptive scheduling slashes external memory access by 81.3%, enabling stable 4K video delivery under variable network conditions.

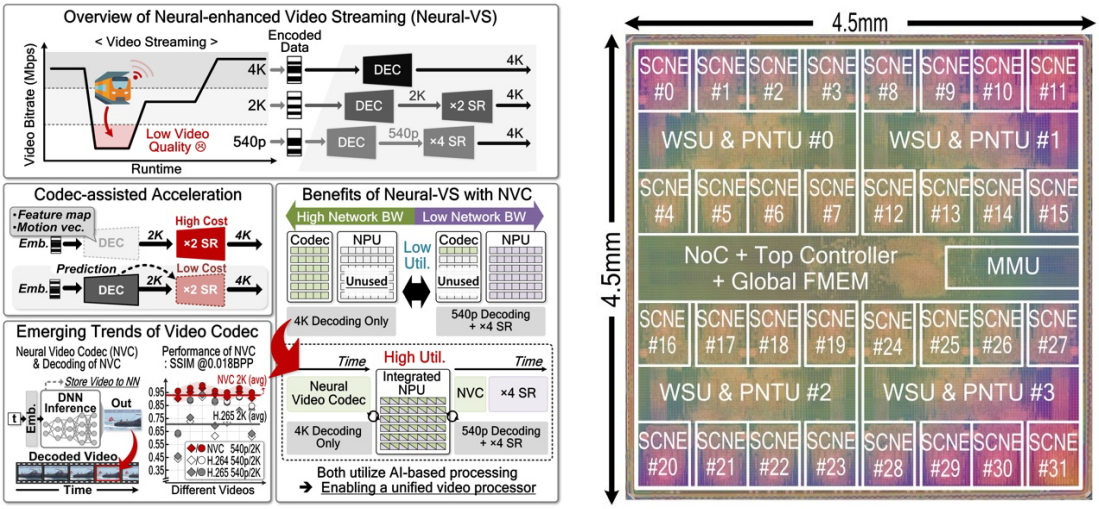
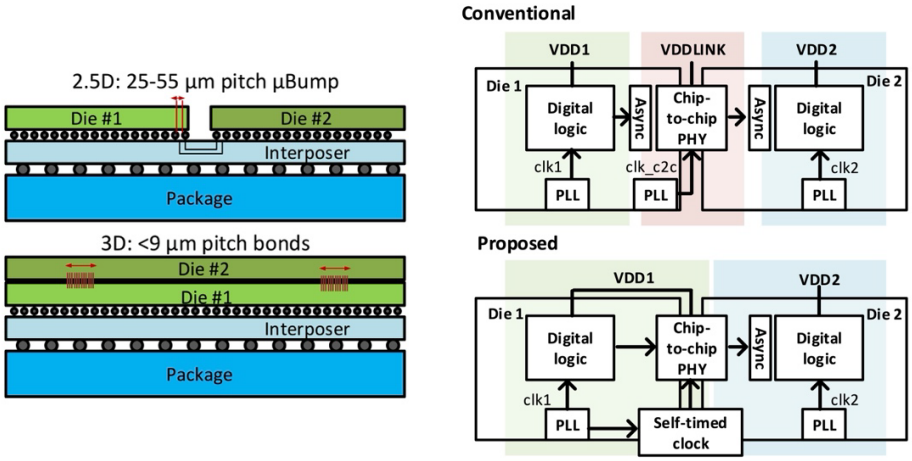


Figure: NuVPU chip supporting seamless 4K neural video streaming and post-processing with NTT-based acceleration.

Digital Circuits, Hardware Security, Signal Integrity, Ios

"A 77 fJ/bit 8 Gbps Low-Latency Self-Timed Die-to-Die Link for 2.5D and 3D Interconnect in 3nm (Paper C7-3)

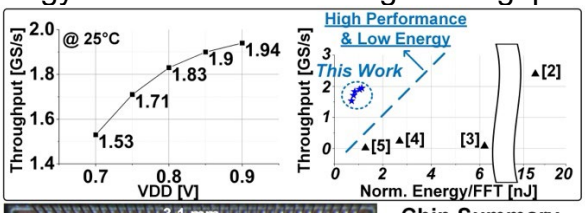
NVIDIA researchers present a self-timed die-to-die serial link for 2.5D and 3D stacked die interconnects using a standard adaptive digital clock and voltage supply. The link achieved 8Gbps/pin bandwidth with a 1 cycle latency, energy efficiency of 77fJ/b, and 44 Tbps/mm^2 at 07V in a 3nm process.

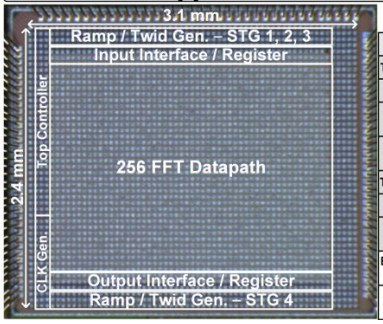


Figures: (Left) Cross section of 2.5D and 3D packages,
(Right) comparison between conventional and proposed architectures.

"A 0.71nJ, 1.53GS/s Throughput 256-FFT using Floating Point Analog Computation (Paper C23-1)

University of Michigan proposes a 256-point FFT engine using the analog floating point implementation. The proposed method encodes the mantissa value with both voltage and pulse width and a digital 4-bit exponent. Implemented in 22nm CMOS, the chip demonstrates a low energy of 0.71nJ/FFT at a high throughput of 1.53 GS/s.





Chip Summary

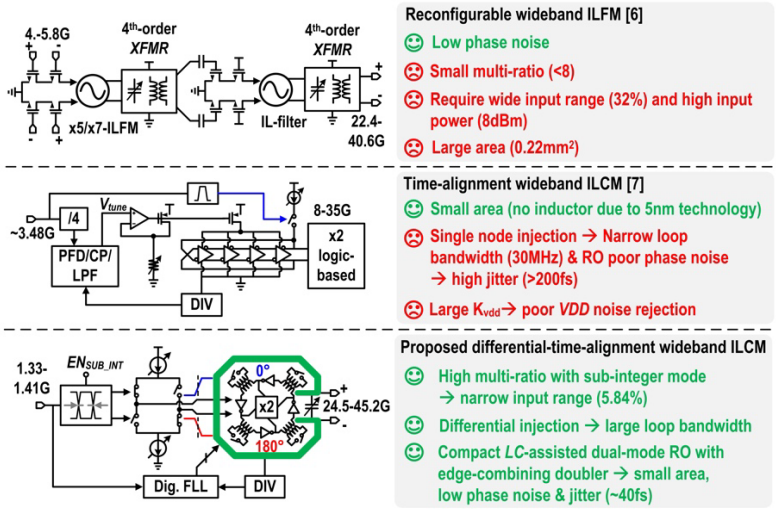
	Specifications		
Technology	TSMC 22 nm		
Die Area	3.1 mm × 2.4 mm		
Supply Voltage	0.7 - 0.9V		
Max. Frequency	2.4 GHz		
Throughput	1.53 - 1.94 GS/s		
System Performance			
Op. Cond. (25°C)	0.7V 1.9 GHz	0.8V 2.2 GHz	0.9 V 2.4 GHz
Energy/FFT [nJ]	0.71	0.84	1.13
Latency [ns]	211	182	167

Figures: Relation between throughput and Vdd, comparison of FoM with other works, and chip micrograph

Frequency Generation and Clocking Circuits

"A 24.5-to-45.2-GHz Dual-Injection Clock Multiplier with Folded-Inductor-Based Magnetic-Flux Cancellation Achieving 32.83-fsrms Jitter and 0.037-mm2 Core Area (Paper C19-1)

University College Dublin presents an injection-locked clock multiplier (ILCM) with a wide frequency tuning range and low jitter. An LC-series dual-mode quadrature ring oscillator is co-designed with a frequency doubler to simultaneously extend the frequency tuning range and lower the phase noise in mm-wave bands. A differential time-alignment technique is utilized to achieve a large loop bandwidth. The proposed circuit, fabricated in 28nm CMOS and occupying a core area of 0.037 mm^2, achieves an output frequency range of 24.5 to 45.23 GHz and a measured RMS jitter of 32.83 fs at 39.5 GHz.



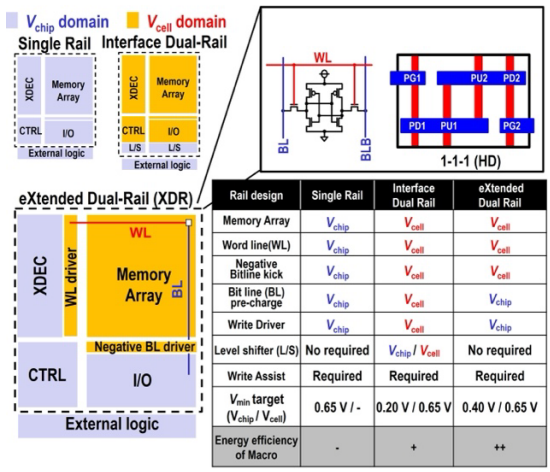
Figures: Conceptual diagrams of prior wideband injection-locked frequency multipliers (ILFMs) with large high-order transformer, single-node injection ring oscillator (RO), and the proposed folded-LC-assisted dual-injection time-alignment clock multiplier.

Memory Technologies, Devices, Circuits, and Architectures

"A 3nm FinFET 563kbit 35.5Mbit/mm2 Dual-Rail SRAM with 3.89pJ/access High Energy Efficient and 27.5uW/Mbit 1-cycle Latency Low-Leakage Mode (Paper C4-1)

Authors at TSMC demonstrate a high-density (HD) 6T SRAM for mobile applications using the eXtended Dual Rail XDR architecture and two key techniques. The Delaying-Write-WL (DeWL) technique resolves the problem of contention between the cell and the write-driver (WDRV), and the 1-cycle latency low-leakage mode (1-CLM) reduces

power by turning off BL pre-chargers during no operation (NOP) periods. A 3-nm FinFET test chip achieves a 17% reduction in active energy and a 10% decrease in standby leakage.



Rail design	Single Rail	Interface Dual Rail	eXtended Dual Rail
Memory Array	V_{chip}	V_{cell}	V_{cell}
Word line(WL)	V_{chip}	V_{cell}	V_{cell}
Negative Bitline kick	V_{chip}	V_{cell}	V_{cell}
Bit line (BL) pre-charge	V_{chip}	V_{cell}	V_{chip}
Write Driver	V_{chip}	V_{cell}	V_{chip}
Level shifter (L/S)	No required	V_{chip} / V_{cell}	No required
Write Assist	Required	Required	Required
V_{min} target (V_{chip} / V_{cell})	0.65 V / -	0.20 V / 0.65 V	0.40 V / 0.65 V
Energy efficiency of Macro	-	+	++

	Conventional IDR design	Proposed XDR design
Technology	3nm FinFET	
Bitcell	High density 6T (1-1-1)	
Macro configuration	0.563 Mbit	
Highest metal	M6	
Total capasity	1.689 Mbit (0.563 Mbit × 3)	5.067 Mbit (0.563 Mbit × 9)
Macro area	0.0159 mm²	0.0159 mm²
Density	35.5 Mbit/mm²	35.5 Mbit/mm²
Standby leakage @V_{chip} = 0.40 V V_{cell}=0.650 V, 25 °C	37.1 μW/Mbit	28.5 μW/Mbit @Normal mode 27.5 μW/Mbit @Low leak mode
Read active energy @V_{chip} = 0.40 V V_{cell}=0.650 V, 85 °C	3.85 pJ/access	2.11 pJ/access
Write active energy @V_{chip} = 0.40 V V_{cell}=0.650 V, 85 °C	8.27 pJ/access	5.70 pJ/access
Typical energy efficiency @V_{chip} = 0.40V V_{cell}=0.650 V, 85 °C	6.06 pJ/access	3.89 pJ/access
F_{max} @V_{chip} = 0.65 V	1.76 GHz	1.22 GHz

Figures: Comparison of three types of architecture for SRAM macro and features.

Power Management Devices and Circuits

A 0.087 fs FOM Current-mirror-based Analog-assisted Digital LDO with VO Ripple Optimization (Paper C18-1)

Sogang University presents a current-mirror-based analog-assisted (CBAA) digital low-dropout regulator (DLDO) that achieves a fast transient response and output voltage (V_O) ripple optimization. It features less than 1 mV V_O ripple at 200 mA load current. Fabricated using a 28 nm CMOS process, the CBAA DLDO shows a superior figure-of-merit (FOM) of 0.087 fs among low-input voltage DLDOs.

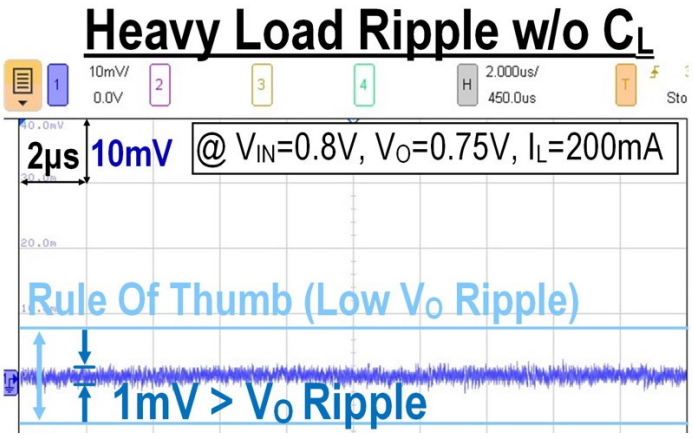
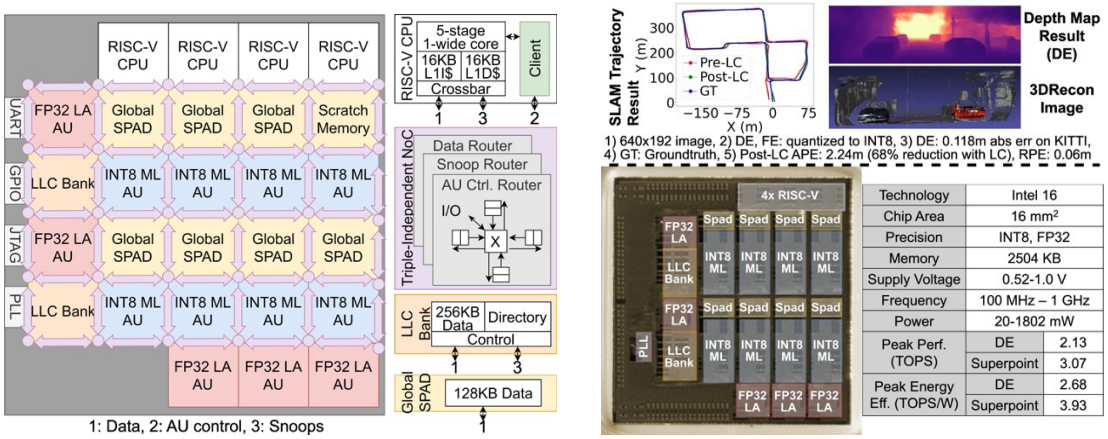


Figure: Measured LDO output voltage waveform with less than 1 mV V_O ripple at 200 mA load current.

Processors and SoCs

MAVERIC: A 16nm 72 FPS, 10 mJ/frame Heterogeneous Robotics SoC with 4 Cores and 13 INT8/FP32 Accelerators (Paper C10-5)

Researchers at the University of California, Berkeley, report the heterogeneous SoC (MAVERIC) with 4 cores and 13 INT8/FP32 accelerator units for ML and robotics applications. 3D reconstruction robotics application combines depth estimation (DE) and simultaneous localization and mapping (SLAM) for perception tasks, posing compute demand, accelerator integration, and scheduling challenges. MAVERIC operates at up to 1 GHz and achieves 8 TOPS/W peak energy efficiency. It supports loop closure and delivers 10 mJ/frame and 72 FPS at the end-to-end DE and SLAM.



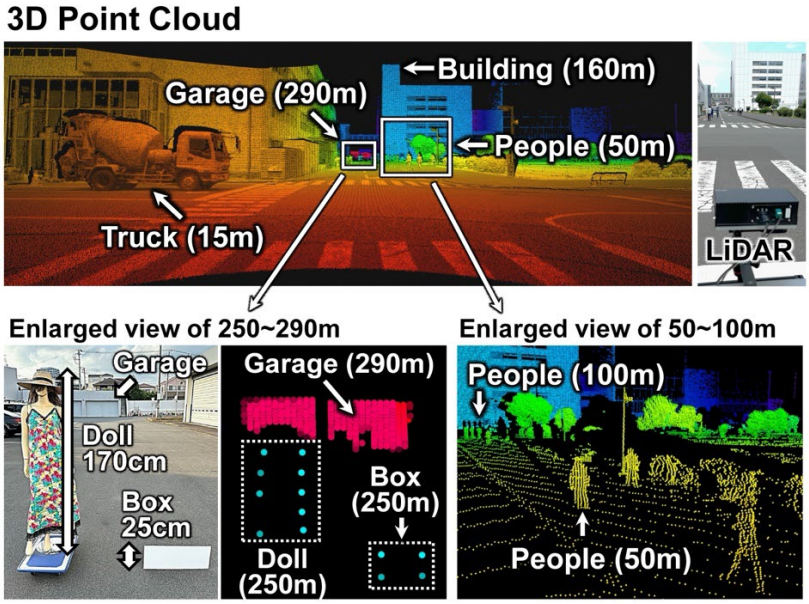
Technology	Intel 16	
Chip Area	16 mm²	
Precision	INT8, FP32	
Memory	2504 KB	
Supply Voltage	0.52-1.0 V	
Frequency	100 MHz – 1 GHz	
Power	20-1802 mW	
Peak Perf. (TOPS)	DE	2.13
	Superpoint	3.07
Peak Energy Eff. (TOPS/W)	DE	2.68
	Superpoint	3.93

Figures: (a) Architecture overview of MAVERIC, showing the 8 INT8 ML accelerators, the 5 FP32 linear algebra accelerators, the 4 RISC-V CPUs and 3-layer NoC for binding the sub-blocks.
(b) Chip micrograph and performance overview with SLAM demonstration.

Sensors, Imagers, IoT, MEMS, Display Circuits

A 25M points/s Back-Illuminated Stacked SPAD Direct Time-of-Flight Depth Sensor with Equivalent Time Sampling for Automotive LiDAR (Paper C27-2)

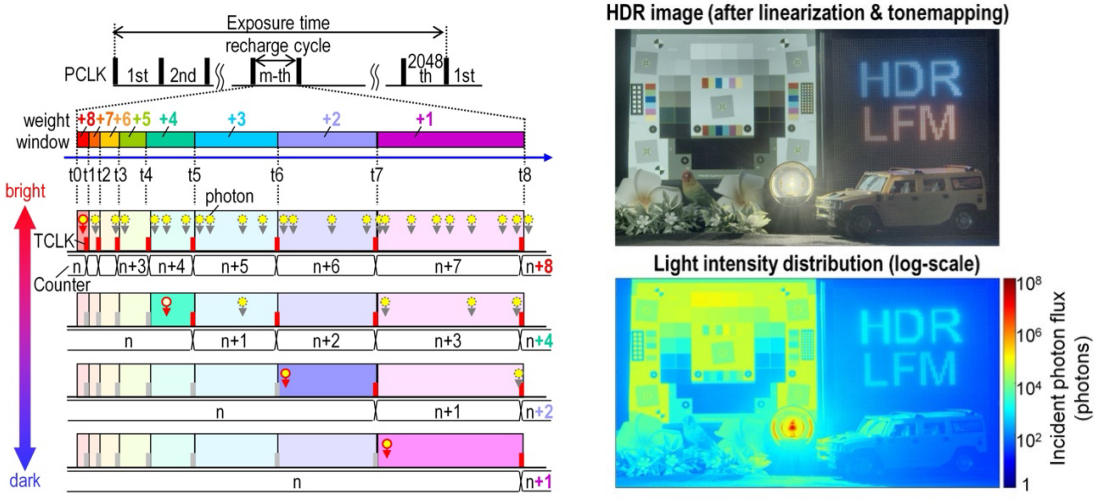
Sony Semiconductor Solutions achieved a range measurement at 25M points/s by pipelining histogram processing and data output and reducing the amount of output data through extraction of distance information within the chip. This achieves distance measurement with the FoV of 120°/26°, the angular resolution of 0.05° and the frame rate of 20 fps required for LiDAR performance which is used autonomous driving over level 3. In addition, the measurement accuracy has been improved without increasing the amount of data by applying an equivalent time sampling method using multi-phase clocks. This sensor detects objects with a height of 25 cm at a distance of 250 m and the maximum distance accuracy is 17 cm at distances up to 300 m.



Figures: Captured images and measurement data with the present sensor system.

"2/3-inch 2.1Megapixel SPAD Image Sensor with 156dB Single-Shot Dynamic Range and LED Flicker Mitigation based on Weighted Photon Counting Technique (Paper C27-1)

Canon presents a SPAD image sensor for automotive applications. The novel weighted photon counting technique achieves 156 dB dynamic range with LED flicker mitigation and seamless global shutter operation. Additionally, image capture is ensured for targets under 0.1 lux through read noise-free operation.

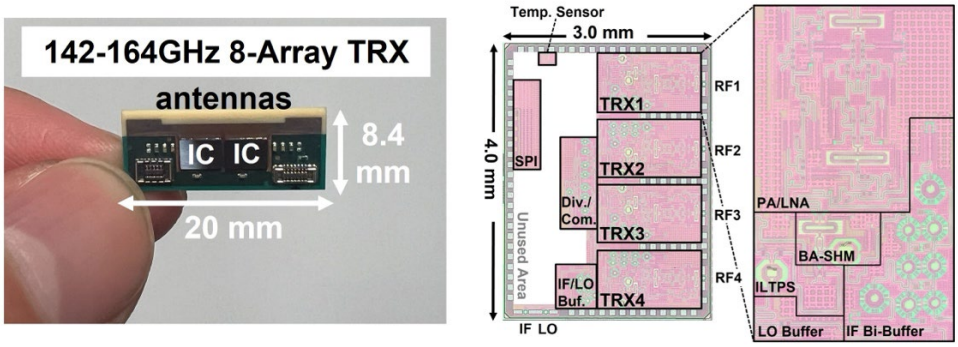


Figures: (Left) Weighted photon counting (WPC) operation principle.
(Right) HDR image and its light intensity distribution.

Wireless and RF Devices Circuits and Systems

A 150 GHz High-Power-Density Phased-Array Transceiver in 65nm CMOS for 6G UE Module (Paper C28-1)

A collaboration led by the Institute of Science Tokyo presents an ultra-compact wireless module IC for mobile devices, designed for use in the 150 GHz (D-band) frequency range expected to be utilized in sixth-generation mobile communication systems (6G). The Antenna-in-Package (AiP) integrates two phased-array transceiver ICs fabricated using 65nm CMOS technology. The power consumption per antenna path is 150 mW during transmission and 93 mW during reception, achieving a data transmission rate of 56 Gb/s.



Figures: (Left)8-element antenna-in-package (AiP) module consisted of proposed 4-element D-band transceiver chips, (Right) chip micrograph.

Wireline and Optical Transceivers, Optical Interconnects and Processors

“A 128Gb/s 0.67pJ/b PAM-4 Transmitter in 18A with RibbonFET and PowerVia (Paper C12-2)

Researchers at Intel present a fully integrated 128-Gb/s DAC-based transmitter (TX) designed for long-reach wireline applications in 18A CMOS process with RibbonFET, PowerVia and a backside power delivery network. The backside power layer is also used for inductors and clock distributions. The TX achieves the best energy efficiency of 0.67 pJ/bit (0.75 pJ/bit with the PLL) and the smallest area reported while meeting key electrical compliance specifications for PAM-4 standards.

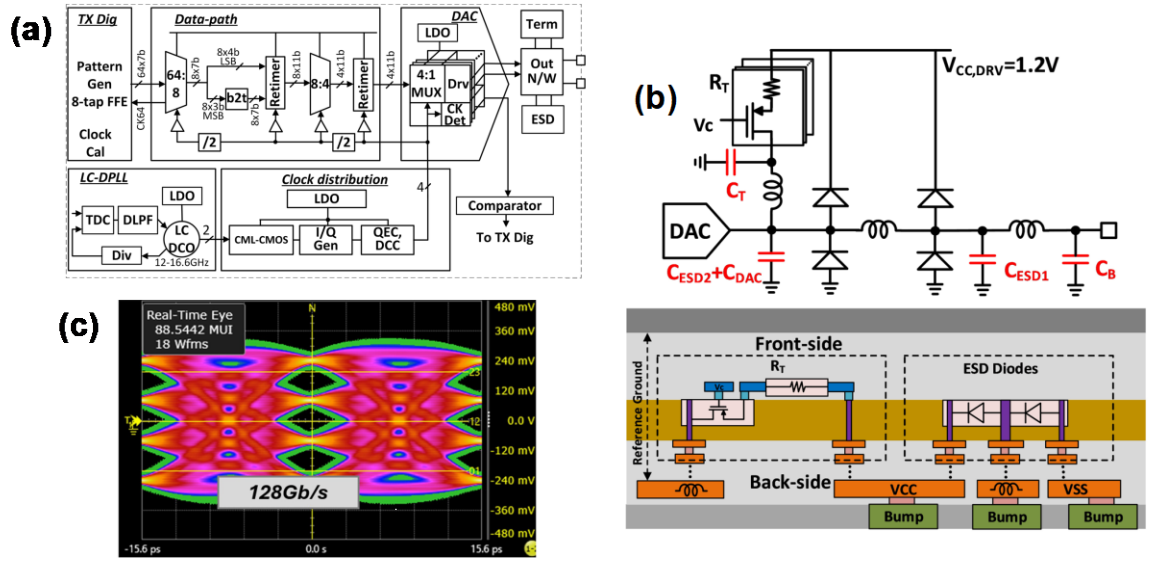


Figure: (a) Block diagram of the DAC-based PAM-4 TX. (b) Output network design utilizing back-side low-resistance metals. (c) Measured TX eye diagrams.