2025 Symposium on VLSI Technology and Circuits (Sunday, June 8)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Le Bois	La Cigogne	Le Cygne	Time
8:00-20:00	Registration									8:00-20:00
8:30-13:00	8:30-18:30 2025 Silicon Nanoelectronics Workshop (Day 1)									8:30-13:00
13:00-15:00			Special Workshop *13:00-19:00	Workshop 1		Workshop 2		[Satellite Room] Workshop 2		13:00-15:00
15:30-18:00				Workshop 3		Workshop 4	Workshop 5	Workshop 6	Workshop 7 *15:30-18:30	15:30-18:00
19:00-21:30				Workshop 8		Workshop 9	Workshop 10 *18:30-21:30	Workshop 11	Workshop 12	19:00-21:30

Special Workshop: Centennial Anniversary of FET Invention: Past, Present, and Future (FET 100) [Suzaku I]

1 Opening Remark, K. Endo, Tohoku Univ.

2 Remark on FET100, B. Zhao, President, IEEE EDS

3 Overview - FET History, Present and Future, H. Iwai, NYCU/Institute of Science Tokyo

4 Structural Evolution and Functional Integration of FETs Traced in a Public Semiconductor Roadmap and the Future Prospectives, Y. Hayashi, AIST

5 The Evolution of HPC and AI and Their Demands on FET Technologies, M. Kondo, Keio Univ.

6 GAA: Genuine Architecture for AI Generation, Y. Masuoka, Samsung

7 Emerging FETs in Future Chiplet LSIs, H. Wakabayashi, Institute of Science Tokyo

8 Evolution of Technology to 3D-Memory in DRAM, Flash, and Emerging Memories, J. Lee, Samsung

9 Progress and Future Challenges of Si and Wide Bandgap Semiconductor Power FETs, T. Kimoto, Kyoto Univ.

10 Closing Remark, T. Kimoto, President, JSAP

Workshop 1: Innovating Semiconductor Manufacturing: Science Meets AI [Shunju II+III]

1 Opening (Science Meets AI), J. Jeong, Samsung Electronics

2 Building Scientific Foundation Models: Challenges, Methodologies, and Semiconductor Manufacturing Applications, N. Park, KAIST

3 Applications of Science-driven AI in the Semiconductor EDA, I. Markov, Synopsys

4 Light Out! Virtualizing the Semiconductor Ecosystem, J. Ervin, Lam Research

5 From Challenge to Control: Bridging Semiconductor Process Complexity with Science-Based AI, C. Jeong, UNIST

6 An Exploration of the Necessity for Science-driven AI Integration, K. Azzizzadenesheli, Nvidia

Workshop 2: Advanced Heterogeneous System with 3D Chiplet Integration [Shunju I]

1 Hybrid Bonding Interconnect Pitch Scaling: Wafer-to-Wafer and Die-to-Wafer Cu/SiCN Hybrid Bonding, E. Beyne, Imec

2 The Role of EDA as Chips Transform Into 3D Systems, K. Roze, Cadence Design Systems

3 HBM (High Bandwidth Memory) and Advanced Packaging Technologies for AI Era, K. Lee, SK hynix

4 Chiplet and Heterogeneous Integration Technologies for HPC and AI, K. Sakuma, IBM

5 Integrating AI and GPU Accelerated Simulation to Build Real-time Digital Twins for Semiconductor Manufacturing Processes, J. Linford, NVIDIA

Workshop 3: Semiconductor Manufacturing with AI [Shunju II+III]

1 Revolutionizing Chip Manufacturing through AI, G. Thareja, Applied Materials

2 Recursive AI in Material Engineering, Y.-J. Kang, Synopsys

3 Leveraging AI for Enhanced Efficiency and Quality in Semiconductor Manufacturing, S. Shuto, Toshiba

4 Deep Topological Data Analysis and Self-Supervised Learning for Yield and Quality Optimization, J. Giri, Intel

5 Enabling a New Paradigm In Semiconductor Design-Manufacturing Co-optimization through Simulation Technologies, V. Spandan, Sony

Workshop 4: Innovations and Challenges in the Advanced Packaging Era [Shunju I]

1 3D Heterogeneous Integration and EDA, A. V.-Varnai, Siemens

2 Co-Packaged Optics: Enabling Scalable and Efficient Interconnects for the Future of Accelerated Computing, L. Gantz, NVIDIA

3 Perspectives on Benefits and Implementation of 3DI in Advanced Memory, M. Tagami, Kioxia

4 Advancing AI Performance: Innovations in 3D Chiplet Platforms and Integration, K. Larsen, Synopsys

5 Progress in Semiconductor Equipment Development to Drive 3DI Expansion, A. Raley, Tokyo Electron Ltd

6 Ultra-Dense 3D Heterogeneous Integration: Architectures, System-Level Benefits, and Manufacturing Readiness, S. Choi, Standford / SiClarity

Workshop 5: Architectural Benchmarking of Compute-in-Memory Systems [Le Bois]

1 CIM-based Processing of DNNs, X. Sun, TSMC

2 GainSight: Fine-Grained Memory Access Profiling for GCRAM-Based AI Accelerators, T. Tambe, Stanford Univ.

3 Tile Efficiency is not System Efficiency - CIM Architecture Studies of LLMs and Other Large DNNs Accelerators, P. Narayanan, IBM Research Almaden

4 HISIM: Efficient Design Space Exploration of 2.5D/3D Heterogeneous Integration for AI Computing, Y. Cao, Univ. of Minnesota

5 Recent Development of NeuroSim Benchmark Framework towards Angstrom Nodes and Heterogeneous 3D Integrated System, S. Yu, Georgia Institute of Technology

Workshop 6: Recent Advances in CMOS Cellular and Molecular Biosensors [La Cigogne]

1 Multi-Modal CMOS Biosensing and Actuation: Advancing Cellular and Molecular Diagnostics, H. Wang, ETH Zurich

2 Continuous Monitoring of Small Molecules Using Electrochemical Aptamer-Based Biosensors with CMOS Electronic, J.-C. Chien, Univ. of California

3 Neuronal Synaptic Connectivity Mapping by CMOS Microchip, D. Ham, Harvard Univ.

4 A Scalable CMOS Molecular Electronics Chip for Single-Molecule Biosensing, D. Hall, UC San Diego

5 Cyber-Secure Biological Systems, R. T. Yazicigil, Boston Univ.

6 Panel Discussion

Workshop 7: What is Possible with Open Chip Design? The Journey so Far. [Le Cygne]

1 Toward a World where Everyone can Design and Fabricate LSI, J. Akita, Kanazawa Univ.

2 Open PDK Initiative & Free Open Source MPW Access in IHP Technology, F. Vater, IHP

3 End-to-end Open-source IC Design, F. K. Gürkaynak, ETH Zürich

4 Open-Source Analog Circuit Design Course With IC Emphasis, H. Pretl, Johannes Kepler Univ.

5 Toward End-to-End Open Platforms and Chips for Embodied AI, C. Reita, Fondazione Chips-IT

6 Veryl: A New Hardware Description Language Developed as Open-Source Software, N. Hatta, PEZY Computing, K.K.

7 Using Open-Source EDA for Machine Learning, T. Spyrou, Precision Innovations Inc

8 Open Source Co-Design of LLMs for the Edge – From Cloud to Handheld – for Ushering in an Era of Localized Intelligence, G. Kielian, Google Research

9 Let's Create an Open-Source MOSbius, P. Kinget, Columbia Univ.

Workshop 8: Manufacturing Advanced VLSI Systems Using Virtualization and Machine Learning [Shunju II+III]

1 Manufacturing with Virtual Silicon: The Role of Process Modeling and Machine Learning in High-Volume Semiconductor Manufacturing, J. Ervin, Lam Research

2 Leveraging Virtual Twins and ML/AI During Manufacturing of Advanced VLSI Systems, Y. Hanada, Dassault Systèmes

3 Federated Digital Twins and Hybrid AI Applied Across Processes in a Fab Ecosystem, W. Verachtert, Imec

4 Leveraging Fast Process Modeling for Assessing GAA Standard Cells, E. Panning, SiClarity

5 Improving Wafer Yield with Process Virtualization, Feature Engineering and Targeted Sampling, A. Torres, Siemens

Workshop 9: Hybrid Bonding-Breaking Boundaries in Advanced Packaging and Heterogeneous Integration in the Era of Chiplets and AI [Shunju I]

1 Hybrid Bonding Outlook for Chip-to-Wafer Memory Stacking, C. Wang, Micron Inc.

2 Metrology and Inspection Challenges in Hybrid Bonding for Advanced Packaging and Heterogeneous Integration, S. Lee, Samsung Electronics Co.

3 Unlocking the Next Generation of Hybrid Bonding, J. Abdilla, Besi

4 Wafer Bonding Challenges and the Resolution of Paths, I. Son, TEL

5 Development of Polymer Hybrid Bonding toward to 3D Packaging Integration, T. (Ken) Fujiwara, Toray Industries Inc.

6 Unique Challenges of D2W Hybrid Bonding for Logic and Memory Applications, J. Yeo, Applied Materials Inc.

7 Inspection, Metrology, and Process Challenges in Die-to-wafer Hybrid Bonding, C. Lenox, KLA

8 Enabling In-Line Process Control for Hybrid Bonding Applications in HPC and AI, M. Pau, Onto Innovation

9 High-Throughput In-line AFM Metrology for Hybrid Bonding Applications, H. Chin, NearField Instruments

10 Innovative Metrology Solutions for HB Process Challenges in Advanced Packaging, A. Lee, Nova

Workshop 10: Advancing Neuromorphic Technology Research and Commercialization: From Sensors to Edge to Cloud [Le Bois]

1 Novel Neuromorphic Visual Perception Modalities to Enable Physical AI, X. Iturbe, IKERLAN Technology Centre

2 MISEL: A Multiband Event-Based Intelligent Vision System, J. Flak, VTT Technical Research Centre of Finland Ltd.

3 Nanophotonic Neuromorphic Computing and Sensing: Broadcasting Networks of Nanoscale Neural Nodes that Receive, Transmit, and Analyze Light Signals, A. Mikkelsen, Lund Univ.

4 Low-power and Secure Photonic Accelerators Based on Augmented Silicon Photonics Platforms, F. Pavanello, CROMA, CNRS

5 Integrated Photonics for Hardware Accelerators and Neuromorphic Computing, M. Hejda, Hewlett-Packard Labs (HPE)

6 Heterogeneous Neural Processing Units Leveraging Analog In-Memory Computing for Edge AI, I. Boybat, IBM Research Europe-Zurich

7 Innatera's Spiking Neural Processor (SNP): Mixed-signal MCU for Power Constrained Tiny ML Applications, P. Bogdan, Innatera Nanosystems B.V.

8 A 3D Integration Technologies for Neuromorphic Systems, G. Van der Plas, Imec

9 Expanding Edge AI for Wearable Augmented Reality (AR) with 3D Silicon Integration, O. Moreira, Snap Inc.

10 Scaling Up Neuromorphic Computing to Cloud-Level, F. Negri, SpiNNcloud Systems GmbH

Workshop 11: Revolutionizing Electronics with GaN: Opportunities and Challenges [La Cigogne]

1 RF GaN-on-Si Electronics: Advancing Technology Frontiers and Bringing from Lab to Fab, G. I. Ng, Nanyang Technological Univ.

2 GaN Power Devices: Plenty of Room at the Bottom and the Top, Y. Zhang and H. Wang, Univ. of Hong Kong

3 High Temperature Electronics: An Exciting New Application for Gallium Nitride HEMTs, J. Niroula, Massachusetts Institute of Technology

4 Vertical GaN Power Devices: Design, Characterization and Perspectives, J.-H. Hsia (Sharon) , Massachusetts Institute of Technology

5 Monolithic Integration in Power GaN: Prospects and Challenges - An Examination of Lateral GaN Technology After a Decade of Development, A. Syed, GlobalFoundries

6 Developing High-Performance GaN Complementary Circuit Technology, N. Chowdhury, Bangladesh Univ. of Engineering and Technology (BUET)

7 GaN Technologies: A Foundry Perspective, S. Bentley, GlobalFoundries

8 GaN on Si for RF Applications - An Industry Perspective, Y. Ngu and A. Raman, GlobalFoundries

Workshop 12: Chip Tapeout Classes: Methodologies, Technologies and Outcomes [Le Cygne]

1 Opening, B. Nikolic, Univ. of California, Berkeley

2 Creating Agile Chip Design Flows Using High-Level Synthesis and Mflowgen, P. Raina, Stanford Univ.

3 Chip Design Flows Using Commercial Tools in Cloud-Based Classroom Environments, M. Morrison, Univ. of Notre Dame

4 Three Chips in a Semester, B. Nikolic, V. Jain, Univ. of California, Berkeley

5 Anatomy of an Undergraduate SoC Tape Out Class, K. Kornegay, Morgan State Univ.

6 Balancing Creative Freedom and Success Rate via Standardization in a Tapeout Course Sequence, K. Mai, Carnegie Mellon Univ.

7 From Schematic to Silicon: ADC Tapeout in 10 Weeks, D.Hall, University of California, San Diego

8 Industry announcements and Q&A

2025 Symposium on VLSI Technology and Circuits (Monday, June 9)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Salon de Charme	Le Bois	La Cigogne	Time
7:30-18:00	Registration									7:30-18:00
8:25-12:05	8:30-18:30 2025 Silicon Nanoelectronics Workshop (Day 2)	**Short Course 2** **Circuits and Systems for AI and Computing** **8:25 Opening** **8:30 Hardware Accelerator Design for AI: Enabling Efficient Generative Models,** L. Chang, IBM **9:20 Architecture Trends for AI Hardware Platforms,** N. James, AMD **10:10 Break** **10:25 Modular Chiplet Approaches for Scalable and Efficient Machine Learning,** Z. Zhang, Univ. of Michigan **11:25 AI for EDA: Challenges and Opportunities,** I. Markov, Synopsys		**Short Course 1** **Key VLSI Technologies in the AI Era** **8:25 Opening** **8:30 CMOS Scaling Exploration: Technology Trends and System-Level Perspectives,** L. Yang, TSMC **9:20 2D Materials and Their Application Space - Recent Insights Gained -,** J. Appenzeller, Purdue Univ. **10:10 Break** **10:25 Heterogenous System Partitioning, the 2.5D and 3D Integration Landscape and Roadmap,** E. Beyne, imec **11:15 Etch and Materials Innovations for Advanced Logic and Memory Applications,** T. Lill, Lam Research			**8:25-17:00 [Satellite Room] Short Course 1**	**8:25-17:00 [Satellite Room] Short Course 1**	8:25-12:05
12:05-13:10							Lunch			12:05-13:10
12:55-17:30		**12:55 Connectivity Technologies to Accelerate AI,** T. C. Carusone, Univ. of Toronto Alphawave Semi **13:45 3D Optical Interconnect Design,** F. Lee, TSMC **14:35 Break** **14:50 HBM for AI Computing,** J. Lee, SK hynix **15:40 Semiconductor Storage for Further Evolution of Generative AI,** J. Deguchi, KIOXIA Corp. **16:30 Advancements in Power Architectures for AI Computing: The Role of Intermediate Bus Converters and Hybrid Power Systems,** K.-H. Chen, National Yang Ming Chiao Tung Univ.		**12:55 DRAM History and Challenges,** Y. Matsumoto, Micron **13:45 Current Landscape and Future Outlook of Emerging Memory Technologies,** S. G. Kim, SK hynix **14:35 Break** **14:50 DTCO/STCO for Multi-Objective Optimization from Device to System, H.-O.** Kim, Samsung **15:40 Heterogeneous Integration Technologies for 3D Integrated CMOS Image Sensors,** Y. Kagawa, Sony **16:30 Closing**					12:55-17:30
17:30-21:45	19:30-21:45 2025 Spintronics Workshop				**17:30-19:30 Demo Session & Reception** **18:00- Reception**					17:30-21:45

2025 Symposium on VLSI Technology and Circuits (Tuesday, June 10)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Salon de Charme	Le Bois	La Cigogne	Le Cygne	Time
7:00-17:00	Registration										7:00-17:00
8:00-10:00		[Satellite Room] Opening & Plenary 1		Opening and Plenary Session 1 8:00-8:40 *Opening Remarks* PL1-1 8:40-9:20 (Plenary) SK hynix: Driving Innovation in DRAM Technology-Towards a Sustainable Future PL1-2 9:20-10:00 (Plenary) NVIDIA: Innovate VLSI for AI Growth							8:00-10:00
10:30-12:35	**C2: RF/mm-wave Tx and Rx** C2-1 10:30-10:55 Institute of Science Tokyo: A Ka-Band 8-Stream Phased-Array Receiver with Time-Hopping Blocker Rejection for 6G Applications C2-2 10:55-11:20 imec: An IEEE802.15.4ab/a/z Compatible IR-UWB 2TRX with Dual-Antenna Full-Duplex 1x3 SIMO Radar Sensing and Aliasing Suppressing Semi-Synchronous TX C2-3 11:20-11:45 Institute of Science Tokyo: A Triple-Band Transceiver for Formation Flying Satellite Communication with Dual Circular Polarized Wireless Power and LO Transfer C2-4 11:45-12:10 Pusan National Univ.: A Digital Envelope Tracking RF Power Amplifier Achieving 400MHz Channel Bandwidth and 91.9% Efficiency for Upper-Mid Band Extreme Massive MIMO 6G Communications C2-5 12:10-12:35 National Univ. of Singapore: Sub-μW Battery- and Crystal-Free Tag featuring 802.11ba/b-Compliant Wake-up Receiver, Backscattered Transmitter and 3D Localization	**C1: CIM and Quantum-inspired Computing** C1-1 10:30-10:55 TSMC: A 3nm 125 TOPS/W-29 TFLOPS/W, 90 TOPS/mm^2-17 TFLOPS/mm^2 SRAM-Based INT8 and FP16 Digital-CIM Compiler with Multi-Weight Update/Cycle C1-2 10:55-11:20 The Hong Kong Univ. of Science and Technology: NeuC-CIM: A 1.3pJ/SOP Neuromorphic Charge-Domain Compute-In-Memory Macro For Spiking Neural Network C1-3 11:20-11:45 Tsinghua Univ.: LLM-CIM: A 28nm 126.7TOPS/W Input-LUT-Based Digital CIM Macro with Reconfigurable Matrix Multiplication and Nonlinear Operation Modes for LLMs C1-4 11:45-12:10 POSTECH: An 8K-Spin Ising Machine IC with Reconfigurable Many-Body Spin Interactions and Limitless Multichip Extension C1-5 12:10-12:35 Univ. of California, Santa Barbara: m-Zephyr: A Digital In-Memory Ising Chip with 240 Spins Featuring Enhanced Connectivity Based on a Modified 3D Zephyr Topology		**T1: Technology Highlights 1** T1-1 10:30-10:55 Intel: Intel 18A Platform Technology Featuring RibbonFET (GAA) and PowerVia for Advanced High-Performance Computing T1-2 10:55-11:20 Sony Semiconductor Solutions: A Back-illuminated 10 μm-pitch SPAD Depth Sensor with 42.5% PDE at 940 nm using an Optimized Doping Design T1-3 11:20-11:45 Georgia Institute of Technology: Demonstration of Tungsten-Doped Indium Oxide MOSFETs with 3 Angstrom EOT, Improved Stability and High On-Current T1-4 11:45-12:10 TSMC: Performance Step-Up in PMOS with Monolayer WSe_2 Channel T1-5 12:10-12:35 Samsung Electronics: Highly Scalable and Reliable Cell Characteristics for 1Tb 9th Generation 3D-NAND Flash Memory		**C3: Energy Harvesting** C3-1 10:30-10:55 Du, Delft Univ. of Technology: A Fully Integrated SC Converter Hybridizing Dickson and Continuously-Scalable- Conversion-Ratio Topologies with a Wide Bipolar VCR range for Energy Harvesting C3-2 10:55-11:20 Korea Univ.: A Reconfigurable Multi-Level AC-DC/DC-DC Ocean Energy Harvester IC Achieving 77.7% End-to-End Power Efficiency for Triboelectric Nanogenerators C3-3 11:20-11:45 Fudan Univ.: A Globally Optimized 3-D MPPT System for Dual-Band RF Energy Harvesting with Collaborative Source Reconfiguration C3-4 11:45-12:10 Sogang Univ.: 2,771% Power Improvement Triple-source Ground-Symmetric Pile-Up Resonant Energy Harvester			10:30-12:35
12:00-14:00							Diversity Meeting - Hosted by SSCS Women in Circuits				12:00-14:00
14:00-15:40	**C5: Application-Specific ADCs** C5-1 14:00-14:25 Univ. of Michigan: A Calibration-Free 175MHz Bandwidth 60dB SNDR 6th-order Bandpass Cascaded Time-Interleaved Noise-Shaping SAR ADC with Optimum Zero Placement C5-2 14:25-14:50 Delft Univ. of Technology: A 4GHz 2b 5th Order Continuous-Time ΔΣ Modulator with −100.1dBc THD and 122dBFS SFDR in 100MHz BW C5-3 14:50-15:15 The Univ. of Tokyo: A 76.5-dB Dynamic-Range 8-bit 100-MS/s Variable-Range SAR ADC C5-4 15:15-15:40 Univ. of California, Berkeley: A 4-Element Baseband Charge-Domain Beamformer Integrated into 9-bit SAR ADC Achieving 32dB Spatial Notch with 52.1mW	**C4: SRAM and Mask ROM** C4-1 14:00-14:25 TSMC Design Technology Japan: A 3nm FinFET 563kbit 35.5Mbit/mm2 Dual-Rail SRAM with 3.89pJ/access High Energy Efficient and 27.5μW/Mbit 1-cycle Latency Low-Leakage Mode C4-2 14:25-14:50 IBM: A 6+ GHz 128KB Multi-Port L1 Cache using Ground Rule Clean 10T Bitcells in 5nm Technology C4-3 14:50-15:15 TSMC Design Technology Japan: A 13.8% Speed-Enhanced 1T Mask ROM by Algorithmically Signed Program Data on 3-nm Fin-FET Logic CMOS C4-4 15:15-15:40 Synopsys: A 37.8Mb/mm^2 SRAM in Intel 18A Technology Featuring a Resistive Supply-Line Write Scheme and Write-Assist with Parallel Boost Injection		**T2: Oxide Semiconductors 1: Novel Applications and Structures** T2-1 14:00-14:25 TSMC: Integration of 0.75V V_{DD} Oxide-Semiconductor 1T1C Memory with Advanced Logic for An Ultra-Low-Power Low-Latency Cache Solution T2-2 14:25-14:50 National Univ. of Singapore: A 2-Transistor-1-Modulator (2T1M) Electronic-Photonic Hybrid Memory Architecture for Deep Neural Network CIM and Very Large-Scale Transformers T2-3 14:50-15:15 National Univ. of Singapore: BEOL-Compatible ITO FET with Ultra-Short Channel Length of 5 nm T2-4 15:15-15:40 National Univ. of Singapore: A Generalizable Tri-Layer Design Framework for Enhancing OSFET Reliability	**JFS1: 3D Integration and Photonics** JFS1-1 14:00-14:25 (Invited) GlobalFoundries: Key Technologies and Performance Aspects for Electrical and Optical Interconnects JFS1-2 14:25-14:50 (Invited) AIST: 3D Interconnect Technology for Superconducting Quantum Devices JFS1-3 14:50-15:15 Intel: 1.536TB/s/mm2 Bandwidth Scalable Attention Accelerator with 22.5GOPS Throughput High Speed SoftMax for Quantized Transformers in Intel 3 JFS1-4 15:15-15:40 Celestial AI: A 3D-Integrated 56 Gb/s Silicon Photonic Transceiver with 5nm CMOS Electronics for Optical Compute Interconnects		**C6: Imagers** C6-1 14:00-14:25 Samsung Electronics: A 1.22 e-rms Temporal Random Noise, 110 dB High Dynamic Range, 2.988 μm Pixel-Pitch 3-Stacked Digital Pixel Sensor with On-Chip HDR Merger C6-2 14:25-14:50 Sony Semiconductor Solutions: A 0.8μm 32Mpixel Always-On CMOS Image Sensor with Windmill-Pattern Edge Extraction and On-Chip DNN C6-3 14:50-15:15 Carnegie Mellon Univ.: A Multispectral Vision Sensor with Embedded Convolutional Neural Network Using Programmable Fractional Weights and nMOS-Only PWM Pixels C6-4 15:15-15:40 Samsung Electronics: A 12-Mpixel Automotive Image Sensor with 137-dB Single-Exposure Dynamic Range and 0.55-electron Read Noise by Oversampling-Based Noise Reduction		**T3: Modeling and Reliability** T3-1 14:00-14:25 Peking Univ.: Towards Understanding Cryogenic Reliability in FinFETs Under Hot Carrier Stress: *New Findings on Ge Migration, and Impacts of Tail States Evolution* T3-2 14:25-14:50 National Tsing Hua Univ.: High Resolution Well-Plasma Detection Device in 16nm CMOS FinFET Process T3-3 14:50-15:15 National Taiwan Univ.: Unified Physics-Based CFET Thermal SPICE Considering BEOL, Substrate, and BSPDN Using Adiabatic Cones T3-4 15:15-15:40 National Univ. of Singapore: Uncovering True DIBL in Oxide-Semiconductor FETs: Impact of Negative Bias Stress and its Significance in 2T0C DRAM Retention	14:00-15:40
16:00-18:05	**C8: High-Speed ADCs** C8-1 16:00-16:25 The Univ. of Tokyo: An 11.9-ENOB 560-MS/s Subranging ADC Employing Amplifier-Switching Architecture with Multi-Threshold Comparators C8-2 16:25-16:50 Texas A&M Univ.: A 46GS/s 7-bit Time-Interleaved Time-Domain ADC with Synthesizable Unit ADCs in 16nm FinFET C8-3 16:50-17:15 Univ. of Macau: A Single-Channel 14b 3GS/s Pipelined ADC in 28nm Technology C8-4 17:15-17:40 Univ. of Macau: A PVT-Robust 16GS/s 4×TI Time-Domain ADC with Vernier-based Multipath Flash TDC achieving 25.7fJ/c-s FoM in 28nm CMOS	**C7: High-Density Short-Reach Links** C7-1 16:00-16:25 Institute of Semiconductors, Chinese Academy of Sciences: A 4x112-Gb/s, 3.51-pJ/bit Monolithically Integrated Silicon-Photonic Transceiver for High-Density Co-Packaged Optics C7-2 16:25-16:50 Cadence Design Systems: A 0.52pJ/bit 0.448Tbps/mm UCIe Standard Package Die-to-Die Transceiver with Low-Latency TX Clock Alignment in 3nm FinFET C7-3 16:50-17:15 NVIDIA: A 77 fJ/bit 8 Gbps Low-Latency Self-Timed Die-to-Die Link for 2.5D and 3D Interconnect in 3nm C7-4 17:15-17:40 Oregon State Univ.: A 3.2pJ/b 0.068pJ/b/dB 25Gb/s NRZ Wireline Transceiver with 3-tap FFE and Random Forest Classification for Compensating 47dB Loss in 16nm FinFET C7-5 17:40-18:05 KAIST: A 12-Gb/s Single-Ended Transmitter with Echo-Canceling FFE for Multi-drop Bus in 28nm CMOS		**T4: RRAM and MRAM** T4-1 16:00-16:25 National Tsing Hua Univ.: High Density 7nm FinFET Dielectric RRAM in Embedded Memory Applications T4-2 16:25-16:50 Univ. of Chinese Academy of Sciences: First Implementation of Monolithic Integrated CIM with 1Mb Ultra-High-Density 8-Layer 3D VRRAM, Achieving High Computing Density (204.8GOPs/mm^2) and FoM (2.13x10^6 GOPS^2/W/mm^2) for Efficient Scientific Computing T4-3 16:50-17:15 imec: High Density, High Speed STT-MRAM N7 Macros: Material and DTCO Exploration T4-4 17:15-17:40 TSMC: Demonstration of Embedded MRAM with Sub-50 nm MTJ for RAM-Like and MCU Applications T4-5 17:40-18:05 Fudan Univ.: 96-Kb Voltage-Controlled-Magnetic-Anisotropy MRAM for In-situ Reservoir Computing with High Endurance (>10^{12}), Sub-ns Operation (0.3 ns) and Ultralow Power Consumption (40 fJ)	**JFS2: DTCO and Design Enablement** JFS2-1 16:00-16:25 (Invited) TSMC: Analog Cells DTCO and Their Impact on Advanced Node CMOS Analog/Mixed-Signal Circuits JFS2-2 16:25-16:50 (Invited) Qualcomm Technologies: Enhancing Power-Performance-Area Scaling of Std-Cell, SRAM, and Analog Designs through Design-Technology Co-Optimization JFS2-3 16:50-17:15 (Invited) Cadence Design Systems: Backside Routing Enablement Considerations for Advanced Node GAA Devices JFS2-4 17:15-17:40 Samsung Electronics: Realistic and Scalable TCAD for Yield-Aware Full-Chip DTCO JFS2-5 17:40-18:05 Samsung Electronics: Design-Aware Full-Chip Warpage Modeling for STCO: Bridging Reliability and Design for a New Era of Advanced Systems	[Satellite Room] T5	**C9: Advanced Bio-Sensing Techniques** C9-1 16:00-16:25 Univ. of Southern California: Frequency-Division Multiplexed Magnetic Induction Based Wireless Wearable Sensor Network for Real-Time Motion Tracking C9-2 16:25-16:50 POSTECH: A 10.42μW/Ch. PPG Sensor with a Zoomed Sampling Based on Velocity of Blood Flow C9-3 16:50-17:15 KU Leuven: DERMIS: A Flexible Fully-Integrated 600μm-Resolution Per-Taxel Slip-to-Spikes Tactile Sensor Readout on a-IGZO TFT for Large-Area High-Density Electronic Skins C9-4 17:15-17:40 Rice Univ.: A 28nm Online Spike Sorting Processor Based on Multi-Channel Template Matching		**T5: Imagers and Sensors** T5-1 16:00-16:25 Huawei Technologies, Japan: A Monolithic Dual-Layer Pixel Design with BEOL IGZO Transistors featuring High Dual Conversion Gain Ratio and Scaled Pixel Size for Future Image Sensors T5-2 16:25-16:50 Samsung Electronics: Adaptive Metasurface Microlens Array for Ultra-Wide-Angle CMOS Image Sensors T5-3 16:50-17:15 Yonsei Univ.: Back-Illuminated U-Shape p-i-n SPAD With High PDE and Broad Spectral Response Fabricated in 110nm CIS Foundry Technology T5-4 17:15-17:40 Yonsei Univ.: Optimization of a 3.5 μm Pitch 3D-Stacked Back-Illuminated SPAD in 40 nm CIS Technology: Achieving 37% PDP at 940 nm T5-5 17:40-18:05 Samsung Electronics: A 1.2Mp 2.8 um 4-tap Indirect Time-of-Flight Sensor with 42% Quantum Efficiency at 940 nm Wavelength with Enhanced Angular Response	16:00-18:05
18:00-19:30									SSCS/EDS Young Professionals and Women in Circuits Mentoring Event		18:00-19:30
20:00-21:30		Evening Panel Discussion 2 **Practical Circuits & Technology Training: Academia vs. Industry – Where Do We Learn the Most?**		Evening Panel Discussion 1 **What Can Semiconductor Industry Do for Greener Society?**							20:00-21:30

2025 Symposium on VLSI Technology and Circuits (Wednesday, June 11)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Salon de Charme	Le Bois	Le Cygne	Time
7:00-17:00	Registration									7:00-17:00
8:00-10:00		[Satellite Room] Award & Plenary 2		Award and Plenary Session 2 8:00-8:40 *Award Ceremony* PL2-1 8:40-9:20 (Plenary) MediaTek: Enabling Generative AI: Innovations and Challenges in Semiconductor Design Technologies PL2-2 9:20-10:00 (Plenary) STMicroelectronics: The Evolution of Edge AI: Contextual Awareness and Generative Intelligence					8:00-10:00
10:30-12:35	**C11: High-Performance Oscillators** C11-1 10:30-10:55 Huazhong Univ. of Science and Technology: A 0.06mm^2 27.5-to-30GHz Series Resonance VCO with Magnetic Mutual Resistance Achieving 207.2dBc/Hz FoM$_A$ at 10MHz Offset C11-2 10:55-11:20 Fudan Univ.: A 0.06mm^2 14.7-to-20.2GHz Quad-Core VCO Enabled by the Folded Circular Transformer Achieving 201.1dBc/Hz FoM$_T$ and 203.4dBc/Hz FoM$_A$ C11-3 11:20-11:45 Univ. of Illinois at Urbana-Champaign: A 1 ppb MEMS Oscillator Achieving -90 dBc/Hz at 10 Hz Offset Enabled by 5 MΩ TIA and 360° Phase Shifter C11-4 11:45-12:10 Southern Univ. of Science and Technology: A 425pW, 0.3V, 32kHz Crystal Oscillator in 22nm FDSOI with Adaptive Pulse Injection and Amplitude Regulation Across -40°C to 125°C C11-5 12:10-12:35 Nanjing Univ. of Posts and Telecommunications: A 24-MHz Crystal Oscillator with 6.9-µs Startup Time and 2% Injection-ΔF Tolerance Using Phase-Interpolator-Assisted Synchronized Injection	**C10: AI Accelerators 1** C10-1 10:30-10:55 National Tsing Hua Univ.: CATTUS: A 4K-UHD 30fps Deep Image Processor for Channel Attention Equipped U-Net Acceleration in 16nm FinFET C10-2 10:55-11:20 KAIST: NuVPU: A 4.8~9.6 mJ/frame Progressive NTT-based Unified Video Processor for Stable Video Streaming and Processing with Neural Video Codec C10-3 11:20-11:45 Univ. of California, San Diego: Clo-HDnn: A 4.66 TLOPS/W and 3.78 TOPS/W Continual On-Device Learning Accelerator with Energy-Efficient Hyperdimensional Computing via Progressive Search C10-4 11:45-12:10 Univ. of Michigan: EVA: A 16mm^2 1.54TFLOPS Tiled-Based Accelerator for Evolvable Edge Computing C10-5 12:10-12:35 Univ. of California, Berkeley: MAVERIC: A 16nm 72 FPS, 10 mJ/frame Heterogeneous Robotics SoC with 4 Cores and 13 INT8/FP32 Accelerators	**T6: Technology Highlights 2** T6-1 10:30-10:55 imec: High-Density Wafer Level Connectivity Using Frontside Hybrid Bonding at 250nm Pitch and Backside Through-Dielectric Vias at 120nm Pitch After Extreme Wafer Thinning T6-2 10:55-11:20 Micron Technology: Voltage Reduction (1.4V) and Array Scaling (41nm) of Ferroelectric NVDRAM for Low-Power and High-Density Applications T6-3 11:20-11:45 The Univ. of Tokyo: A Gate-All-Around Nanosheet Oxide Semiconductor Transistor by Selective Crystallization of InGaOx for Performance and Reliability Enhancement T6-4 11:45-12:10 Peking Univ.: First Demonstration of 1T FDSOI-based >1000fps Image Sensor with In-Pixel Computing T6-5 12:10-12:35 Huawei Technologies: 1T1C 3D HZO FeRAM with High Retention (>125°C) and High Endurance (>1E13) for Embedded Nonvolatile Memory Application		**C12: Ultra High-speed Wireline** C12-1 10:30-10:55 imec: A 7-bit 150-GSa/s DAC in 5nm FinFET CMOS C12-2 10:55-11:20 Intel: A 128Gb/s 0.67pJ/b PAM-4 Transmitter in 18A with RibbonFET and PowerVia C12-3 11:20-11:45 Marvell Semiconductor: A Monolithic 400Gbps Electro-Optical Retimer with Integrated TIA and Class-AB Silicon-Photonics/VCSEL Driver in 5nm FinFET C12-4 11:45-12:10 Samsung Electronics: A 212.5Gb/s PAM-4 Receiver with Mutual Inductive Coupled Gm-TIA in 4nm FinFET C12-5 12:10-12:35 Marvell Semiconductor: A 128Gb/s ADC/DAC Based PAM-4 Transceiver with >45dB Reach in 3nm FinFET		10:30-12:35
12:35-14:00										12:35-14:00
14:00-15:40	**C14: Analog Techniques** C14-1 14:00-14:25 Univ. College Dublin: A Pipelined-SAR-TDC with Time-Domain Noise-Shaping Self-Calibration C14-2 14:25-14:50 Univ. of Twente: A 0.5-0.8V 10-85 MS/s 12-bit SAR ADC in 22nm FDSOI Utilizing an Inverter-Based Comparator Architecture C14-3 14:50-15:15 Sogang Univ: A G_m-Boosted 3-Stage Amplifier with Gain-Enhancing Feedforward Path for CL of 40-160nF C14-4 15:15-15:40 KAIST: A Boosted 3.5W, -81.6dB THD+N, 92.6% Total Efficiency, Battery-Powered Class-D Audio Amplifier with True-Zero-Switching Achieving Quiescent Current of 0.9mA	**C13: AI Accelerators 2** C13-1 14:00-14:25 KAIST: Adelia: A 4nm LLM Accelerator with Streamlined Dataflow and Dual-Mode Parallelization for Efficient Generative AI Inference C13-2 14:25-14:50 Univ. of Michigan: A 22nm 25.08TOPS/W Multi-Task Transformer Accelerator with Mixed Precision Structured Sparsity and Two-Stage Task-Adaptive Power Management C13-3 14:50-15:15 Cornell Tech: ASAP: A 28nm Transformer Training Accelerator with Alternating Sparsity and Asymmetrical Microscaling Floating-Point Precision C13-4 15:15-15:40 Tsinghua Univ.: A 94Hz Inference and 7.4mJ/epoch Fine-Tune Edge SoC for Diffusion-based Robot Manipulation with Speculation and Disturbance Enhancement	**TFS1: Memories for AI Applications** TFS1-1 14:00-14:25 (Invited) Micron Technology: High Bandwidth Memory for AI TFS1-2 14:25-14:50 (Invited) Samsung Electronics: Emerging Embedded Non-Volatile Memories Beyond 28nm in AI Era TFS1-3 14:50-15:15 Peking Univ.: A Hybrid Monolithic 3D Integration of 2T0C DRAM and RRAM Chip for High-Precision In-Memory Point Cloud Acceleration with Ultra-Fine-Grained Dataflow TFS1-4 15:15-15:40 SK hynix: 224 TOPS/W-level Analog Computation in Memory Cell Using Hybrid Ferroelectric Tunnel Junction Having Enhanced On-State Conductance	**T7: 3D Power Delivery Network** T7-1 14:00-14:25 imec: Backside Power Delivery for Power Switched Designs in 2nm CMOS: IR Drop and Block-level Power-Performance-Area Benefits T7-2 14:25-14:50 POSTECH: A Novel Backside Signal Inter/Intra-Cell Routing Method Beyond Backside Power for Angstrom Nodes T7-3 14:50-15:15 KAIST: Heterogeneous 3D Integration of Low-Voltage E/D-mode GaN HEMTs on CMOS Chip for Efficient On-Chip Voltage Regulation in Active Power Delivery Networks T7-4 15:15-15:40 Tsinghua Univ.: A 10W 3.8-5V Input IVR Chiplet with 93%-Peak-Efficiency and 3.2A/mm^2 Density Featuring Wide Load Range and Adaptive Ganging for 2.5D/3D Vertical Power Delivery	**C16: Hardware Security** C16-1 14:00-14:25 Osaka Univ.: A High-Order Masking with Load-Delay-Equalized WDDL for Provable Side-Channel Security C16-2 14:25-14:50 POSTECH: A 1.7 pJ/bit 10 MHz Calibration-Free PVT Variation and Mismatch Tolerant Latch-Based True Random Number Generator in 4 nm FinFET C16-3 14:50-15:15 Columbia Univ.: GUARD: A Fully-Digital TDC-Based Clock and Voltage Glitch Detector with On-Demand Protection in a 28nm CMOS C16-4 15:15-15:40 National Univ. of Singapore: Online Learning-Based Countermeasure Against Power Analysis Attacks	**C15: Biomedical Readout and Stimulation** C15-1 14:00-14:25 Yonsei Univ.: A Fully Balanced Biphasic Neurostimulator with Body-Coupled Powering and Full-Duplex Communication via Baseband Load Shift Keying C15-2 14:25-14:50 imec: A Flexible HV Stimulator ASIC with Stimulus-Synchronized Charge Balancing and Embedded CM Regulation for Implantable Peripheral Nerve Stimulation C15-3 14:50-15:15 KU Leuven: An N-type-only a-IGZO Thin-Film-Transistor Based Nyquist-rate 8-bit CDAC+SAR ADC Consuming 1.7mW at 32ksps and Achieving 44dB SNDR C15-4 15:15-15:40 KAIST: A 16-QAM-Based Multi-Node BCC System with Bias-Electrode-Free Multi-Channel ExG Readout ICs	**T8: Integrated Optical Devices and Photodetector** T8-1 14:00-14:25 California Institute of Technology: Monolithic Optical Clock Distribution in Bulk CMOS Using I-Beam Waveguides T8-2 14:25-14:50 Harvard Univ.: Digital-to-Optical Converters (DOCs) with Improved Nonlinearity for Energy-Efficient Optical Data Transmission T8-3 14:50-15:15 KAIST: High-Performance Monolithic 3D Integrated Red µLEDoS Display for AR/VR T8-4 15:15-15:40 Zhejiang Univ.: A Heterogeneous CMOS Chip Monolithically integrating Monolayer MoS_2 for Enhanced NUV Detection: A Scalable Platform Leveraging 2D Materials to Complement and Surpass Silicon	14:00-15:40
16:00-18:05	**C18: Power Management** C18-1 16:00-16:25 Sogang Univ.: A 0.087 fs FOM Current-Mirror-Based Analog-Assisted Digital LDO with VO Ripple Optimization C18-2 16:25-16:50 Peking Univ.: Distributed Power Management for 22nm AI Processor with Event-Driven Exponential Dual-Loop LDOs and Online Sparsity-Aware Droop Mitigation C18-3 16:50-17:15 Intel: A Fully Integrated Buck Voltage Regulator in 16nm with in-Package Air Core Inductor Featuring Digital Computational Control for Fast Transient Responses C18-4 17:15-17:40 National Yang Ming Chiao Tung Univ.: An 85.6%-Efficiency Supply Modulator with Auxiliary Bidirectional Power for 200MHz 5G NR Applications C18-5 17:40-18:05 POSTECH: A 90-260 V_{AC} Isolated Offline Single-Stage Single-Transformer-Winding Multiple-Output (STWMO) RGBW LED Driver with <0.7% Current Variation and Dimmable Current-Regulated Error-Based Control	**C17: CIM-based AI Accelerators** C17-1 16:00-16:25 KAIST: DIAL: An Energy-Efficient DRAM In-Memory Computing Accelerator with Compact Partial Product LUT and Twisted Differential ADC C17-2 16:25-16:50 National Tsing Hua Univ.: A 22nm 41.8TFLOPS/W AI-edge Transformer/CNN Nonvolatile-Processor Using QKV-Softmax-Layer-Fused Hybrid ReRAM-CIM and Concurrent-Transpose/Non-Transpose SRAM-CIM C17-3 16:50-17:15 Tsinghua Univ.: CELLA: A 28nm Compute-Memory Co-Optimized Real-Time Digital CIM-Based Edge LLM Accelerator with 1.78ms-Response in Prefill and 31.32 Token/s in Decoding C17-4 17:15-17:40 Univ. of California, Santa Barbara: A Fully Integrated Mixed-Signal Compute-In-Memory Accelerator for Solving Arbitrary Order Boolean Satisfiability Problems	**T10: Advanced CMOS Platform** T10-1 16:00-16:25 imec: Monolithic CFET Flow Improvements Integrating Cover Spacer and Dual-WF RMG T10-2 16:25-16:50 IBM Research: NanoStack Transistor Architecture for CMOS 7A Node and Beyond T10-3 16:50-17:15 Peking Univ.: First Experimental Demonstration of Dual-sided N/P FETs in Filp FET (FFET) on 300 mm Wafers for Stacked Transistor Technology in Sub-1nm Nodes T10-4 17:15-17:40 National Taiwan Univ.: First Demonstration of Monolithic 3-Tier Nanosheet Transistor Stacking with Split Gate Featuring Tri-State Inverter/Half SRAM Functionalities	**T11: Ferroelectric Materials for Memory Applications** T11-1 16:00-16:25 The Univ. of Tokyo: Revealing Wake-Up Mechanism In Ultra-Thin Ferroelectric HZO: Domain De-Pinning Triggered by Oxygen Vacancy Annihilation Exhibiting Optimal Wake-Up Frequency T11-2 16:25-16:50 National Univ. of Singapore: Record-high P_r ($2P_r$ > 40 µC/cm^2) in 3 nm (Physical) Ferroelectric HZO Annealed at 450°C: High-T (85°C) Electrical Cycling and Oxygen Vacancy Engineering T11-3 16:50-17:15 National Taiwan Univ.: Innovative Nb Electrode Engineering for Ultra-Low-Voltage (V_{dd} = 0.8 V) Ferroelectric Memory with Record-High Energy Efficiency: Applications in Selector-Free FeRAM and Neuromorphic Computing T11-4 17:15-17:40 National Taiwan Univ.: Stacked AFE-Like/FE HZO (4.5nm) to Achieve 0.75V Operating Voltage and Record Endurance Exceeding 7E12 Using Water Quenching and TiN Top Electrodes T11-5 17:40-18:05 Fudan Univ.: First Demonstration of Annealing-free RT-prepared AlScN Film with Large Polarization ($2P_r$ > 300 µC/cm^2) and Ultra-Sharp E_c Distribution for 0T1C FeRAM	**C20: Acoustic Sensors** C20-1 16:00-16:25 Delft Univ. of Technology: A -87.2 dB THD+N 89.1 dB DR Fully-Integrated Shunt-Resistor-Based In-Line Current Sensor with up to 2 MHz 14.4 V PWM Rejection C20-2 16:25-16:50 Zhejiang Univ.: A 131-dBSPL AOP 66.3-dB SNR 105.7-µA-Standby All-Dynamic Digital Microphone with Self-Clocked Interference-Resilient Acoustic Activity Detection C20-3 16:50-17:15 Univ. of Macau: A 5.2µW, 2-to-8-Channel Scalable, Speaker-Tracking Microphone Array Featuring a CNN-Defined AFE C20-4 17:15-17:40 ETH Zurich: A 33aFrms, 3.4pF Base Capacitance, 192fF Input Range, 500kHz Sampling Frequency, Capacitance-to-Voltage Converter Using a Resonant LC Bridge C20-5 17:40-18:05 KAIST: A Temperature-Insensitive Period-Modulation CDC with DLL-Based Comparator Delay Compensation Achieving 53.5ppm/°C without Calibration	**C19: Frequency Generation** C19-1 16:00-16:25 Univ. College Dublin: A 24.5-to-45.2-GHz Dual-Injection Clock Multiplier with Folded-Inductor-Based Magnetic-Flux Cancellation Achieving 32.83-fs$_{rms}$ Jitter and 0.037-mm^2 Core Area C19-2 16:25-16:50 Peking Univ.: A Calibration-free ADPLL with < -80 dBc Fractional Spur Based on Pseudo-random Phase Modulation C19-3 16:50-17:15 Univ. College Dublin: A 31.5-36 GHz Low-Spur Gain-Boosting Charge-Sharing Locking PLL with 54fs Jitter C19-4 17:15-17:40 imec: A 2.3-15.8-GHz 8-Phase Injection-Ripple-Filtered Multi-Ring-Coupled DCO Enabling a Wideband Digital PLL	**T9: NAND and NOR** T9-1 16:00-16:25 KIOXIA: A Schottky Junction as a Hole Injector for Enhancing Erase Operation of 3D Flash Memory in CMOS Directly Bonded to Array (CBA) Era with Over 1,000 Word Lines T9-2 16:25-16:50 POSTECH: Low-Temperature NiSi Formation via Microwave Annealing for Stable Metal-Induced Lateral Crystallization in 3D NAND Flash Memory T9-3 16:50-17:15 Micron Technology: Wide Memory Window and Steep ISPP Slope (13.2 V and 2.7) of an Aggressively Scaled 3D Ferroelectric NAND (FeNAND) Cell for <30nm Tier Pitch Scaling T9-4 17:15-17:40 Peking Univ.: 3D NOR-type FeFETs with Record Endurance of 10^{11}, Fast Erase of 50 ns, and Immediate Read-After-Write for In-Memory Learning	16:00-18:05
19:15-21:15	19:15-21:15 **Banquet**					19:15-21:15 **Banquet Lounge Room**				19:15-21:15

2025 Symposium on VLSI Technology and Circuits (Thursday, June 12)

Time	Suzaku III	Suzaku II	Suzaku I	Shunju III	Shunju II	Shunju I	Salon de Charme	Le Bois	La Cigogne	Le Cygne	Time
7:00-17:00	Registration										7:00-17:00
8:30-10:10	**C23: Innovatie Computing Systems**	**C21: Innovations in Brain State Classifcation**		**TFS2: Advanced Transistor Evolution in the Next Decade**		**T12: Oxide Semiconductors 2: IWTO and In_2O_3**	**[Satellite Room] T13**	**C22: OTP and Nonvolatile Memory**		**T13: Power Devices**	8:30-10:10
	C23-1 8:30-8:55	C21-1 8:30-8:55		TFS2-1 8:30-8:55 (Invited)		T12-1 8:30-8:55		C22-1 8:30-8:55		T13-1 8:30-8:55	
	Univ. of Michigan — A 0.71nJ, 1.53GS/s Throughput 256-FFT Using Floating Point Analog Computation	Peking Univ. — PANDA: A 3.178 TOPS/W Reconfigurable Seizure Prediction ANd Detection Neural Network Accelerator for Epilepsy Monitoring		TSMC — Assessment on Nanosheet Transistor Variants Beyond 2nm Node		National Yang Ming Chiao Tung Univ. — First Demonstration of BEOL-compatible ALD-deposited 2 nm-thick Indium-Tungsten-Tin-Oxide (IWTO) TFTs with Superior Short-channel Electrical Characteristics: Achieving Enhancement-mode V_{TH}, $I_{ON/OFF}$> 10^{10}, SS ~ 63.3 mV/dec.		Samsung Electronics — A 2nm Gate-All-Around 128Kb Anti-Fuse One-Time Programmable Memory Featuring Dynamic Bit-Line and Sense-Amplifier Offset Cancellatio		Peking Univ. — 3-kV GaN Smart Power Integration Platform for High-Power-Density Conversion Systems Using Charge-Balanced Superjunction Technology	
	C23-2 8:55-9:20	C21-2 8:55-9:20		TFS2-2 8:55-9:20 (Invited)		T12-2 8:55-9:20		C22-2 8:55-9:20		T13-2 8:55-9:20	
	Univ. of Michigan — An OFDMA Baseband Processor Enabling 165μW Long-Range IoT Localization	Delft Univ. of Technology — A Closed-Loop Neuromodulation Chipset with 0.0009mm²-0.36μW/Ch Recording Frontend and 0.075mm²-6.76μW Seizure Classification Backend		Intel — Beyond RibbonFET: Energy Efficiency Innovations to Drive Technology and Design for the Next Decade		Nara Institute of Science and Technology — ALD Polycrystalline Ga-Doped In_2O_3 (Poly-IGO) Nanosheet Exceeding Intrinsic Mobility of 120 cm^2/Vs for Process-Friendly BEOL-Compatible FET Application		Intel — GAA Backside-Power eFuse with 0.72um2 Bitcell, 1.59V Field Program, On-Demand Read and 1.8V Standby		Southeast Univ. — Improving Irradiation Reliability of 4H-SiC 1200V LDMOS and 20V CMOS Logic Circuits with Leakage Current Blocking Technology	
	C23-3 9:20-9:45	C21-3 9:20-9:45		TFS2-3 9:20-9:45		T12-3 9:20-9:45		C22-3 9:20-9:45		T13-3 9:20-9:45	
	Huazhong Univ. of Science and Technology — A 28nm 84.9KOPS 1.82μJ/op RISC-V Crypto-SoC with Primitive-based Deep-coupling Unified Post-Quantum Engine	KAIST — A No-Patient-Data Seizure Classifier SoC for Real-Time Classification of Seven Seizure Types Using Feature Fusion and Near-Memory Computing		Samsung Electronics — 3D Stacked FET (3DSFET) Logic and SRAM Technology Featuring Single Diffusion Break (SDB) and Back Side Interconnect (BSI) at 48 nm CPP for Advanced Mobile and High Performance Computing (HPC) Applications		Purdue Univ. — Critical Role of Quantum Confinement on Transfer Length in Achieving High-Performance In_2O_3 Transistors with Ultra-Scaled Contacted Gate Pitch		Samsung Electronics — A 4.2 Gb/s 5th generation F-chip of Toggle 5.1 Specification with All-Path Speed Boosting Scheme and SCA Protocol for High Density NAND Flash Applications		imec — High Power/PAE (27.8dBm/66%) Emode GaN-on-Si MOSHEMTs for 5V FR3 UE Applications	
	C23-4 9:45-10:10	C21-4 9:45-10:10		TFS2-4 9:45-10:10		T12-4 9:45-10:10		C22-4 9:45-10:10			
	Industrial Technology Research Institute — Enabling Privacy-Preserving Collective Intelligence: A Twin In-Memory Encryption/Processing Macro Featuring Group Differential Privacy and Spatial-Temporal Ensemble	EPFL — A 32-Channel 196-μW Logarithmic SoC for Brain Network Connectivity Extraction and Adaptive Psychiatric Symptom Classification		IBM Albany NanoTech — Compressive Diffusion Break Stressor for Gate-All-Around Nanosheet pFET Transistor Performance Improvement		National Taiwan Univ. — First Demonstration of 2-floor GAA In_2O_3 Nanosheet FET Enabled by TiN Sacrificial Layers and Fluorine Passivation		TSMC Design Technology — A Prototype 16Mbit RRAM on 55nm BCD with 56% Compact-Area Wordline Driver and Constant Write-Current Scheme for Automotive 150°C Operation			
10:30-12:35	**C25: Advanced PLLs**	**JFS3: AI and ML Hardware**		**T15: 2D and BEOL Transistors**		**C24: Circuit Techniques for Biomedical Applications**	**[Satellite Room] T14**	**C26: Switching Regulators**		**T14: RRAM and Selector Only Memory**	10:30-12:35
	C25-1 10:30-10:55	JFS3-1 10:30-10:55 (Invited)		T15-1 10:30-10:55		C24-1 10:30-10:55		C26-1 10:30-10:55		T14-1 10:30-10:55	
	Politecnico di Milano — A Fractional-N Digital-PLL Based on a Power-Gated Ring-Oscillator and a Frequency-Stabilizing Loop Achieving 74fs Jitter Under 3mV$_{pp}$ Supply Ripple	Cerebras Systems — Wafer-Scale Integration for AI – The Holy Grail?		Intel — Record PMOS WSe_2 GAA Performance Using Contact Planarization, and Systematic Exploration of Manufacturable, High-yield Contacts		KU Leuven — An Active Silicon Perforated MEA for Seamless 3D Organoid Interfacing with Low-Noise, Scalable Multimodal Electrophysiology		Univ. of Macau — A 9.1mW All-5V-CMOS Series-Capacitor AC-DC Converter with C_F Reallocation Operations for 85-230V_{RMS} Mains Achieving 85.6% Efficiency at 858mW/cm² Density		TSMC — A CMOS-Compatible 12nm 8Mb MLC RRAM Enabling Producible 2-Bit Per Cell for High Energy Efficiency Compute-In-Memory in Edge AI Applications	
	C25-2 10:55-11:20	JFS3-2 10:55-11:20 (Invited)		T15-2 10:55-11:20		C24-2 10:55-11:20		C26-2 10:55-11:20		T14-2 10:55-11:20	
	Politecnico di Milano — A 58.9fs-Jitter Fractional-N Digital PLL Using a Double-Edge Variable-Slope DTC	Huawei — Design Considerations for LLM Inference in Data Centers: Chip and Interconnect		National Univ. of Singapore — First Demonstration of BEOL-Compatible Co-Sputter Deposited $Te_{1-x}Se_x$ p-FETs Enabling 3D Stackable Oxide Semiconductor CFET, DRAM, and First CFET-Structured SRAM		Yonsei Univ. — A 10kHz-BW, 86.7dB-SNDR, 176.8dB-FoM, LNA-Embedded CT ΔΣ ADC for Closed-Loop Neural Recording		Univ. of Science and Technology of China — A 16-24V to 1-1.8V 1.187W/mm³-Power-Density Hybrid DC-DC Converter Featuring Inductor Current in Σ-Fibonacci Region for Unmanned Aerial Vehicle Applications		SK hynix — Achieving Outstanding Endurance (> 10^{7}) in Large-Array Two-Deck 16 nm SOM through Process, Structure, and Design Strategies for Emerging SCM Applications	
	C25-3 11:20-11:45	JFS3-3 11:20-11:45 (Invited)		T15-3 11:20-11:45		C24-3 11:20-11:45		C26-3 11:20-11:45		T14-3 11:20-11:45	
	The Hong Kong Univ. of Science and Technology — A 6.4GHz Fractional-N PLL with 96.6fs$_{rms}$ Jitter and -257.4dB FoM	NVIDIA — Marco: Configurable Graph-Based Task Solving and Multi-AI Agents Framework for Hardware Design		National Yang Ming Chiao Tung Univ. — Homo-Channel WSe_2 n/pFETs with High Performance and On/Off Ratio Using Tunable Doping		Rice Univ. — 38kbps Multi-Access Magnetoelectric Backscatter Communication with Non-Interrupted WPT for a Network of Miniature Wireless Bio-Implants		POSTECH — A 94.1%-Efficiency Flying-Capacitor-Shared 2-Inductor 3-Level Boost Converter with Simultaneous V_{CF} and I_L Balance Achieving <0.92%-V_{CF} and <0.22%-I_L Error		Samsung Electronics — Scalable Fabrication and Demonstration of the First Fully Integrated 14nm 2-Stack SOM (Selector Only Memory) Device	
	C25-4 11:45-12:10	JFS3-4 11:45-12:10		T15-4 11:45-12:10		C24-4 11:45-12:10		C26-4 11:45-12:10		T14-4 11:45-12:10	
	MIT — A 55.8-to-64.2GHz, 58.3fs$_{rms}$-Jitter, -250.2dB-FoM$_J$ Fractional-N Cascaded PLL in 28nm CMOS	National Taiwan Univ. — An 157TOPS/W Transformer Learning Processor Supporting Forward Pass Only with Zeroth-Order Optimization		TSMC — 1000x Lower Leakage in High-Performance Carbon Nanotube Nanosheet FETs		Univ. of Michigan — 128-Channel Multi-Chip Acoustic Hologram Generator		Delft Univ. of Technology — Matryoshka CSCR: A Reconfigurable Matryoshka-Stacked Continuous-Scalable-Conversion-Ratio Switched-Capacitor DC-DC Converter with 0.1-to-1.7V Input		POSTECH — Multi-Stack InTe Selector-Only Memory (SOM) Achieving Ultra-Low Power Operation (10 μA) and Excellent Endurance (~ 10^{10} cycles)	
		JFS3-5 12:10-12:35		T15-5 12:10-12:35						T14-5 12:10-12:35	
		Weebit Nano FR — On Chip Customized Learning on Resistive Memory Technology for Secure Edge AI		Samsung Advanced Institute of Technology — Wafer-Scale Monolithic 3D Integration of CMOS Logic Gates Based on 2D Materials						Samsung Advanced Institute of Technology — Differences in Operational Mechanisms of As- and Sb-Based Selector Only Memory for Emerging 3DXP Architecture	
12:35-14:00											12:35-14:00
14:00-15:40	**C30: Cryo-CMOS Circuit**	**C29: Communication and Processors**	**T19: Gate Stack and BEOL Transistor Processes**	**T18: Interconnects**	**T17: Oxide Semiconductors 3: Device Physics and Reliability**	**C27: Sensing and Ranging Technologies**	**[Satellite Room] T16**	**C28: Sub-THz TRXs**		**T16: FeRAM Array and Module**	14:00-15:40
	C30-1 14:00-14:25	C29-1 14:00-14:25	T19-1 14:00-14:25	T18-1 14:00-14:25	T17-1 14:00-14:25	C27-1 14:00-14:25		C28-1 14:00-14:25		T16-1 14:00-14:25	
	IBM T. J. Watson Research Center — A 5.6-100K, 128ppm/K Cryo-CMOS Current Reference	National Taiwan Univ. — A 142mW 6.4Gbps Massive MU-MIMO RSMA Detector for Next-Generation Communication Systems	Stanford Univ. — Orthogonal V_T Tuning for Oxide Semiconductor 2T Gain Cell Enabled by Interface Dipole Engineering	IBM Albany NanoTech — Novel Advanced Low-k Dielectric for 2 nm and Beyond Cu and Post Cu Dual Damascene BEOL Interconnect Technologies	Stanford Univ. — Key to Low Supply Voltage: Transition Region of Oxide Semiconductor Transistors	Canon — 2/3-inch 2.1Megapixel SPAD Image Sensor with 156dB Single-Shot Dynamic Range and LED Flicker Mitigation Based on Weighted Photon Counting Technique		Institute of Science Tokyo — A 150 GHz High-Power-Density Phased-Array Transceiver in 65nm CMOS for 6G UE Module		Samsung Electronics — Designing Robust Interfaces of HZO Module (>10^{12} at 85 °C) with High Sensing Margin (>300 mV) for ≤1.1 V 1T-1F with Common Plate Line and 1T-nF FeRAM	
	C30-2 14:25-14:50	C29-2 14:25-14:50	T19-2 14:25-14:50	T18-2 14:25-14:50	T17-2 14:25-14:50	C27-2 14:25-14:50		C28-2 14:25-14:50		T16-2 14:25-14:50	
	Univ. of Macau — A Cryo-CMOS RF-DAC Based Super-heterodyne Transmitter for Superconducting Qubit Control	Univ. of Michigan — A 6.2mm² 56.6Gbps 18.2pJ/b oFEC Decoder for Optical Communications	SKLFTIC, IMECAS — First Demonstration of 9N+9P Complete Dipole Multi-V_Ts CMOS Integration with Atomic Interfacial Dipole Buffer Layer Technique in GAA NSFETs	Applied Materials — BEOL Interconnects for 2nm Technology Node and Beyond	National Univ. of Singapore — First Demonstration of Fluorine-Treated IGZO FETs with Record-Low Positive Bias Temperature Instability ($\|\Delta V_{TH}\|$ < 44 mV) at an Elevated Temperature (395 K)	Sony Semiconductor Solutions — A 25M points/s Back-Illuminated Stacked SPAD Direct Time-of-Flight Depth Sensor with Equivalent Time Sampling for Automotive LiDAR		Institute of Science Tokyo — A 52Gb/s 8.9dBm EIRP 300GHz-Band Amplifier-Last Outphasing Transmitter with Path Mismatch Calibration in 65nm CMOS		Univ. of Notre Dame — Vertical 2T-nC FeRAM Demonstration: BEOL Read Transistor for 4F² Memory Strings and Two-Terminal Selector Design for Polarization Disturb Mitigation	
	C30-3 14:50-15:15	C29-3 14:50-15:15	T19-3 14:50-15:15	T18-3 14:50-15:15	T17-3 14:50-15:15	C27-3 14:50-15:15		C28-3 14:50-15:15		T16-3 14:50-15:15	
	Tsinghua Univ. — A Cryogenic 1.08mW/Qubit Fully-Integrated 4-Channel Frequency-Division-Multiplexing Transmon Qubit State Readout ASIC in 28nm Bulk CMOS	Univ. of California, Berkeley — Cygnus: A 1 GHz Heterogeneous Octa-Core RISC-V Vector Processor for DSP	imec — Shifter materials and Stack Explorations for V_t Fine-Tunable Dual Dipole Multi-V_t Gate Stacks Compatible with Low Thermal Budget CFET	imec — Selective Deposition and Ruthenium Superfill Exploration Beyond A10 Node Interconnects	IMECAS — First Demonstration of Atomic-Interlayer-Tuning Driven by First Principles Calculations and Atomic Layer Deposition towards High Thermal Stable BEOL IGZO-FETs with SS=62mV/dec, PBTI < 7mV@ 3MV/cm and 353K	Kyoto Univ. — A Radiation-Hardened Neuromorphic Imager with Self-Healing Spiking Pixels and Unified Spiking Neural Network for Space Robotics		Univ. of Science and Technology of China — A 0.184 mm² ***W***-band Single-RTWO-Based Subharmonic RX Achieving 3.72 dB-NF and I/Q Mismatch < 0.8° in 22nm CMOS		Intel — FeRAM Capacitor with Novel Low-Power, Non-Destructive and High Endurance Read Operation for High-Density Embedded Memory	
	C30-4 15:15-15:40	C29-4 15:15-15:40	T19-4 15:15-15:40	T18-4 15:15-15:40	T17-4 15:15-15:40	C27-4 15:15-15:40		C28-4 15:15-15:40		T16-4 15:15-15:40	
	AIST — 0.25 mW/qubit, 5.7-7.5 GHz Cryogenic CMOS Microwave Signal Selector Using Dual-Stage Injection-Locked Oscillator for Frequency-Multiplexed Qubit Control	KU Leuven — A 16nm 550 - 1320 BTOPS/W NPU Exploiting Training-free Structured Bit-level Sparsity and Dynamic Dataflow Processing	Korea Univ. — High-Performance Monolithic 3D CMOS Enabled by Orientation-Aligned Seedless Laser Crystallization and Ultra-Shallow Laser Activation	Samsung Electronics — Effects of Adjacent Floating Metal Interconnect Through Plasma-Induced Coupling	Shanghai Jiao Tong Univ. — First Direct Observation of Two Different Hydrogen-Related Processes Corresponding to the Negative VTH Shift Under PBTI Stress in IGZO Transistors by Pd Hydrogen Spillover	Intel — A 320μm² Minimum Guard-band Metal Resistor-based Temperature Sensor with +/-1.4°C Inaccuracy in 18A RibbonFet CMOS with PowerVia		Univ. of California Irvine — A CMOS Antenna-to-Bits 230-mW 120-Gbps F-band Receiver with Analog-Domain 64QAM Detection and Extraction		KAIST — Exploring FeFET Degradation Mechanisms: Mid-Interlayer as a Viable Solution for Stable Retention, Disturb Immunity, and Low V_{th} Variation	
16:00-18:05	**C33: Wireless Power and Gate Drivers**	**C32: High-Resolution ADCs**	**C31: MEMS and Display**	**T21: Advanced Packaging and 3D Integration**	**T22: DTCO and Design Enablement**	**T20: DRAM**	**[Satellite Room] T21**		**[Satellite Room] T21**	**T23: Wireless and RF Devices**	16:00-18:05
	C33-1 16:00-16:25	C32-1 16:00-16:25	C31-1 16:00-16:25	T21-1 16:00-16:25	T22-1 16:00-16:25	T20-1 16:00-16:25				T23-1 16:00-16:25	
	The Hong Kong Univ. of Science and Technology — A 6.78 MHz Multiple-Transmitter Wireless Power Transfer System with Integrated Coupling Coefficient Sensor	Peking Univ. — An 88.8dB-SNDR 6-MS/s Pipelined SAR ADC with A Closed-Loop Dynamic Amplifier Featuring Highly-Linear Full-Scale Output Swing	Infineon Technologies AG — A Fully Integrated Bipolar 1.8Vpp-to-41Vpp 450kHz Switched-Capacitor MEMS-Driver with a Power Reduction Factor of 16.3	UCLA CHIPS — Power Delivery for Scaled-Out Chiplet-Based Wafer-Scale Systems with 8 μm Cu-Cu Bond Pitch on Active Si-Interconnect Fabric Substrate	imec — Extending the Gate-All-Around (GAA) era to the A10 node: Outer Wall Forksheet Enabling Full Channel Strain and Superior Gate Control	imec — Process Insights into 3D-DRAM with Vertical Bit Line and Scalable GAA Transistor				TSMC — Compact, Low-Loss, Cost-Effective, CMOS Embedded RF Switch Solution Achieving DC-100GHz True-Time Delay Phase Shifter by Phase Change Material	
	C33-2 16:25-16:50	C32-2 16:25-16:50	C31-2 16:25-16:50	T21-2 16:25-16:50	T22-2 16:25-16:50	T20-2 16:25-16:50				T23-2 16:25-16:50	
	KAIST — A Multi-Rectenna, Single-Output, Power Combine-and-Regulate Boost Converter for 5.8GHz Wireless Power Receiver Achieving 3.1W over 50m-Distance	Yonsei Univ. — A 91.2dB-SNDR 250kHz-BW CT Zoom ADC Achieving a 6-bit Linear Zoom-in with Interstage LPF and 1.5-bit DAC	Xidian Univ. — A 22μg/√Hz Noise Floor, 1.6mg/g² VRC, High Efficiency MEMS Capacitive Accelerometer using High-Voltage Orthogonal Excitation Technique	Applied Materials — Investigation of Post-Bonding Die Stretching in Die-to-Wafer Hybrid Bonding	imec — SRAM Scaling Opportunities Below 0.01 μm² Using Double-Row CFET Architecture with Wordline-Folded BitcellDesign for Performance Optimization	Samsung Electronics — High Performance and Reliable 4F² IGZO Vertical Channel Transistor (VCT) with Extremely Low Contact Resistance and 10 Year BTI lifetime for Sub-10nm DRAM				Xidian Univ. — First Demonstration of Top T-gate BEOL-Compatible Indium-Oxide RF Transistors with Record Maximum Oscillation Frequency of 70 GHz	
	C33-3 16:50-17:15	C32-3 16:50-17:15	C31-3 16:50-17:15	T21-3 16:50-17:15	T22-3 16:50-17:15	T20-3 16:50-17:15				T23-3 16:50-17:15	
	Hanyang Univ. — A Wireless Power and Synchronized Full-Duplex Data Transceiver IC with 400 kbps Bidirectional Data Rate Using a Single Inductive Link for Low-power Systems	Tsinghua Univ. — A 0.0035mm² 86dB-SNR 1.25MHz-BW Noise-Shaping SAR ADC Enabling kT/C Noise Shaping	Fudan Univ. — A 560μW 6fA/√Hz 146dB-DR Ultrasensitive Current Readout Circuit for PWM-Dimming-Tolerant Under-Display Ambient Light Sensor	Powerchip Semiconductor Manufacturing — Novel Ultra-thin Transistor Layer Transfer (TLT) Technology for Demonstrating Wafer-Level nm-Scale 3-Layer Stacking to Enable Multi-Tier Transistors and Backside PDN of a 3D Vertical FET Architecture	Peking Univ. — PPA Scaling of Flip FET Technology Down to A2 Node Enabled by Architecture Innovations: Self-aligned Gate, 2T Design with Embedded Power Rail and Ultra-stacked 4-Tier Transistors	KIOXIA — First Thorough Assessment of Time-Dependent Dielectric Breakdown in Sub-25 nm Gate-All-Around Vertical InGaZnO Transistor for 4F² DRAM Application				IBM Research - Zurich — Scaled-Footprint Ultra-Low Power Cryogenic InGaAs/InP HEMTs with Record-High Combination of Low-Noise and High-Frequency Performance	
	C33-4 17:15-17:40	C32-4 17:15-17:40	C31-4 17:15-17:40	T21-4 17:15-17:40	T22-4 17:15-17:40	T20-4 17:15-17:40				T23-4 17:15-17:40	
	Southern Univ. of Science and Technology — A Dual-Mode Direct-Drive D-GaN Driver with Reused Inductor and Power Switches for Negative Voltage Generation and Gate Energy Recycling	Tsinghua Univ. — A 94.4dB-SNDR 500kHz-BW Multi-Rate MASH 0-1-0 ADC with Easy-to-Drive Capacitive Input and Deadband-Embedded Gm-C Loop Filter	Korea Univ. — A Hybrid Touch Sensing AFE with Common-CVQ (Currents, Voltages, and Charges) Subtraction to Improve Display Noise Immunity for Large Sensing Load Up to 820pF	National Univ. of Singapore — First Demonstration of 3D Monolithic-Integrated BEOL OSFETs on GaN HEMTs: CEO-GaN	Peking Univ. — First Demonstration of Symmetric Dual-Sided Vertical FET (DSVFET) for Energy Efficient Computing (EEC): From Processes and Devices to Circuits	Macronix International — A Recall-Free 3D Stackable nvDRAM Built Upon Gate-Controlled Thyristor				Kyungpook National Univ. — Cryogenic $In_{0.8}Ga_{0.2}As$ Quantum-Well High-Electron Mobility Transistors from Low-Power Quantum Computing to Tera-Hz Applications	
	C32-5 17:40-18:05					T20-5 17:40-18:05 (Late News)				T23-5 17:40-18:05	
	Univ. of Michigan — An NS-SAR Quantizer-Based Pipeline Incremental Delta-Sigma ADC Using a Current-Regulated Floating Ring Amplifier and Two-Phase Miller Negative-C					SK hynix — 4F² DRAM Integration with Vertical Gate (VG) Cell Transistor and Peri-Under-Cell (PUC) Architecture				KAIST — Cryogenic $In_{0.8}Ga_{0.2}As$ Quantum-Well High-Electron Mobility Transistors from Low-Power Quantum Computing to Tera-Hz Applications	